

General Description

SY205236ABC is a low-capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With a typical capacitance of 3.5pF, SY205236ABC is designed to protect against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD) ($\pm 30\text{kV}$ air, $\pm 30\text{kV}$ contact discharge), IEC 61000-4-5 (lightning) (20A, 8/20 μs).

The combined features of low capacitance, small size and high ESD robustness make SY205236ABC ideal for high-speed data ports and high-frequency lines (e.g., USB2.0) applications. The low clamping voltage of the SY205236ABC guarantees minimum stress on the protected IC.

Each SY205236ABC device can protect four high-speed data lines. The SY205236ABC is available in a compact SOT23-6 package.

Features

- Transient Protection for High-Speed Data Lines
 - IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (Air) $\pm 30\text{kV}$ (Contact)
 - IEC 61000-4-5 (Lightning) 20A (8/20 μs) Cable Discharge Event (CDE)
- Package Optimized for High-Speed Lines
- Small Package (2.9mm \times 2.8mm \times 1.4mm)
- Protects Four Data Lines
- Low Capacitance: 3.5pF @ 0V (Typical)
- Low Leakage Current: 0.1 μA @ V_{RWM} (Typical)
- Low Clamping Voltage
- Each I/O pin can withstand over 1000 ESD strikes for $\pm 8\text{kV}$ contact discharge.

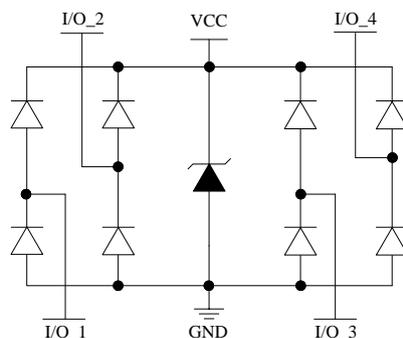
Applications

- USB2.0 Power and Data Line Protection
- Digital Visual Interfaces (DVI)
- 10/100/1000M Ethernet Interfaces
- Desktops, Servers, and Notebooks
- Monitors and Flat Panel Displays
- Video Graphics Cards
- SIM Ports

Mechanical Characteristics

- SOT23-6 Package
- MSL-1 Level
- Flammability Rating: UL 94V-0
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

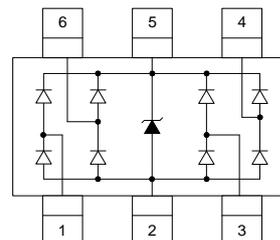
Circuit Diagram



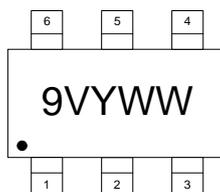
Ordering Information

Part Number	Package Type	Top Mark
SY205236ABC	SOT23-6 RoHS Compliant and Halogen Free	9VYWW

Pinout (Top View)



Marking Codes



Note 1: "9V" is device code, fixed.

Note 2: "YWW" is date code.

Absolute Maximum Rating				
Parameter	Symbol	Min	Max	Unit
Maximum Peak Pulse Current (8/20μs)	I_{PP}		20	A
Maximum Peak Pulse Power (8/20μs)	P_{PK}		350	W
ESD per IEC 61000-4-2 (Air)	V_{ESD}	-30	30	kV
ESD per IEC 61000-4-2 (Contact)				
Operating Temperature	T_{OPT}	-55	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics ($T_A = 25^\circ\text{C}$)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	V_{RWM}				5.0	V
Reverse Leakage Current @ V_{RWM}	I_R	$V_{RWM} = 5\text{V}, T_A = 25^\circ\text{C}$ From I/O to GND		0.1	1.0	μA
Reverse Breakdown Voltage @ I_T	V_{BR}	$I_T = 1\text{mA}$ From I/O to GND	6.0			V
Clamping Voltage @ I_{PP}	$V_C(1)$	$I_{PP} = 20\text{A}, t_p = 8/20\mu\text{s}$ From I/O to GND		15	17	V
Clamping Voltage @ I_{PP}	$V_C(1)$	$I_{PP} = 16\text{A}, t_p = 10/100\text{ns(TLP)}^2$ From I/O to GND		9.5	11.5	V
Dynamic Resistance	$R_{DYN}(1)$	$t_p = 10/100\text{ns(TLP)}^2$ From I/O to GND		0.15		Ω
Parasitic Capacitance	$C_{ESD}(1)$	$V_R = 0\text{V}, f = 1\text{MHz}$ From I/O to GND		3.5	5.0	pF
Parasitic Capacitance	$C_{ESD}(1)$	$V_R = 0\text{V}, f = 1\text{MHz}$ Between I/O and I/O		1.5	2.5	pF

Note 1: Guaranteed by design and not subject to production test.

Note 2: Transmission Line Pulse Test (TLP) Settings: $t_p=100\text{ns}$, $t_r = 10\text{ns}$, I_{TLP} and V_{TLP} averaging window: $t_1 = 70\text{ns}$ to $t_2 = 90\text{ns}$.

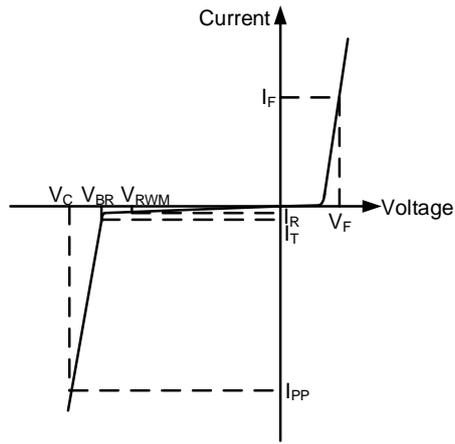
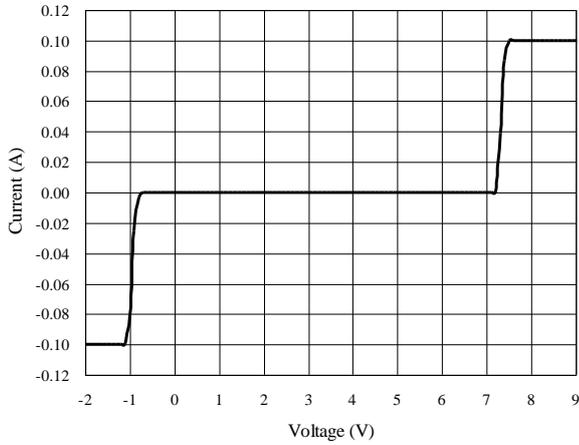


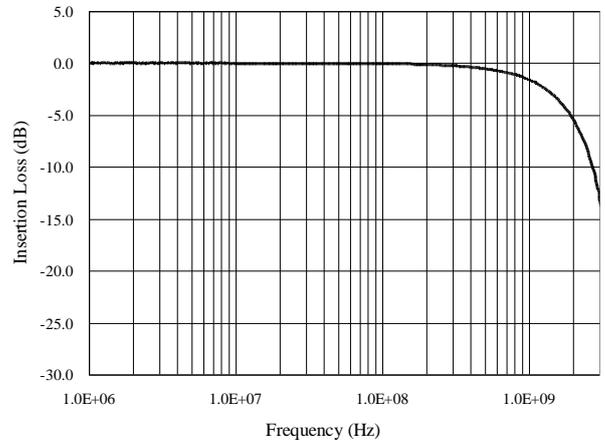
Figure 1. Uni-directional TVS

Typical Characteristics

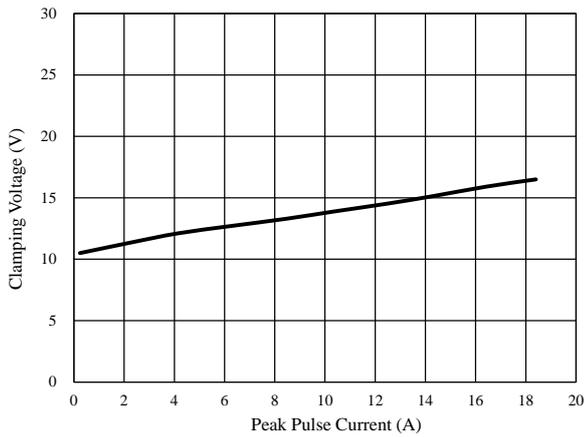
Voltage Sweeping of I/O to GND



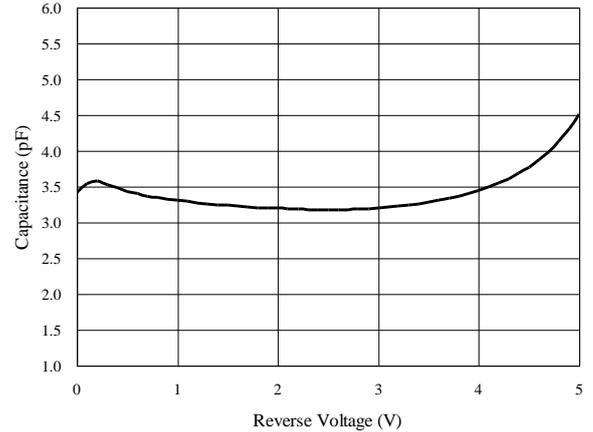
Insertion Loss S21 of I/O to GND



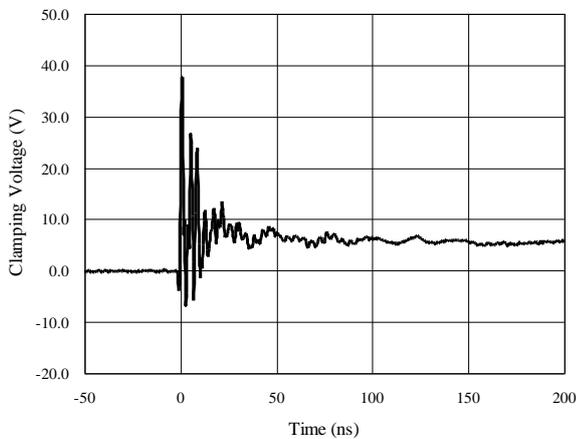
Clamping Voltage vs. Peak Pulse Current



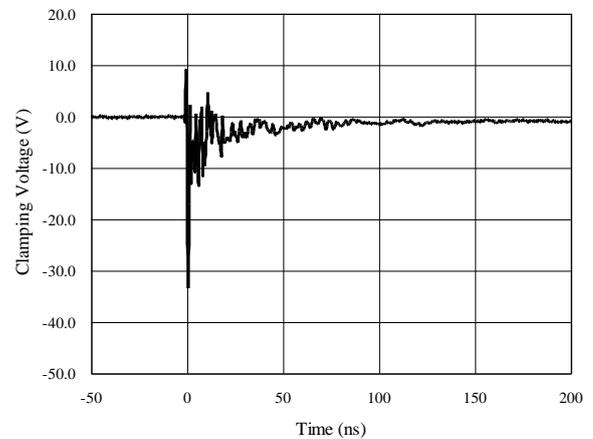
Capacitance vs. Reverse Voltage



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connections

SY205236ABC is designed to provide ESD protection for four data lines simultaneously. The pin connections are shown in Figure 2.

You can connect four parallel data lines from the inner IC to the I/O port connector directly to the four SY205236ABC I/O pins. Pin2 of SY205236ABC is the negative reference pin, which should connect to the ground. Pin5 of SY205236ABC is the positive reference pin, which should connect to the power supply of the PCB. The connection wires should be as short as possible to minimize the parasitic inductance.

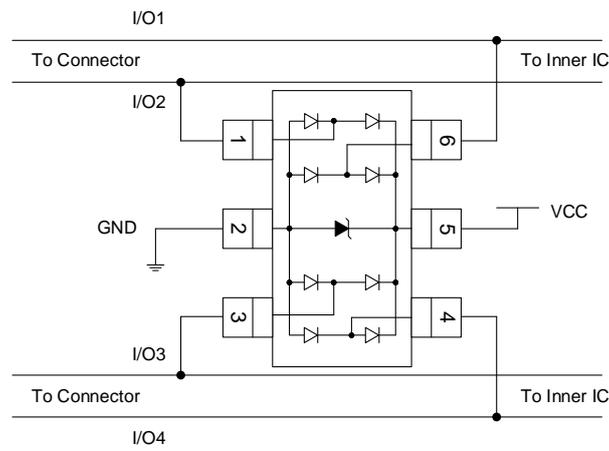


Figure 2. SY205236ABC Pin Connection in PCB

Clamping Voltage Optimization

The SY205236ABC device can use its power clamping circuit to limit the TVS clamping voltage (V_C) to a suitable value during positive and negative mode ESD stress. For example, as shown in Figure 3, if there is no power clamping circuit in SY205236ABC, the I_{ESD1} will be the ESD shunting current from I/O to VCC via D1 and L_p . The V_C at I/O port will be:

$$(1) V_C = V_{F,D1} + L_p \frac{dI_{ESD1}}{dt} + V_{CC}$$

Note: $V_{F,D1}$ is the forward turn-on voltage of the steering diode D1, and L_p is the parasitic inductance in the ESD current shunting path.

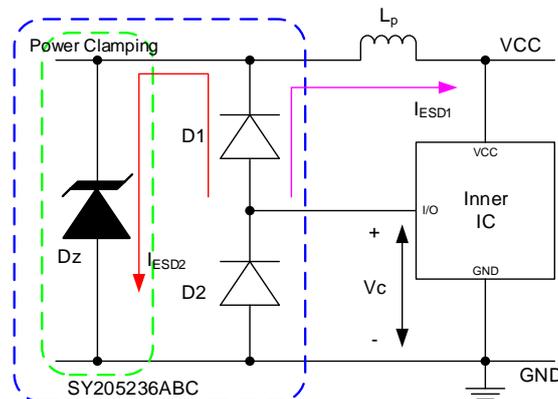


Figure 3. Positive ESD Clamping Voltage Optimization

Without a power clamping circuit, an ESD pulse could discharge a large current in a very short time (potentially ranging from 0.2ns to 10ns) causing the V_C to exceed the inner circuit capability. However, utilizing the power clamping circuit in SY205236ABC will result in the ESD shunting current as I_{ESD2} . The V_C will be:

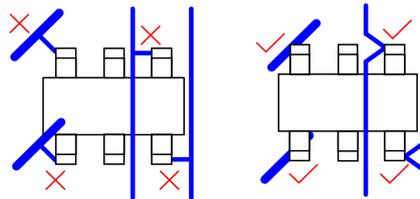
$$(2) \quad V_C = V_{F,D1} + V_{BR,Dz} + V_{CC}$$

Note: $V_{BR,Dz}$ is the reverse breakdown voltage of diode D_z , which is much smaller than the induced clamping voltage by parasitic inductance L_p in equation (1).

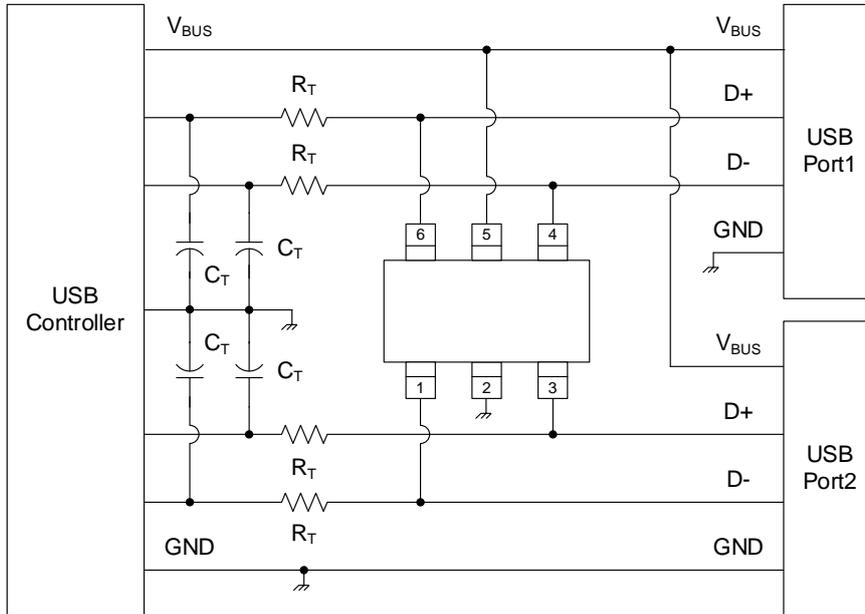
PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

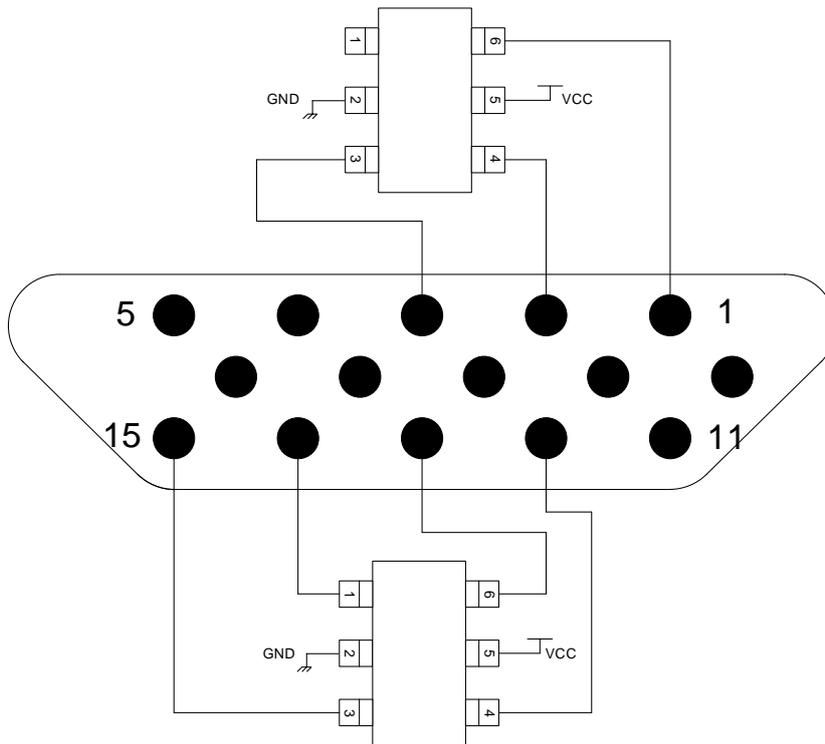
- Place SY205236ABC as close to the connector port as possible.
- The distance between the SY205236ABC ground pin and the GND reference path should be as short as possible.
- Use a large via to connect the SY205236ABC VCC and GND pins to the PCB VCC and GND.
- Avoid running critical signals near board edges.



Application Information (continued)

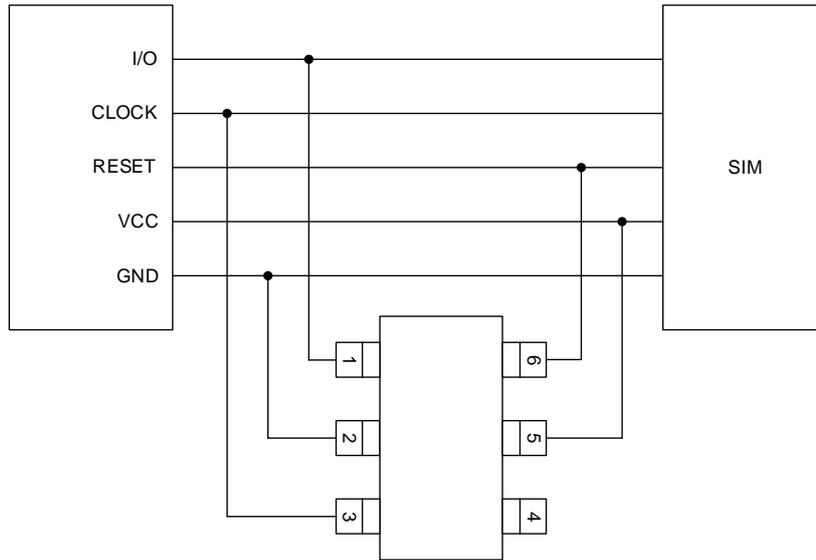


Layout Top View for Dual USB Ports with SY205236ABC

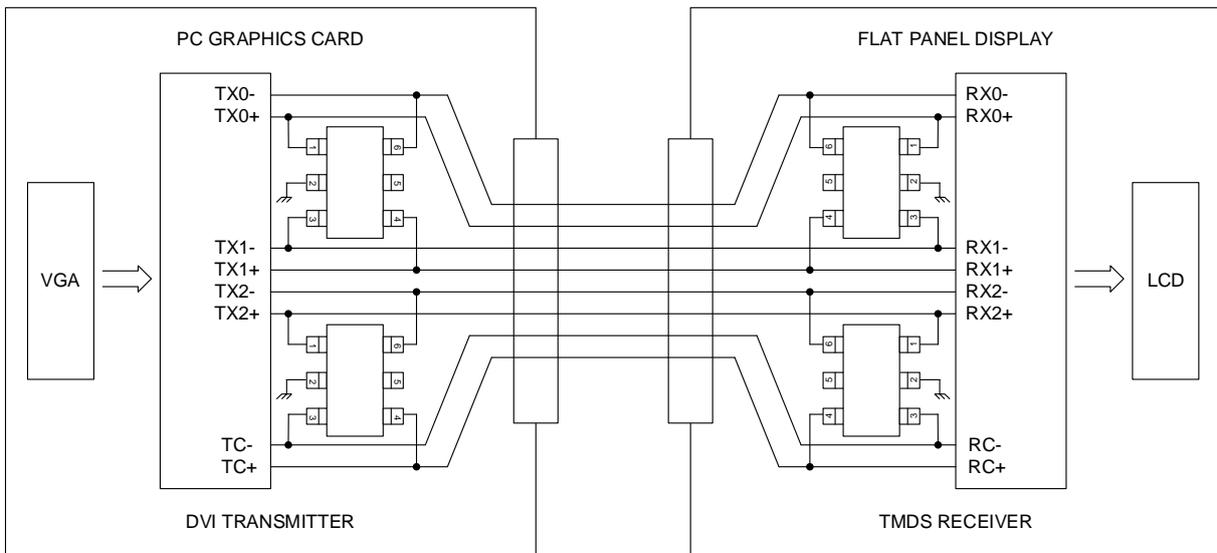


Layout Top View for Video (VGA) Interface with SY205236ABC

Application Information (continued)

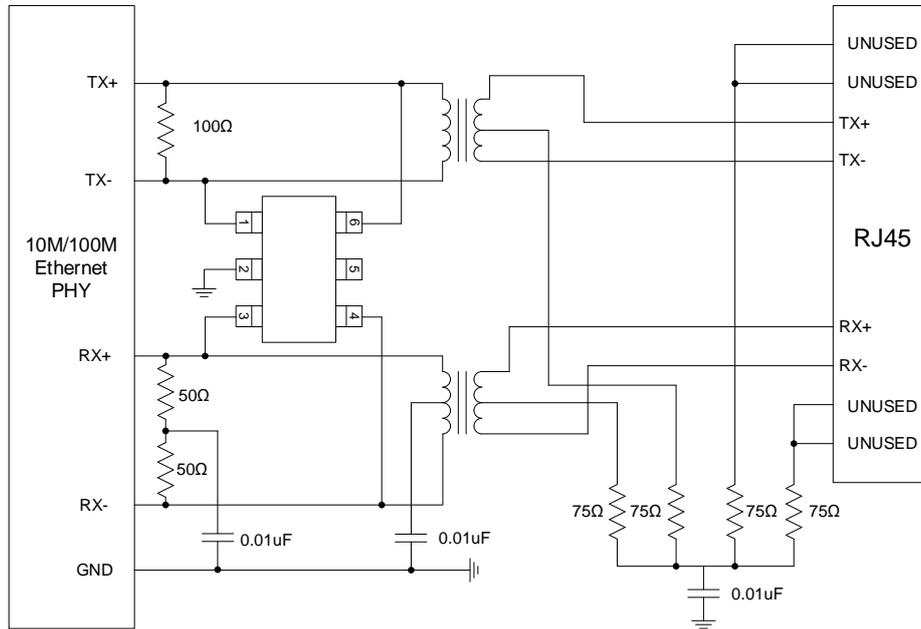


Layout Top View for SIM Port with SY205236ABC



Layout Top View for Digital Visual Interface (DVI) with SY205236ABC

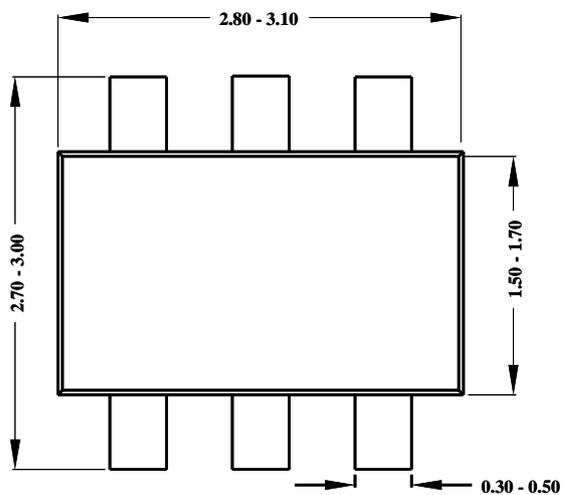
Application Information (continued)



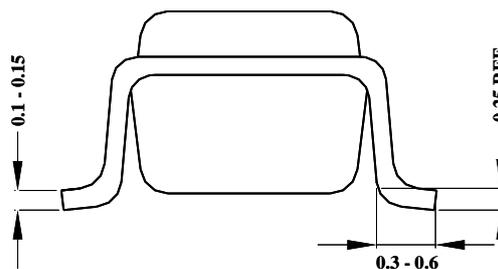
Differential and Common Mode Protection for 10M/100M Ethernet Interface with SY205236ABC

SOT23-6 Package Outline

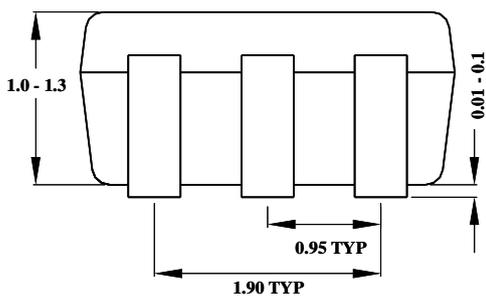
MSL-1 Level



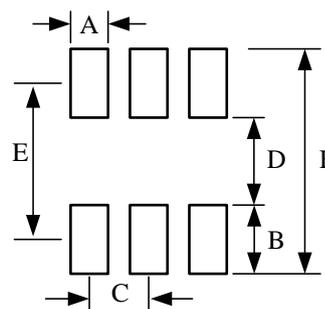
TOP VIEW



SIDE VIEW



SIDE VIEW



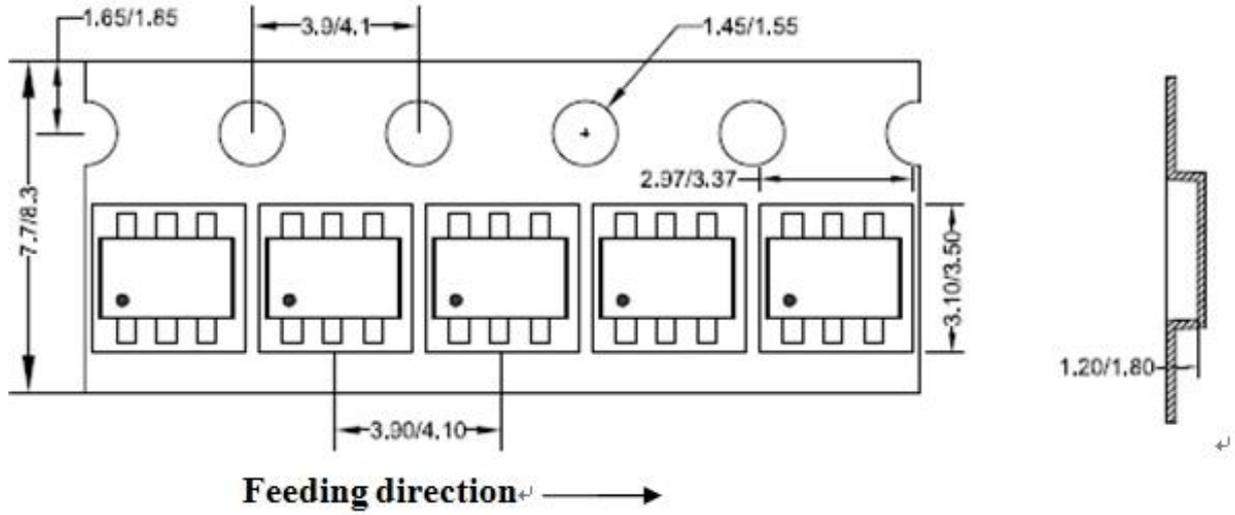
Recommended PCB Layout
(Reference only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

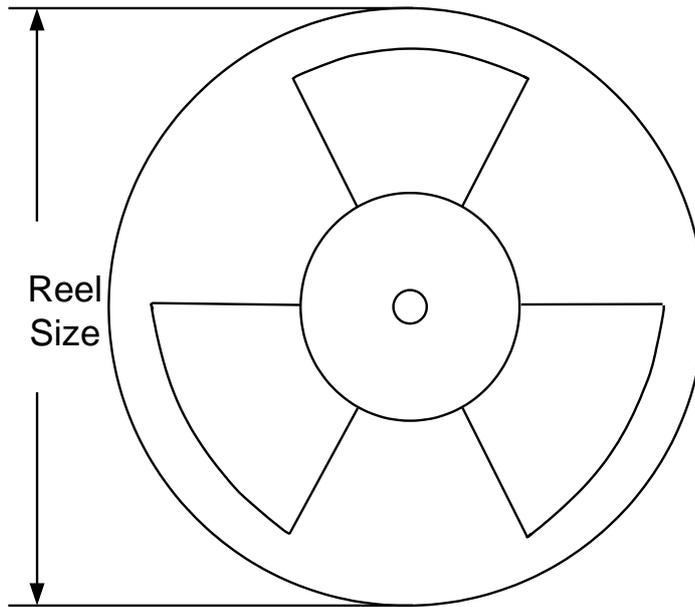
Symbol	Dimensions	
	Millimeters	Inches
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	1.40	0.055
E	2.50	0.098

Tape and Reel Specification

SOT23-6 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel(pcs)
SOT23-6	8	4	7"	3000



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	10/25/2016	Initial Release	
1.0	10/25/2017	Production Release	

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