SY20601

High Efficiency 3MHz, 0.6A Power Module

General Description

SY20601x is a 3MHz, 0.6A synchronous step-down converter module which integrates an inductor and a buck converter in one tiny package (2.0mm×1.5mm, H=1.0mm). It can operate over an input voltage range of 2.5V to 5.5V and integrates the main and synchronous switches with very low R_{DSON} to minimize the conduction loss.

Designing with SY20601x only requires selecting the input and output capacitors along with a resistor divider for configuring the output voltage for the adjustable version.

Applications

- Mobile Phones, Smart Phones
- Bluetooth Headsets
- WiMAX PDA, MID, UMPC
- Portable Game Consoles
- Digital Cameras, Camcorders

Features

- 2.5~5.5V Input Voltage Range
- Low RDS(ON) for Internal Switches (Top/Bottom) 230mΩ/150mΩ
- Integrates the inductor to minimize the external components and simplify the PCB Layout design
- Output Voltage:
  - SY20601: Output Voltage Adjustable
  - SY20601A: Fixed 1.2VOUT
  - SY20601B: Fixed 1.5VOUT
  - SY20601C: Fixed 1.8VOUT
  - SY20601D: Fixed 2.5VOUT
  - SY20601E: Fixed 3.3VOUT
- High switching frequency 3MHz minimizes the external components size
- Internal Soft-Start and Inrush current limits
- 100% Dropout Operation
- RoHS Compliant and Halogen Free
- Output Auto Discharge Function
- Compact Package: QFN2×1.5-8

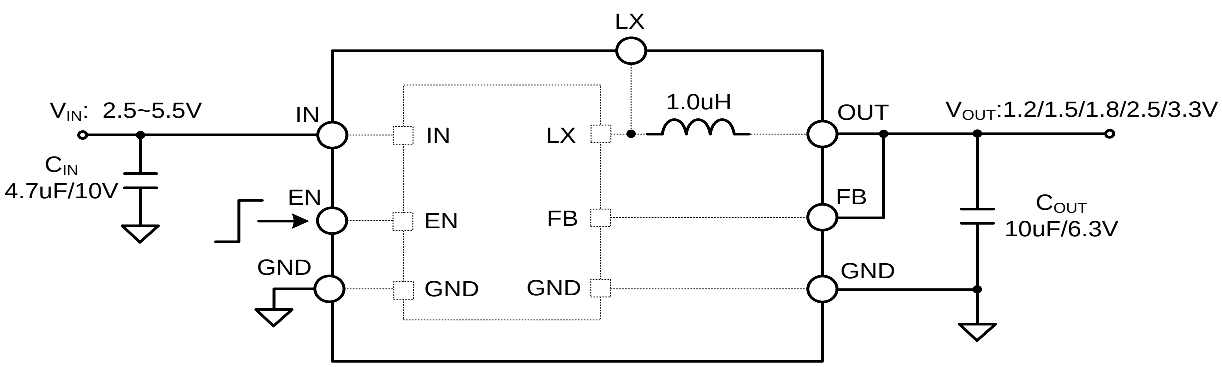


Figure1. Schematic Diagram (For SY20601A/B/C/D/E)

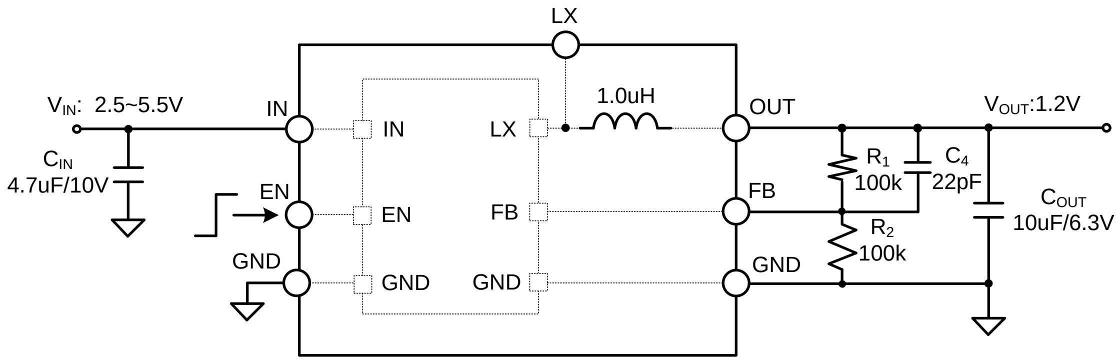


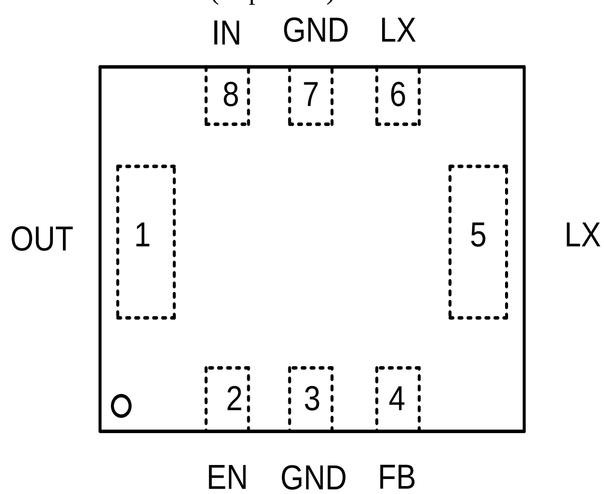
Figure2. Schematic Diagram (For SY20601)

Ordering Information

Ordering Part Number	Package	Top Mark
SY20601QUC	QFN2×1.5-8 RoHS Compliant and Halogen Free	**YG***xyz*
SY20601AQUC	QFN2×1.5-8 RoHS Compliant and Halogen Free	**UM***xyz*
SY20601BQUC	QFN2×1.5-8 RoHS Compliant and Halogen Free	**UN***xyz*
SY20601CQUC	QFN2×1.5-8 RoHS Compliant and Halogen Free	**TP***xyz*
SY20601DQUC	QFN2×1.5-8 RoHS Compliant and Halogen Free	**UO***xyz*
SY20601EQUC	QFN2×1.5-8 RoHS Compliant and Halogen Free	**UP***xyz*

x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin Name	Pin Number	Pin Description	
OUT	1	Output Pin. Decouple this pin to ground with at least 4.7uF ceramic cap.	
EN	2	Enable control. Pull high to turn on. Do not float.	
GND	3, 7	Ground pin.	
FB	4	SY20601	Output adjustable version. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT}=0.6\times(1+R_1/R_2)$.
		SY20601A/B/C/D/E	Fixed output version. Connect this pin to the output for the output voltage regulation.
LX	5,6	Built-in inductor node. Leave it floating.	
IN	8	Input pin. Decouple this pin to GND pin with at least a 4.7μF ceramic cap.	

Block Diagram

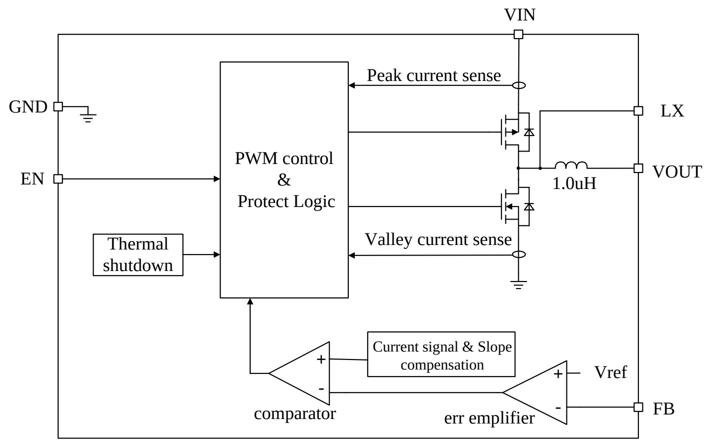


Figure 3. Block Diagram

Absolute Maximum Ratings (1)	Min	Max	Unit
LX		6	V
FB		IN + 0.6	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-65	150	

Thermal Information (2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		61	°C/W
θ_{JC} Junction-to-case Thermal Resistance		10	
P_D Power Dissipation T_A=25°C		410	mW

Recommended Operating Conditions (3)	Min	Max	Unit
IN	2.5	5.5	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	°C

Electrical Characteristics

Electrical Characteristics V_{IN} = 5V, V_{OUT} = 1.8V, C_{OUT} = 4.7µF, T_A = 25°C, unless otherwise specified						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input Voltage Range	V_{IN}		2.5		5.5	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		40		µA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	µA
Feedback Reference Voltage	V_{REF}	SY20601	0.588	0.6	0.612	V
Output Voltage	V_{OUT}	SY20601A	1.176	1.2	1.224	V
		SY20601B	1.47	1.5	1.53	V
		SY20601C	1.764	1.8	1.836	V
		SY20601D	2.45	2.5	2.55	V
		SY20601E	3.234	3.3	3.366	V
PFET R_{ON}	$R_{DS(ON),P}$			230		mΩ
NFET R_{ON}	$R_{DS(ON),N}$			150		mΩ
Inductance	L			1.0		uH
PFET Current Limit	I_{LIM}		1.3			A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				2.5	V
UVLO Hysteresis	V_{HYS}			0.1		V
Oscillator Frequency	f_{OSC}			3		MHz
Min ON Time				65		ns
Max Duty Cycle			100			%
Soft-start Time	t_{SS}			1		ms
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Output Discharge Resistor	R_{DSC}			120		Ω

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

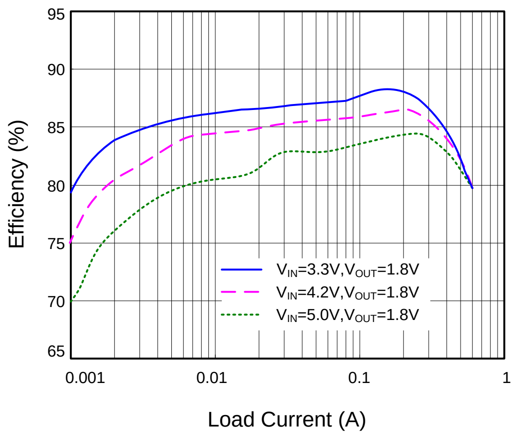
Note 2: θ_{JA} is measured in the natural convection on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

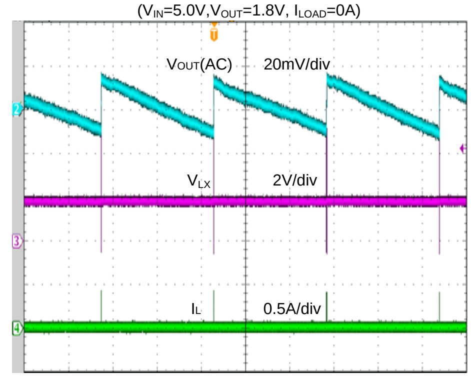
(SY20601C)

Efficiency vs. Load Current



Output Ripple

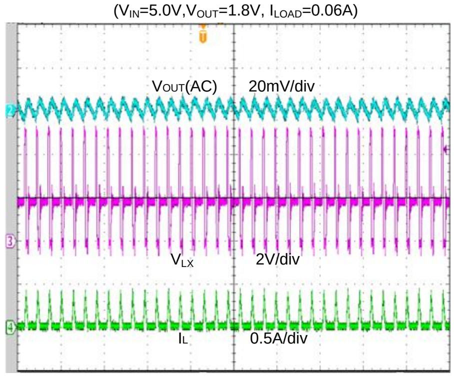
(V_{IN}=5.0V,V_{OUT}=1.8V, I_{LOAD}=0A)



Time (4ms/div)

Output Ripple

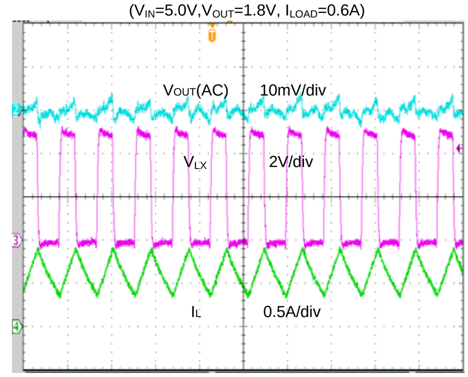
(V_{IN}=5.0V,V_{OUT}=1.8V, I_{LOAD}=0.06A)



Time (4μs/div)

Output Ripple

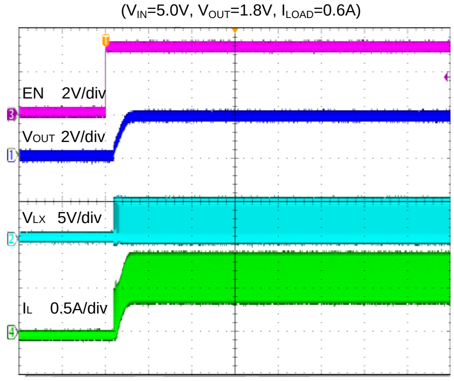
(V_{IN}=5.0V,V_{OUT}=1.8V, I_{LOAD}=0.6A)



Time (400ns/div)

Startup

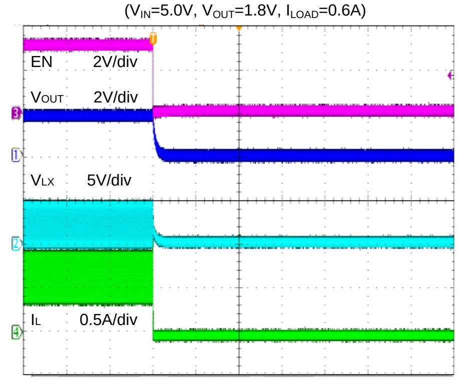
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.6A)



Time (2ms/div)

Shutdown

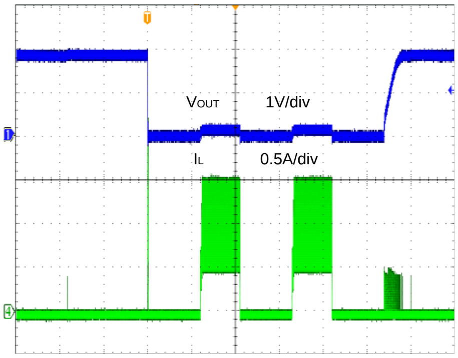
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.6A)



Time (200μs/div)

Short Circuit Protection

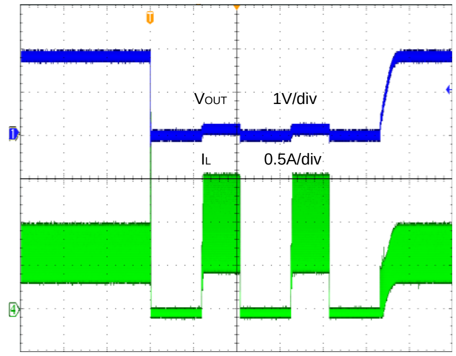
(V_{IN}=5.0V, V_{OUT}=1.8V, 0A to Short)



Time (2ms/div)

Short Circuit Protection

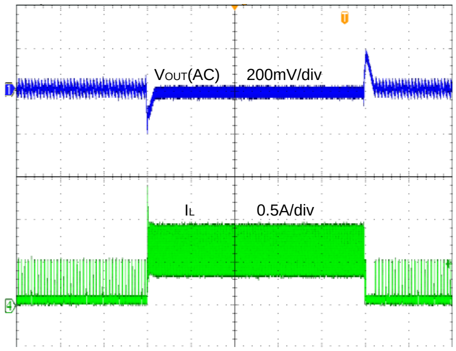
(V_{IN}=5.0V, V_{OUT}=1.8V, 0.6A to Short)



Time (2ms/div)

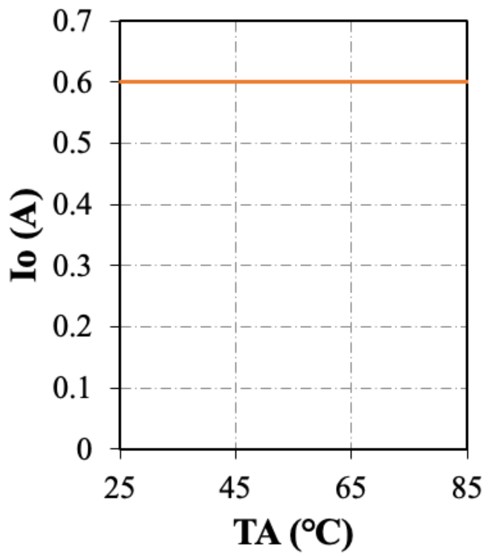
Load Transient

(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.06-0.6A)



Time (40μs/div)

Thermal Derating Curve
（VIN=5.5V, VOUT=3.3V, no air flow）



Note:

1）TA: Air temperature, measured 0.5 inch above module.

2）Based on a two-layer Silergy evaluation board and using natural convection.

3）The IC case temperature is below 115°C under the TD curve.

4）For any other application conditions, keep the the maximum module case temperature below 115°C.

Application Information

The circuit around the SY20601 requires selecting the input and output capacitors to address and meet the system level requirements. In addition, the adjustable version uses two resistors for configuring the required output voltage. Background information on component selection is outlined below.

Input Capacitor C_{IN}

A ceramic capacitor whose capacitance is greater than 4.7µF is recommended. The component should be placed as close as possible to the module, while also minimizing the loop area formed by C_{IN} and the IN/GND pins. When selecting an input capacitor ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires it is recommended adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1\text{-}D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications a single 4.7 uF X5R capacitor is sufficient.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, it is recommended using a X7R or better grade ceramic capacitor with 6V rating and a capacitane that is greater than 10uF.

For applications where the design must meet strigent ripple requirements the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = (0.6A I_{OUT} x 40%) = 0.24 A and using a 10µF ceramic capacitor with an ESR of ~10mΩ.

$V_{RIPPLE,\ ESR}$ = 0.24A x 10mΩ = 2.4 mV

$V_{RIPPLE,\ CAP}$ = 0.24A/(8x10x3MHz) = 1 mV

The capacitive ripple might be higher because for ceramic capacitors the effective capacitance decreases with the voltage across the terminals. The voltage derating is usually included in the capacitor datasheet as a chart and the ripple can be re-calculated taking the target output voltage into account.

Load Transient Considerations:

SY20601/A/B/C/D/E integrates the compensation components to achieve good stability and fast transient response.

During transient conditions, the output voltage overshoot and undeshoot are influenced by the capacitor selection.

Bench test results based on using a suggested value of 10uF for the output capacitor are shown in the “Typical Performance Characteristics” section.

In the case of the adjustable output voltage option, adding a feed-forward capacitor can help improve the transient response. A value between 10 pF and 22 pF is recommended.

Layout

The following considerations have to be followed for an optimal layout design:

1) Place CIN and COUT close to the module.

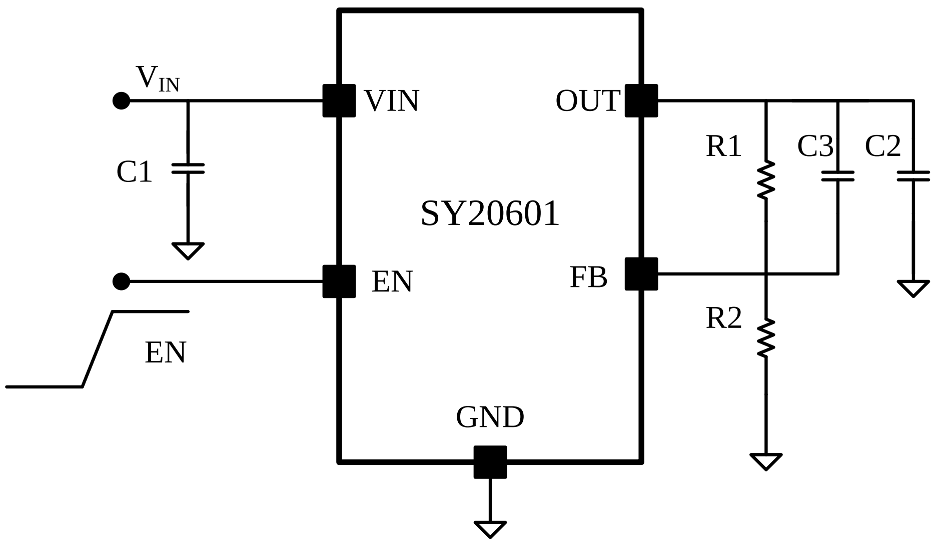
2) Use a large copper area connected to GND for optimal thermal performance. If cost and other design considerations allow it, a ground plane is highly desirable.

2) C_{IN} must be close to IN and GND pins. The loop area formed by C_{IN} and GND must be minimized.

3) Use a short trace to connect the LX pins together. It is strongly recommended to reduce the LX routing area to avoid potential noise problems.

4) Route the trace connecting to the FB pin far away from the LX node to reduce noise coupling.

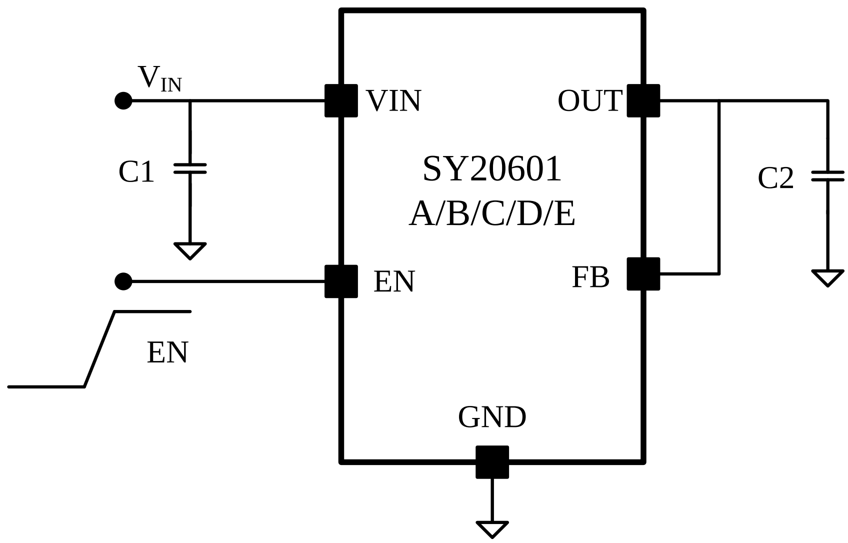
Application Circuit -Adjustable Output Voltage



Bom list

Designator	Description	Part Number	Manufacturer
C1	4.7uF/10V,0402,X5R	C1005X5R1A475M	TDK
C2	10uF/6.3V,0603,X5R	C1608X5R1A106M	TDK
C3	10pF/50V,0603,X5R	C1608C0G1H10D	TDK
R1	100kohm, 1%, 0603	RC0603FR-07100KL	Yageo
R2	49.9kohm, 1%, 0603, set 1.8V	RC0603FR-0749K9L	Yageo
	22.1kohm, 1%, 0603, set 3.3V	RC0603FR-0722K1L	Yageo

Application Circuit -Fixed Output Voltage



Bom list

Designator	Description	Part Number	Manufacturer
C1	4.7uF/10V,0402,X5R	C1005X5R1A475M	TDK
C2	10uF/6.3V,0603,X5R	C1608X5R1A106M	TDK

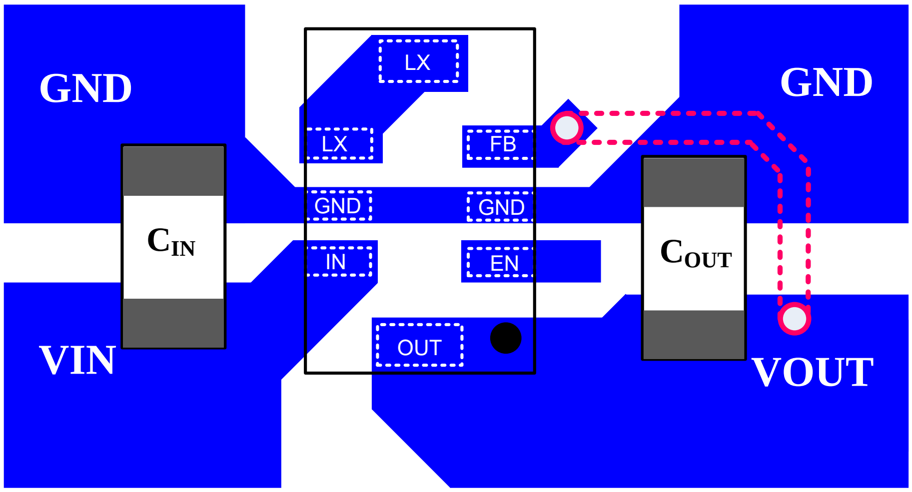
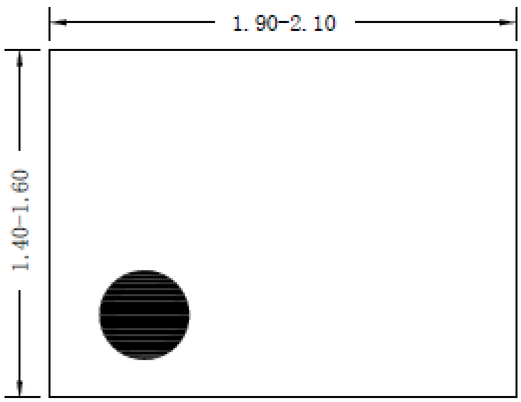
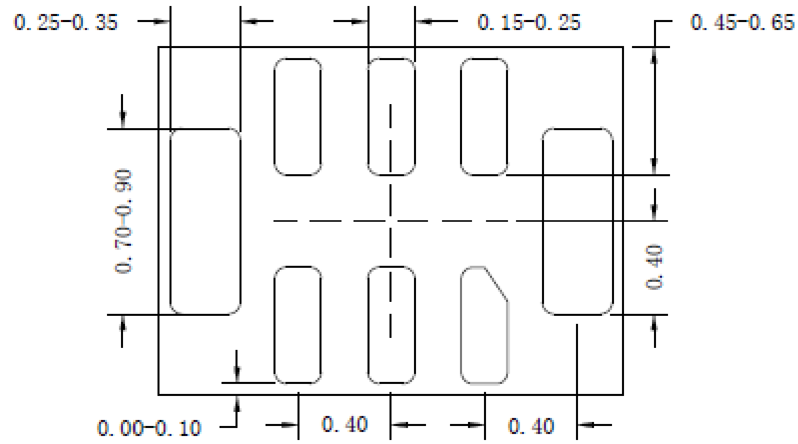


Figure4. PCB Layout Suggestion

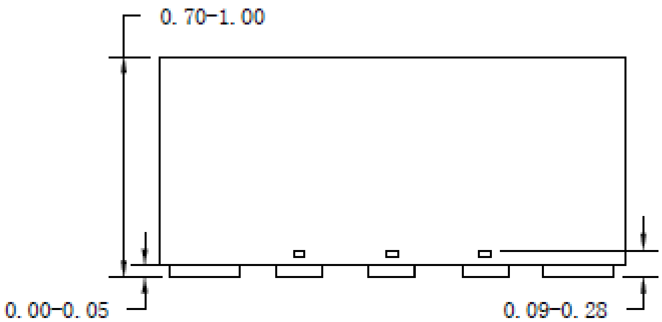
QFN2×1.5-8 Package Outline Drawing



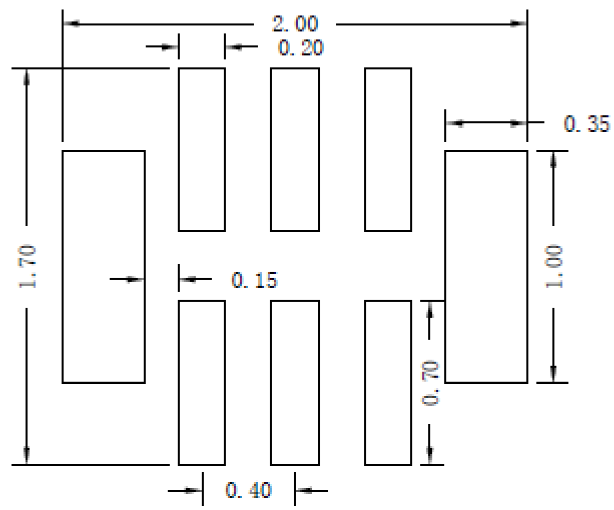
Top View



Bottom View



Side View

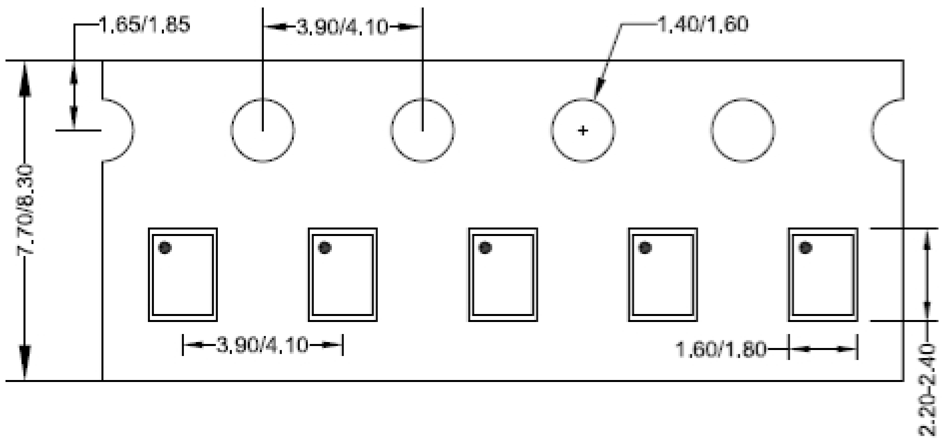


Recommended PCB layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

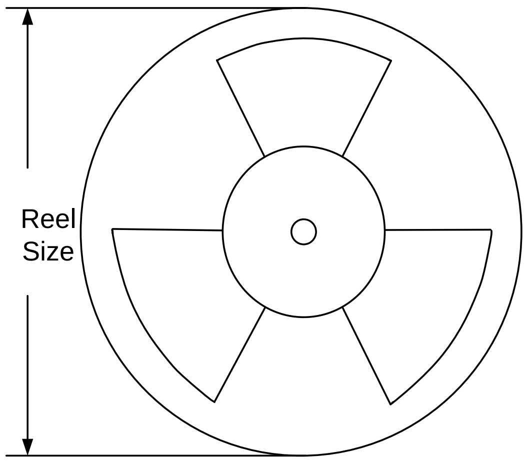
Taping & Reel Specification

1. QFN2×1.5 Taping Orientation



Feeding direction →

2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2×1.5	8	4	7	400	160	3000

3. Others: NA

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