SY20624

High Efficiency 3MHz, 4A Inductor Built-in Synchronous Step Down Regulator

General Description

SY20624 is a 3MHz, 4A synchronous step-down regulator which integrates an inductor and a control IC in a tiny package (3.0mm×3.0mm, H=2.0mm). It operates over a wide input voltage range from 2.75V to 5.5V. It integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Applications

- Mobile Phone, Smart Phone
- Bluetooth Headsets
- WiMAX PDA, MID, UMPC
- Portable Game Console
- Digital Camera, Camcorder

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 35/15 mΩ
- 2.75-5.5V Input Voltage Range
- 3 MHz Switching Frequency Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 4A Continuous Output Current Capability
- Shutdown Mode Draws<0.1μA Supply Current
- 100% Dropout Operation
- Power Good Indicator
- OCP/UVLO/OTP Protections
- RoHS Compliant and Halogen Free
- Compact Package: QFN3x3-10

Typical Applications

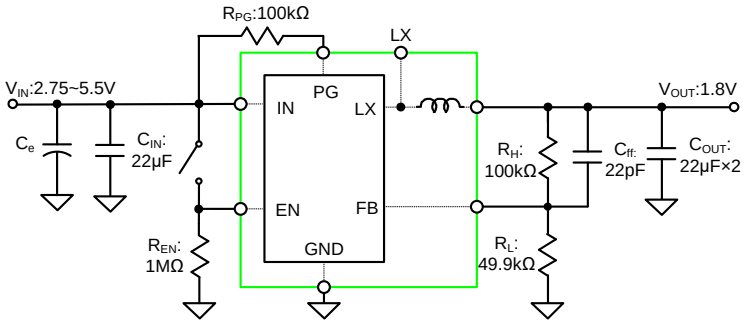


Figure1. Schematic Diagram

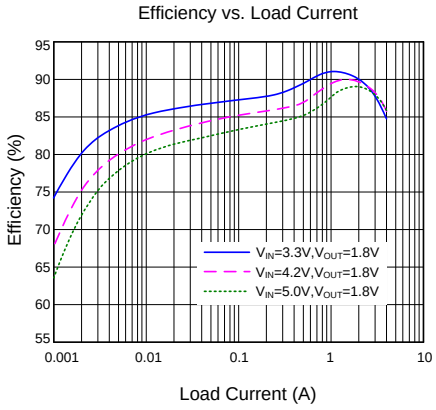


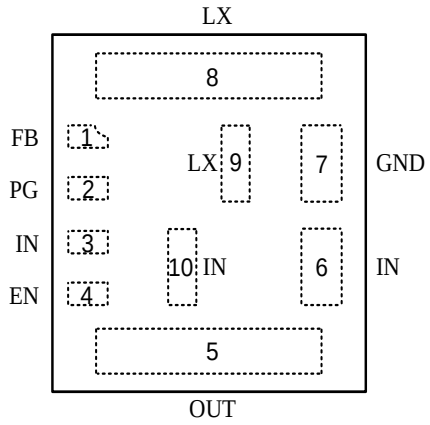
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY20624QNC	QFN3x3-10 RoHS Compliant and Halogen Free	**BCY*xyz***

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin Number	Description
FB	1	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
PG	2	Power good indicator, open drain. When the output voltage exceeds 90% of the regulation point, it becomes high; low otherwise.
IN	3,6,10	Power input pin.
EN	4	Enable control. Pull high to turn on. Do not leave it floating.
OUT	5	Output pin. Decouple this pin to GND with at least a 40μF ceramic capacitor.
GND	7	Ground pin.
LX	8,9	Built-in inductor node. Leave it floating.

Block Diagram

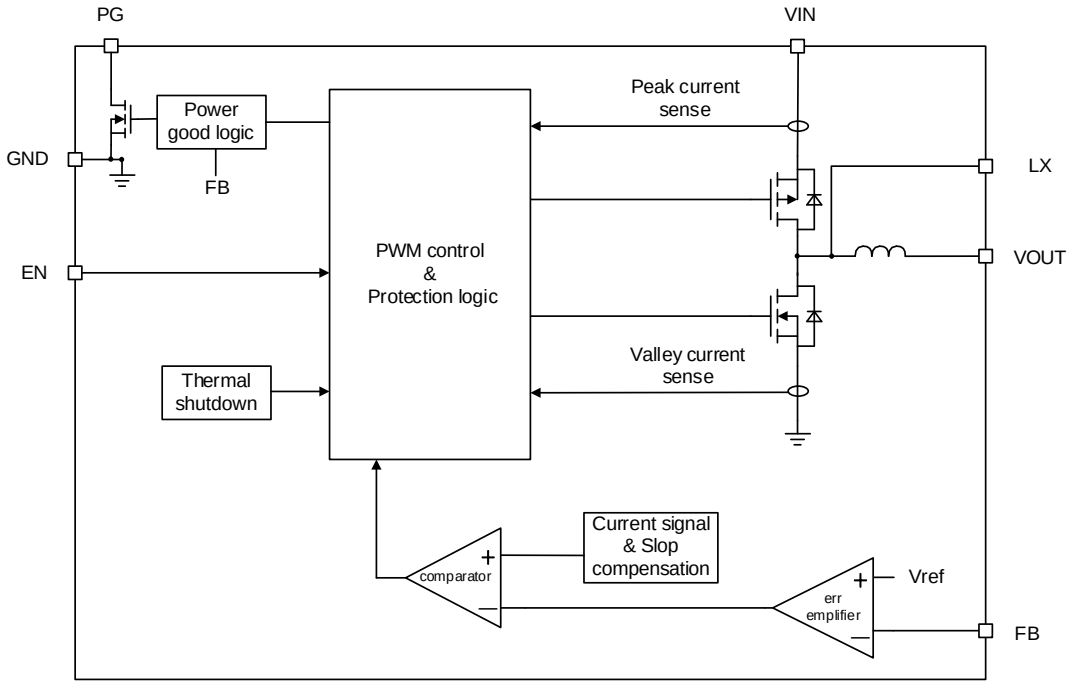


Figure 3. Block Diagram

Absolute Maximum Ratings(1)	Min	Max	Unit
IN, LX		6	V
All Other Pins		IN + 0.5	
Junction Temperature Range		150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-65	150	

Thermal Information (2)	Min	Max	Unit
Package Thermal Resistance (Note 2)			°C/W
θ_{JA} Junction-to-ambient Thermal Resistance		50	
θ_{JC} Junction-to-case Thermal Resistance		5	
P_D Power Dissipation T_A=25°C		2	W

Recommended Operating Conditions (3)	Min	Max	Unit
IN	2.75	5.5	V
Junction Temperature Range	-40	125	°C
Ambient Temperature Range	-40	85	

Electrical Characteristics

Electrical Characteristics V_{IN} = 5V, V_{OUT} = 2.5V, C_{OUT} = 22µFx2, T_A = 25°C, I_{OUT} = 1A unless otherwise specified							
Parameter		**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input	Voltage	V_{IN}		2.75		5.5	V
	UVLO, rising	$V_{IN,UVLO}$				2.75	V
	UVLO, Hysteresis	$V_{IN,HYS}$			300		mV
	Shutdown Current	I_{SHDN}	V_{EN}=0V		0.1	1	µA
	Quiescent Current	I_Q	I_{OUT}=0, EN=1, FB=105%×V_{REF}		68		µA
Output	Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
	NFET RDS(ON)	$R_{DS(ON)N}$			15		mΩ
	PFET RDS(ON)	$R_{DS(ON)P}$			35		mΩ
	Internal Soft-start Time	t_{SS}			0.8		ms
General Specifications	Oscillator Frequency	f_{OSC}			3		MHz
	Thermal Shutdown Temperature	T_{SD}			150		°C
	Thermal Shutdown Hysteresis	T_{HYS}			15		°C
	LX Node Discharge Resistor	R_{DSH}			50		Ω
	Input Peak Current Limit	I_{LIM}		5			A
Signal Specifications	PGOOD Under Voltage Threshold	$V_{FB,LV}$			0.54		V
	Short Circuit Protection Threshold	V_{SCP}			0.25		V
	Min ON Time				60		ns
	Max Duty Cycle			100			%
	EN Rising Threshold	V_{ENH}		1.2			V
	EN Falling Threshold	V_{ENL}				0.4	V

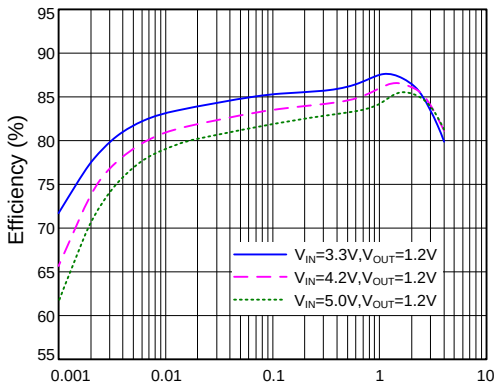
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of QFN3x3-10 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

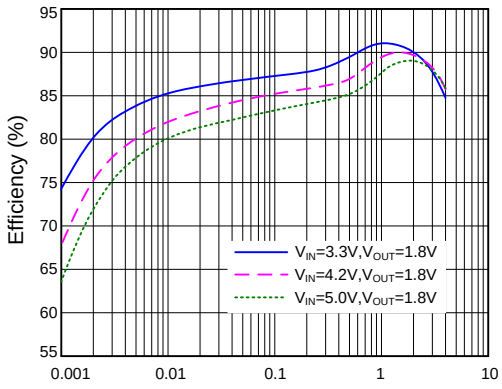
Typical Performance Characteristics

Efficiency vs. Load Current



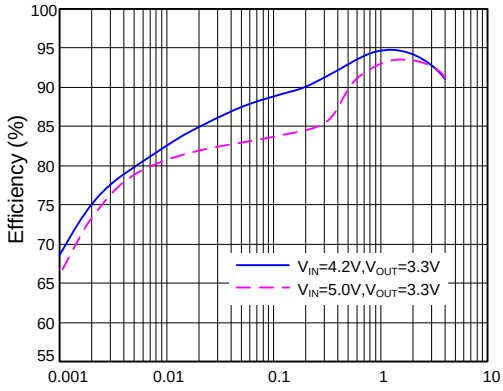
Load Current (A)

Efficiency vs. Load Current



Load Current (A)

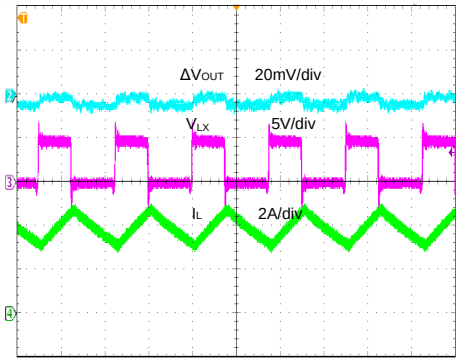
Efficiency vs. Load Current



Load Current (A)

Output Ripple

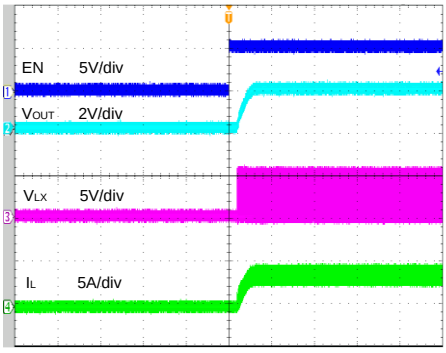
(V_{IN}=5.0V,V_{OUT}=1.8V, I_{OUT}=4.0A)



Time (200ns/div)

Startup From Enable

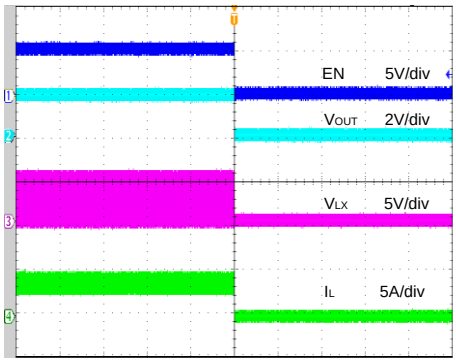
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=4.0A)



Time (2ms/div)

Shutdown from Enable

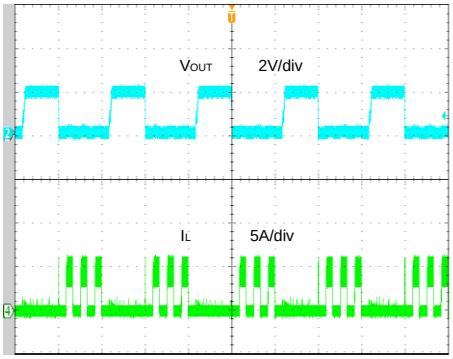
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=4.0A)



Time (4ms/div)

Short Circuit Protection

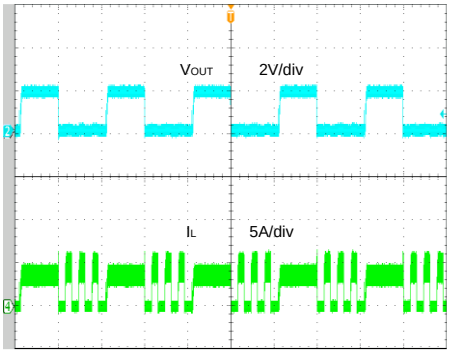
(V_{IN}=5.0V, V_{OUT}=1.8V, 0A to Short)



Time (20ms/div)

Short Circuit Protection

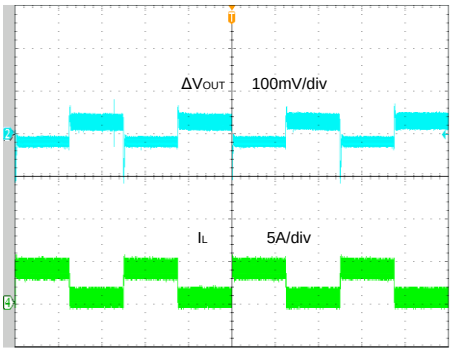
(V_{IN}=5.0V, V_{OUT}=1.8V, 4.0A to Short)



Time (20ms/div)

Load Transient

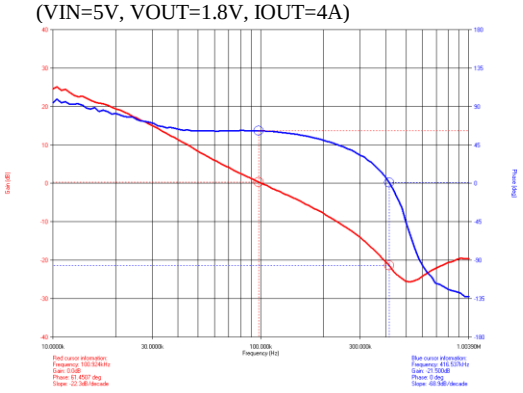
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=0.4 ~ 4.0A)



Time (400μs/div)

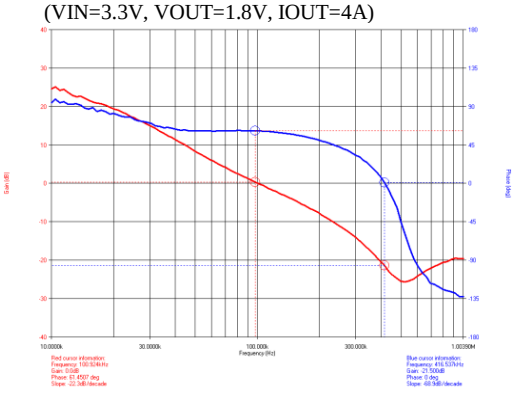
Bode Plot

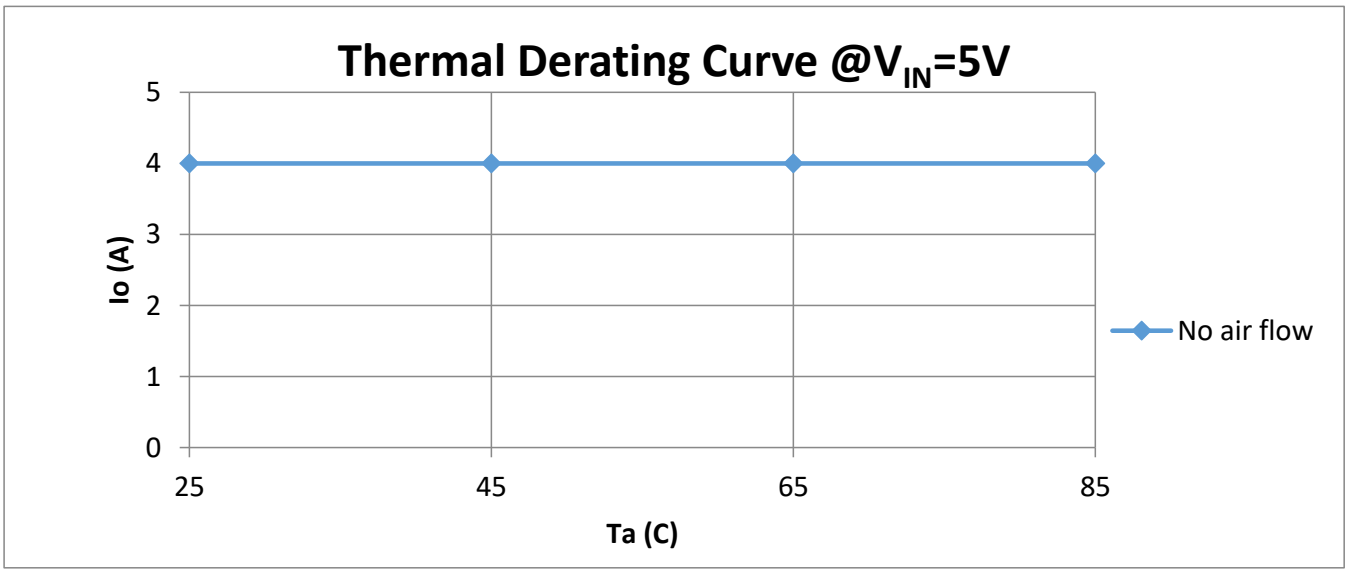
(VIN=5V, VOUT=1.8V, IOUT=4A)



Bode Plot

(VIN=3.3V, VOUT=1.8V, IOUT=4A)





Notes:

1) T_A: Air temperature, 0.5 inch above IC.
2) Based on a four-layer Silergy Evaluation Board in the natural convection.
3) The inductor temperature is not beyond 115℃ under this TD curve.
4) For customer's specific application, the recommended inductor temperature limitation is 115℃.

Operation

SY20624 is a 3MHz, 4A synchronous step-down regulator which integrates an inductor and a control IC in a tiny package (3.0mm × 3.0mm, H=2.0mm). It operates over a wide input voltage range from 2.75V to 5.5V. It integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Applications Information

Because of the high integration in the SY20624, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT} and the feedback resistors (R_H and R_L) need to be selected for the targeted applications.

Feedback Resistor Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_H and R_L. A value between 100kΩ and 1MΩ is highly recommended for both resistors. If R_L=120kΩ is chosen, then R_H can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.6V) \times R_L}{0.6V}$$

Input Capacitor C_{IN}

A typical X7R or better grade ceramic capacitor larger than 10µF capacitance is recommended. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the IN/GND pins.

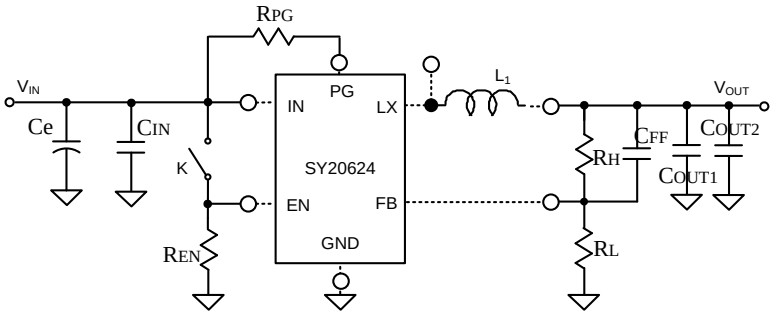
Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X7R or better grade ceramic capacitor with 6V rating and greater than 40uF capacitance.

Load Transient Considerations

SY20624 integrates the compensation components to achieve good stability and fast transient response. In some applications, adding a 22pF ceramic capacitor in parallel with R_H may further speed up the load transient response and is thus recommended for applications with large load transient step requirements.

Application Schematic (V_{OUT}=1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
Ce	470µF/16V Electrolytic Cap		
C_{IN}	22µF/6.3V/X5R, 0805	C2012X5R0J226M	TDK
C_{OUT1}, C_{OUT2}	22µF/6.3V/X5R, 0805	C2012X5R0J226M	TDK
C_{FF}	22pF/50V/X5R, 0805	C1608C0G1H22D	TDK
R_H	100kΩ, 0603, 1%		
R_L	49.9kΩ, 0603, 1%		
R_{EN}	1MΩ,0603		
R_{PG}	100kΩ, 0603		

Recommend Table for Typical Applications

V_{OUT}(V)	R_L (KΩ)	R_H (KΩ)	C_{FF} (pF)
0.6	0	100	22
1.2	100	100	22
1.8	50	100	22
3.3	22.1	100	22

Layout Design

For the minimum noise problem, the following components should be placed close to the IC: C_{IN} and C_{OUT}.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.

2) C_{IN} must be close to the IN and GND pins. The loop area formed by the C_{IN} and GND must be minimized.

3) Connect the LX pins together to reduce the inductor DCR. It is strongly recommended to reduce the LX routing area to avoid the potential noise problem.

4) The trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to the FB pin.

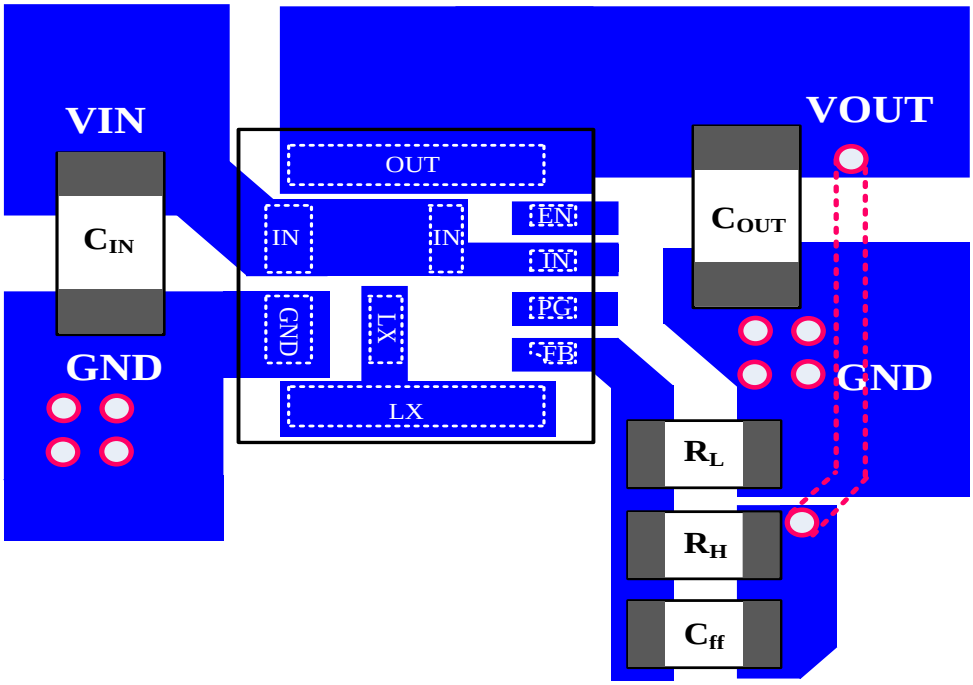
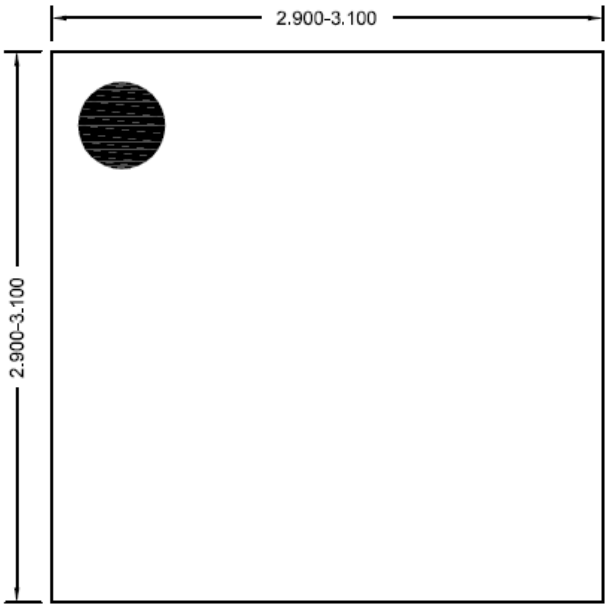
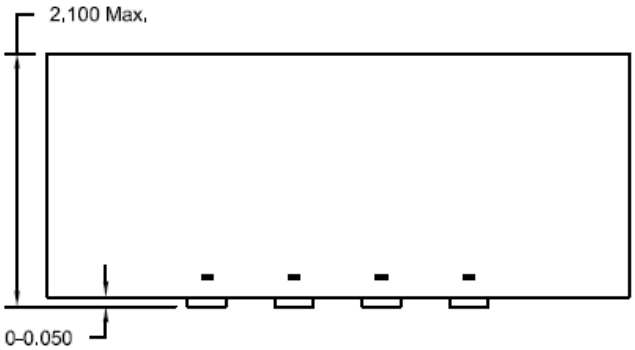


Figure4. PCB Layout Suggestion

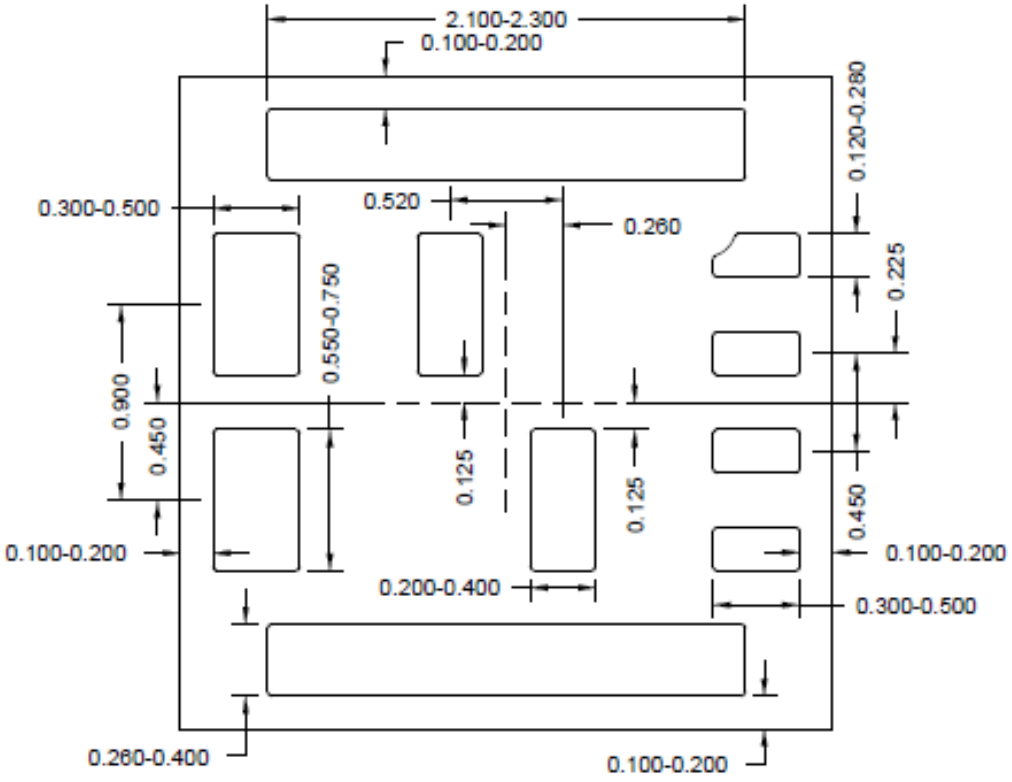
QFN3x3-10 Package Outline Drawing



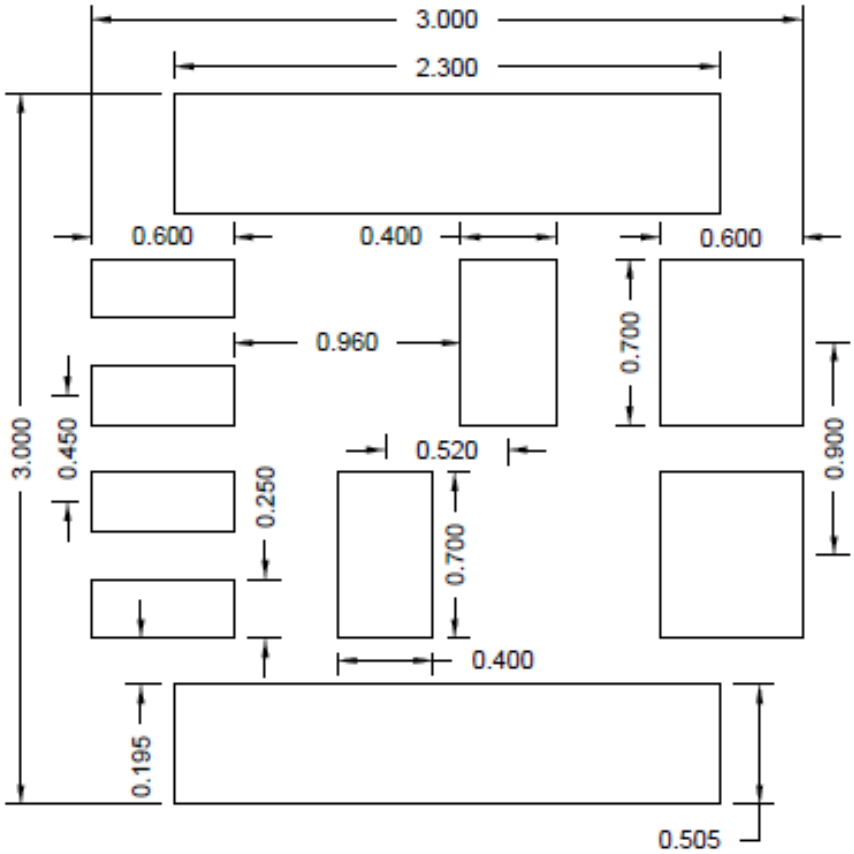
Top View



Side View



Bottom View

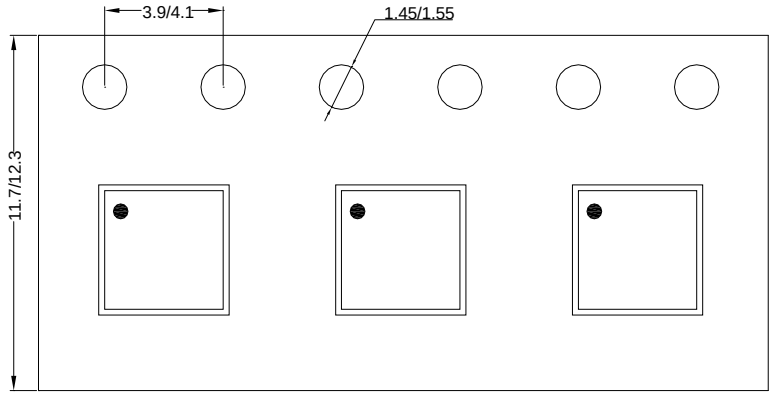


Recommended PCB layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr**.**

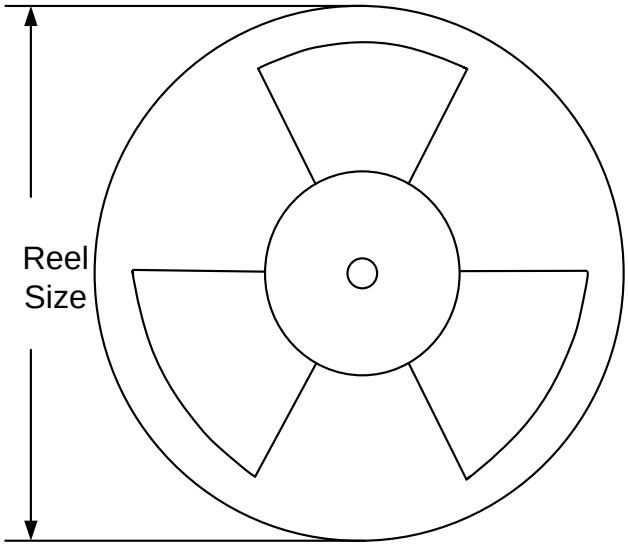
Taping & Reel Specification

1. QFN3×3 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	3000

3. Others: NA

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