SY26901

High efficiency, 1.5A, Synchronous Buck-boost DC/DC converter

General Description

The SY26901 is a wide input voltage range, high efficiency, fixed frequency buck-boost converter that operates from the input voltage above, below or equal to the output voltage. It provides a power supply for system powered by either a two-cell or three-cell alkaline, Ni-Cd or Ni-MH battery, or a one-cell Li-Ion or Li-polymer battery.

The SY26901 can support for 1.5A load current capability. It is based on a fixed frequency, pulse-width-modulation(PWM) controller using synchronous rectification to obtain maximum efficiency. The output voltage and compensation circuit can be programmed using external resistors and capacitors network. During shutdown, the load is disconnected from the battery. The device is packaged in tight MQFN2×3-13.

Features

- Fixed frequency operation with battery voltage above, below or equal to the output
- Four internal power switches to form true 4- switches buck-boost with single inductor.
- Seamless buck-boost transition.
- 2.65V to 5.5V Input Voltage Range.
- 1.5A continuous output current capability
- Output disconnect at shutdown.
- Power good indicator.
- Compact package: MQFN2×3-13
- Built in thermal shut down protection, hard short protection.

Applications

- Palmtop Computers
- Handheld Instruments
- MP3/MP4 Players
- Digital Cameras/Camcorders
- Personal Medical Products
- High Power LED's
- All two-cell and three-cell alkaline, Ni-Cd or Ni-MH or signal-cell Li battery powered products
- Optical communication module

Typical Applications

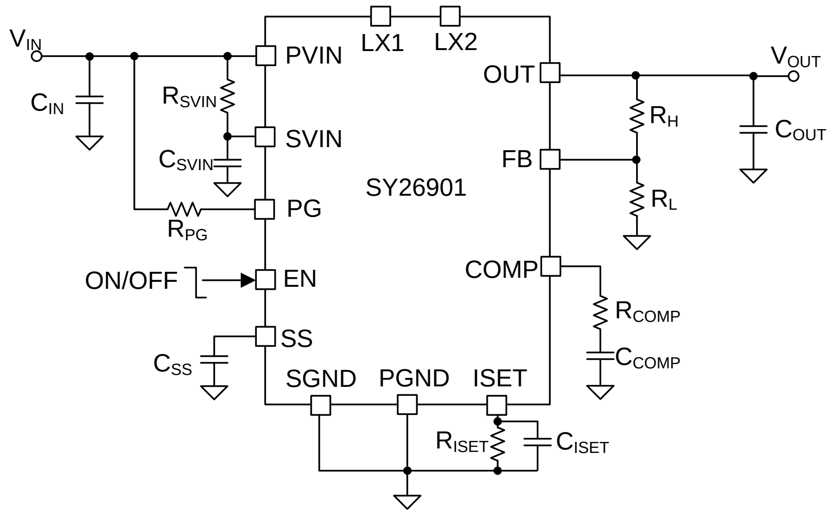


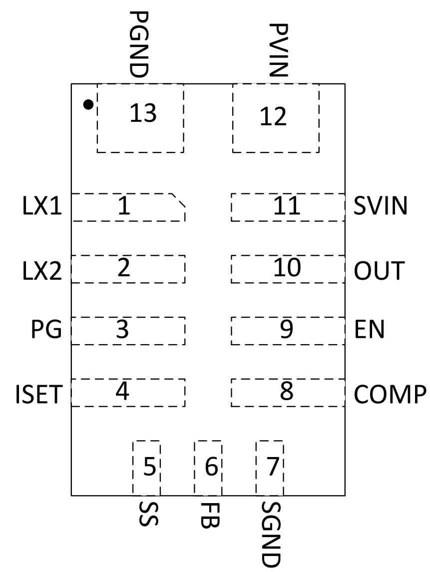
Figure1. Schematic Diagram

Ordering Information

Ordering Part Number	Package type	Top Mark
SY26901ACM	MQFN2×3-13 RoHS Compliant and Halogen Free	**EEW*xyz***

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin Number	Pin Description
LX1	1	Switching node, leave it floating.
LX2	2	Switching node, leave it floating.
PG	3	Power good indicator. Recommend to connect 100kΩ Resistor to PVIN.
ISET	4	Tie to ground for forced PWM operation. Set R_{ISET}=250kΩ, C_{ISET}=10nF for PFM operation.
SS	5	Connect this pin to a soft-start capacitor to program soft-start time. Connect at least 4.7nF ceramic cap between this pin and GND.
FB	6	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage.
SGND	7	Signal ground pin. Tie to PGND.
COMP	8	External compensation for voltage loop, Connect a 1nF ceramic capacitor and 15K resistor from COMP to PGND.
EN	9	Enable control. Pull high to turn on. Internal integrated with 1MΩ pull down Resistor.
OUT	10	Output of the synchronous rectifier. Decouple this pin to GND with at least 22uF ceramic cap. Minimize the loop area formed by output cap, OUT pin and GND paddles.
SVIN	11	Signal power input pin. Decouple this pin to GND with at least 1uF ceramic cap. Connect this pin to PVIN with 10Ω resistor.
PVIN	12	Power input pin. Decouple this pin to GND with at least 22uF ceramic cap. Minimize the loop area formed by input cap, PVIN pin and GND paddles.
PGND	13	Power ground pin.

Block diagram

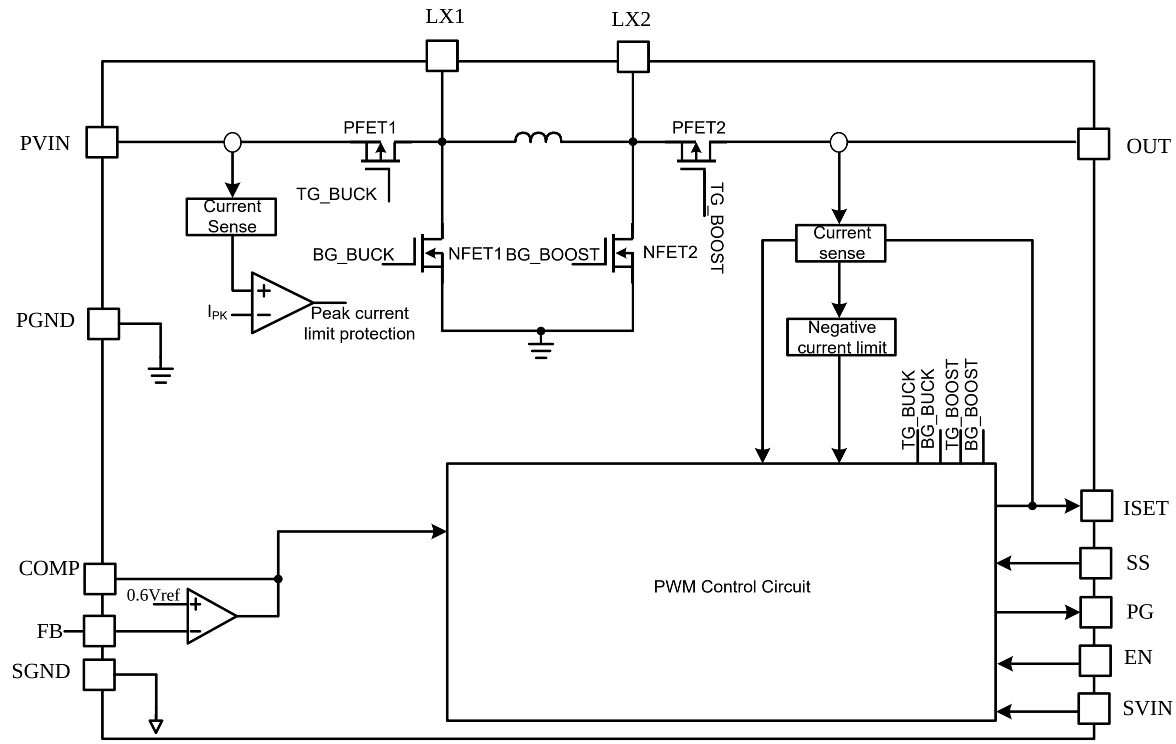


Figure 2. Block Diagram

Absolute Maximum Ratings (1)	Min	Max	Unit
OUT		4	V
All Other Pins		6	
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-55	125	

Thermal Information (2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		39	°C/W
P_D Power Dissipation T_A=25°C		2.3	W

Recommended Operating Conditions (3)	Min	Max	Unit
IN	2.65	5.5	V
Output Voltage		3.3	
Output Current	0	1.5	A
Junction Temperature	-40	125	°C

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Electrical Characteristics V_{IN} = 3.3V, V_{OUT} =3.3V, I_{OUT} = 0.7A, C_{IN}=22*2μF, C_{OUT} = 22*4μF, R_{COMP}=15kΩ, C_{COMP}=1nF, FCCM mode, T_A= 25°C, unless otherwise specified						
Input Specifications						
Input Voltage Range	V_{IN}		2.65		5.5	V
Input UVLO Rising Threshold			2.2	2.5	2.6	V
UVLO hysteresis				0.25		V
Input Current with No Load		V_{IN}=3.3V, I_O=0A, EN=high		9		mA
Shutdown current		EN=low		0.1	1	uA
Output Specifications						
Feedback reference voltage	V_{FB}		0.591	0.6	0.609	V
Load Regulation		V_{IN}=3.3V, T_A=25°C, I_O=0 to 1A		10		mV
Line Regulation		V_{IN}=2.65-5.5V, T_A=25°C, I_O=0.7A (Vo@Vinmax-Vo@Vinmin)/Vo@Vinnom		1		%
Temperature Regulation		V_{IN}=3.3V, T_A=-40°C to 85°C, I_O=0.7A	-5		5	%
General Specifications						
Switching Frequency	F_{sw}		0.75	1	1.15	MHz
Output Voltage Over Protection				125		%
Thermal Shutdown Temperature		OTP Mode: Auto Recovery		150		°C
Thermal Shutdown Hysteresis				15		°C
Min Duty Cycle(Note 4)		Boost & Buck		10		%
Max Duty Cycle (Note 4)		Boost & Buck		90		%
Control and Indicator Signals						
EN pin logic high threshold (rising)			1.5			V
EN pin logic low threshold (falling)					0.4	V
SS pin source current	I_{SS}	Soft-start time: tss=(0.7V/Iss)*Css	3	4.4	6	uA
Power Good Deasserts Threshold		V_{FB} falling, PG from high to low		0.48		V
		V_{FB} rising, PG from high to low		0.72		

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

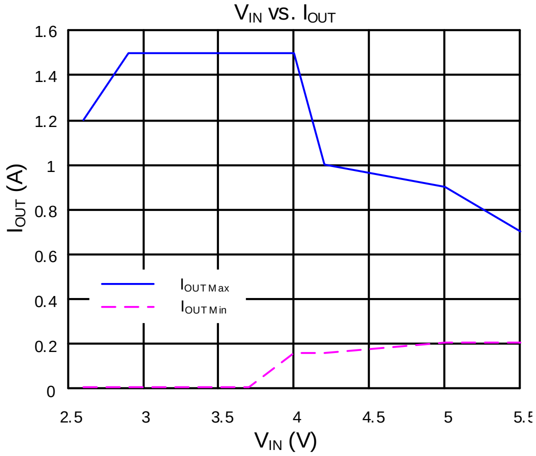
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: The values are guaranteed by design.

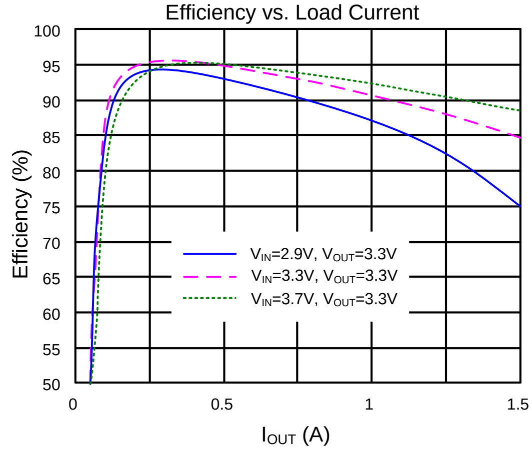
Typical Performance Characteristics

(V_{OUT}=3.3V, C_{OUT} = 4×22μF, T_A = 25°C, FCCM mode, resistor tolerance is ±1%, unless otherwise specified)

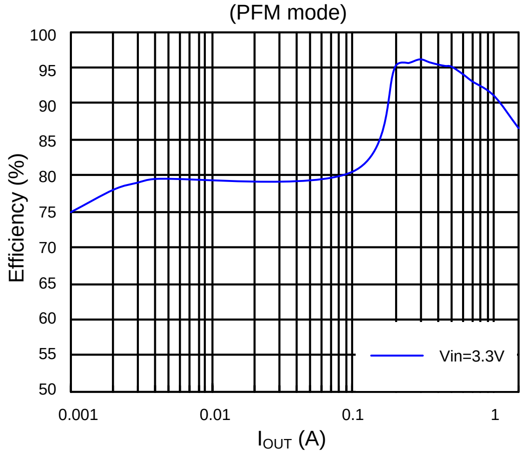
V_{IN} vs. I_{OUT}



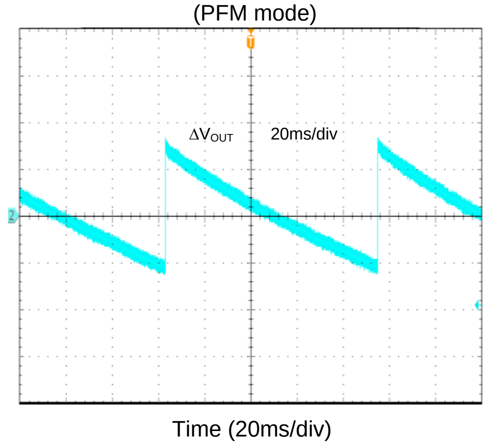
Efficiency vs. Load Current



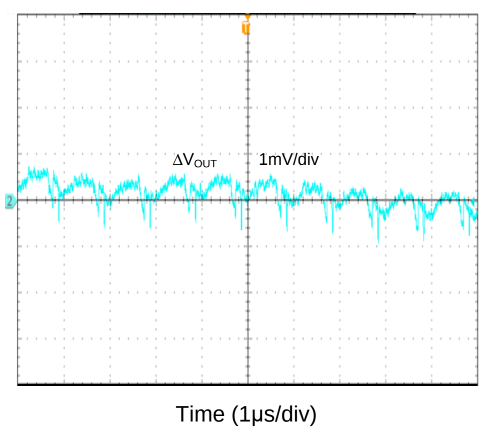
Efficiency vs. Output Current
(PFM mode)



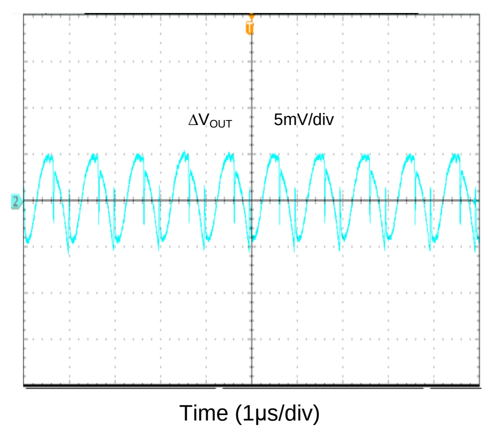
Output Ripple
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=0A)
(PFM mode)



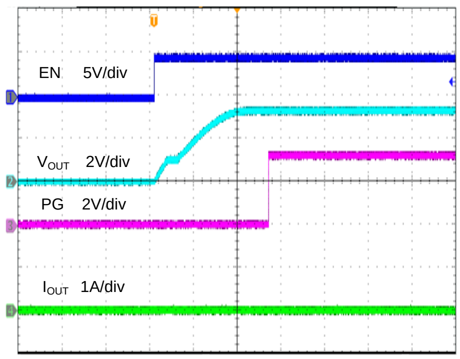
Output Ripple
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=0A)



Output Ripple
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=1.5A)

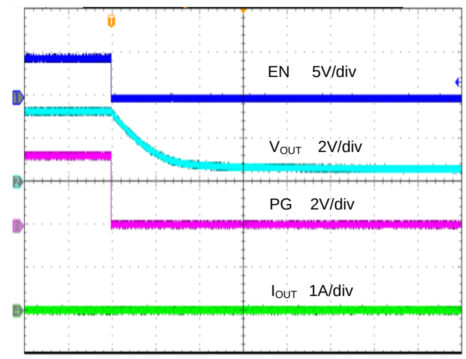


Startup from EN
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=0A)



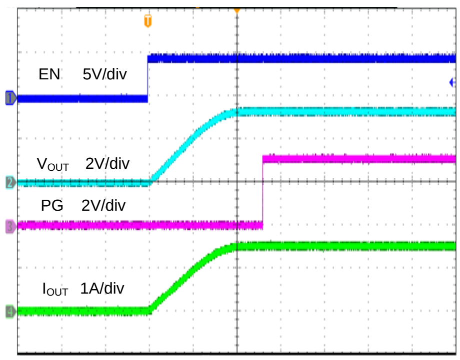
Time (10ms/div)

Shutdown from EN
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=0A)



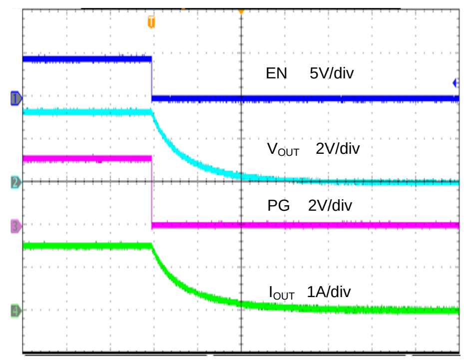
Time (4ms/div)

Startup from EN
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=1.5A)



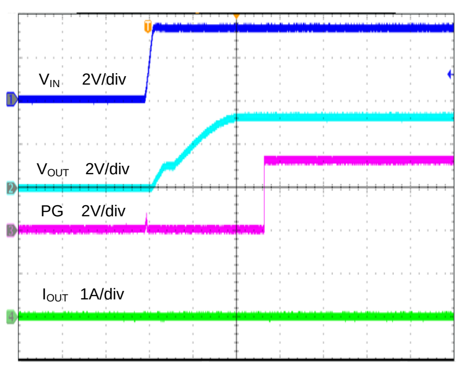
Time (10ms/div)

Shutdown from EN
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=1.5A)



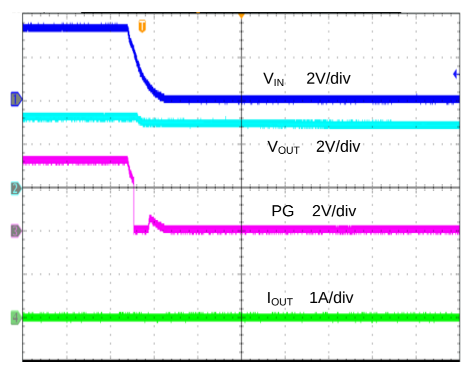
Time (200μs/div)

Startup from V_{IN}
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=0A)



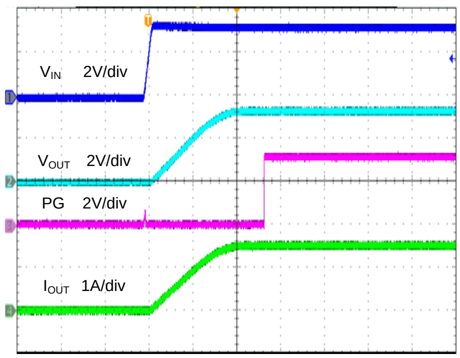
Time (10ms/div)

Shutdown from V_{IN}
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=0A)



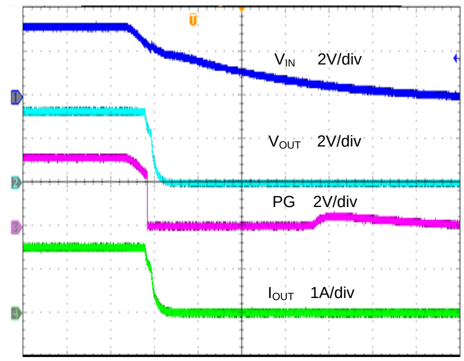
Time (20ms/div)

Startup from V_{IN}
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=1.5A)



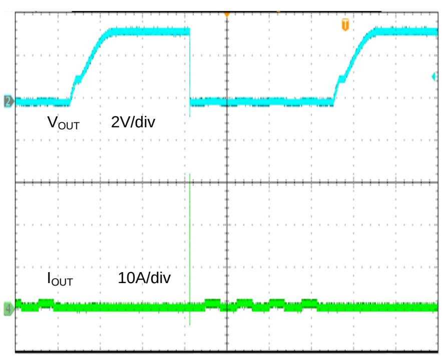
Time (10ms/div)

Shutdown from V_{IN}
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=1.5A)



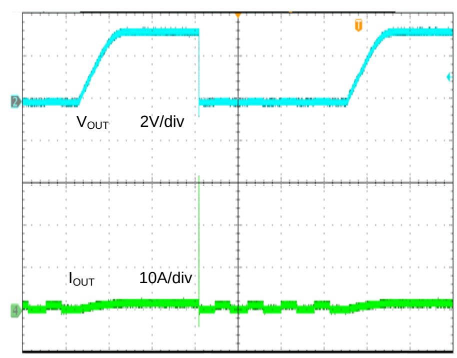
Time (2ms/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=0A-Short)



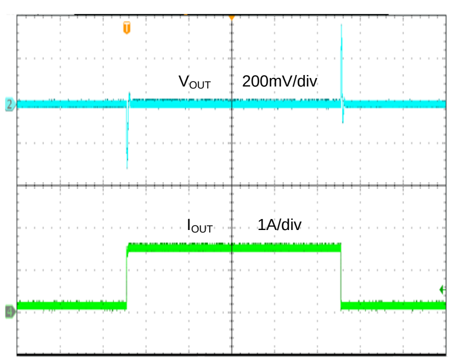
Time (20ms/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=1.5A-Short)

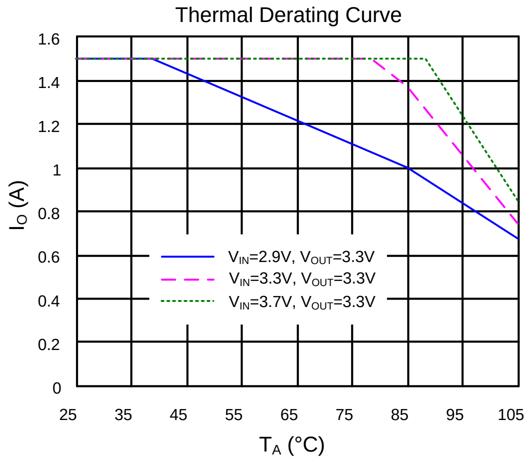


Time (20ms/div)

Load Transient
(V_{IN}=3.3V, V_{OUT}=3.3V, I_{OUT}=0.5A~1.5A)



Time (2ms/div)



Notes:

1) T_A: Air temperature, 0.5 inch above the IC.
2) Based on a four-layer Silergy Evaluation Board in the natural convection.
3) The inductor temperature is not beyond 115℃ under this TD curve.
4) For customer’s specific application, the recommended inductor temperature limitation is 115℃.

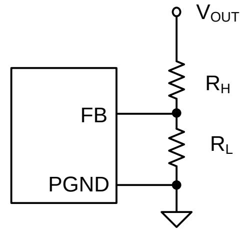
Applications Information

Because of the high integration in SY26901, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, and feedback resistors (R_H and R_L) need to be selected for the targeted applications.

Feedback resistor divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_H and R_L. A value between 10k and 1M is recommended for both resistors. If R_H=100k is chosen, then R_L can be calculated to be:

$$R_L = \frac{0.6R_H}{V_{OUT} - 0.6}(\Omega)$$



Input capacitor C_{IN}

To minimize the potential noise problem, place a typical X7U or better grade ceramic capacitor with higher than 6.3V rating and greater than 44µF capacitance, place this ceramic capacitor really close to the PVIN and PGND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the PVIN/PGND pins.

External Capacitor Recommendation

	Description	Vendor	PN
C_{IN}	10uF/10V/X7T,0603	Murata	GRM188D71A106KA73D
	22uF/6.3V/X7T,0805	Murata	GRM21BD70J226ME44L
	22uF/10V/X7R,1206	Murata	GCM31CR71A226KE02L
	47uF/6.3V/X7U,1206	Murata	GXM31CE70J476ME10L

Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7T or better grade ceramic capacitor with higher than 6.3V rating and greater than 88µF capacitance. Place this ceramic capacitor really close to the OUT and PGND pins to minimize the loop area formed by COUT, and the OUT/PGND pins.

External Capacitor Recommendation

	Description	Vendor	PN
C_{OUT}	10uF/10V/X7T,0603	Murata	GRM188D71A106KA73D
	22uF/6.3V/X7T,0805	Murata	GRM21BD70J226ME44L
	22uF/10V/X7R,1206	Murata	GCM31CR71A226KE02L

If the output capacitance is larger than 1000uF (ceramic) or other type of capacitor (polymer, tantalum…) is used, please contact Silergy supporting team to get more assessment.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown, the SY26901 shutdown current drops to lower than 0.1µA, driving the EN pin high (>1.5V) will turn on the IC again.

Soft Start Programming

SY26901 provides an external soft-start pin that gradually raises the output voltage. The soft-start time can be programmed by the external capacitor across the SS pin and PGND. The soft start time is calculated as:

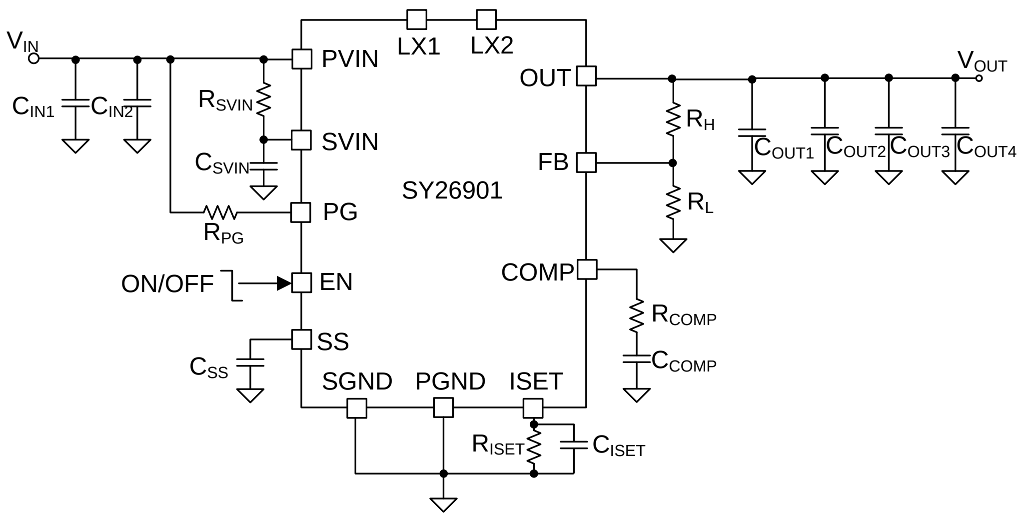
$$t_{SS} = \frac{0.7}{I_{SS}}C_{SS}$$

Don't leave the SS pin floating.

External Capacitor Recommendation

	Description	Vendor	PN
C_{SS}	100nF/50V/X8L,0603	Murata	GCM188L81H104KA57D
	100nF/100V/X8L,0603	Murata	GCJ188L8EL104KA07#
	220nF/50V/X7R,0603	Murata	GCM188R71H224KA64D

Typical application schematic



Bom List

Reference Designator	Description	Part Number	Manufacturer	Note
C_{IN1}, C_{IN2}, C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4}	22uF/6.3V/X7T,0805	GRM21BD70J226ME44L	Murata	
C_{SVIN}	1uF/25V/X7R,0603	GCM188R71E105KA64D	Murata	
C_{SS}	100nF/50V/X8L,0603	GCM188L81H104KA57D	Murata	
C_{COMP}	1nF/50V/C0G,0603	GRM1885C1H102JA01#	Murata	
R_H	100kΩ,1%,0603			
R_L	22.1kΩ,1%,0603			
R_{SVIN}	10Ω,1%,0603			
R_{PG}	100kΩ,1%,0603			
R_{COMP}	15kΩ,1%,0603			
R_{ISET}	0Ω,1%,0603			For FCCM application

Layout Design:

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, C_{OUT}, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to the PGND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.
2) SVIN is the power supply pin for the internal control circuit. Don't connect the SVIN pin to the PVIN pin directly. A separated 1uF ceramic cap is strongly recommended to decouple SVIN pin to PGND.
3) The decoupling capacitor of the VIN must be placed close enough to the PVIN pin and PGND pins. The loop area formed by the input capacitors, the PVIN pin and PGND pin must be minimized.
4) The PCB copper area associated with the LX pin must be minimized to improve the noise immunity.
5) The components R_H, R_L and the trace connecting to the FB/OUT pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to the FB/OUT pin.

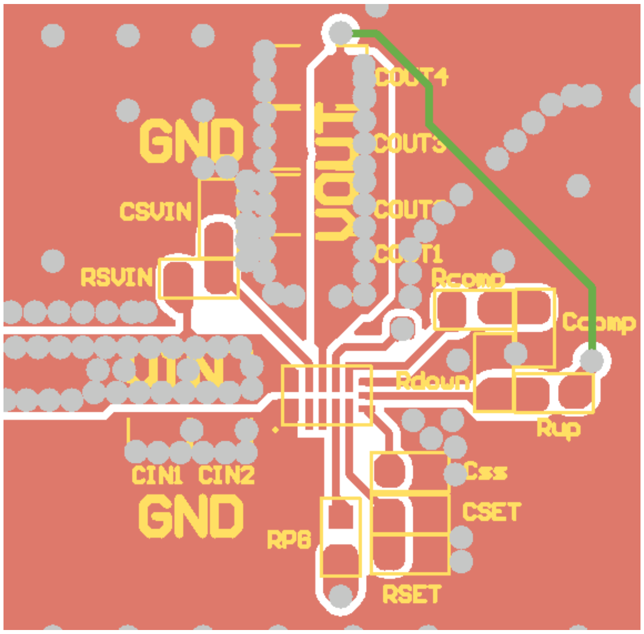
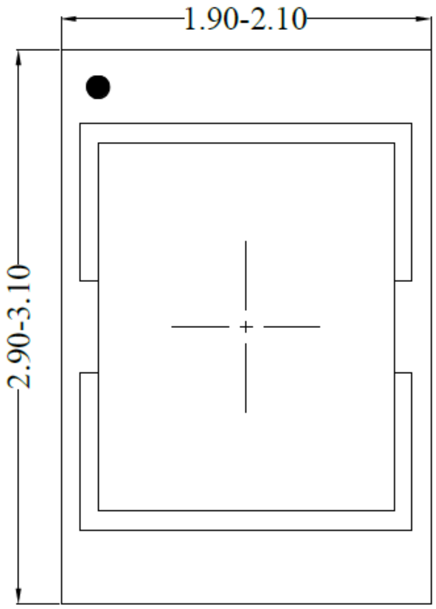
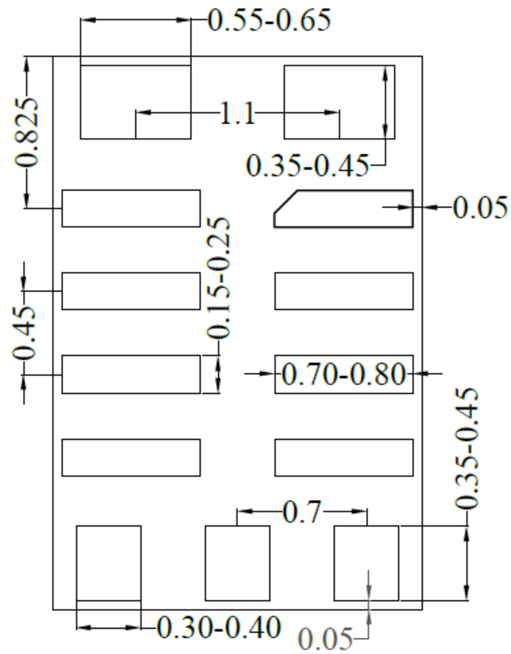


Figure 3. PCB Layout Suggestion

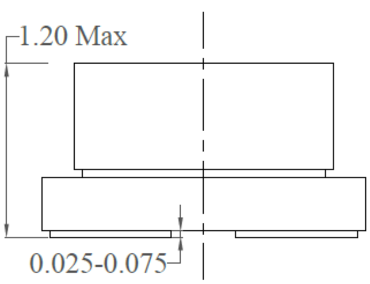
MQFN2×3-13 Package Outline Drawing



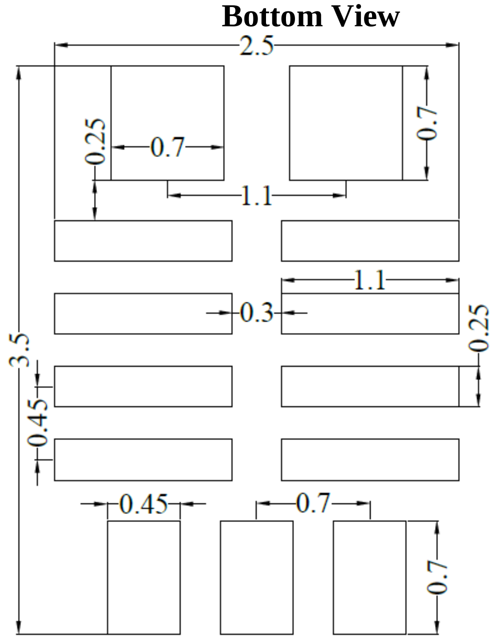
Top View



Bottom View



Side View

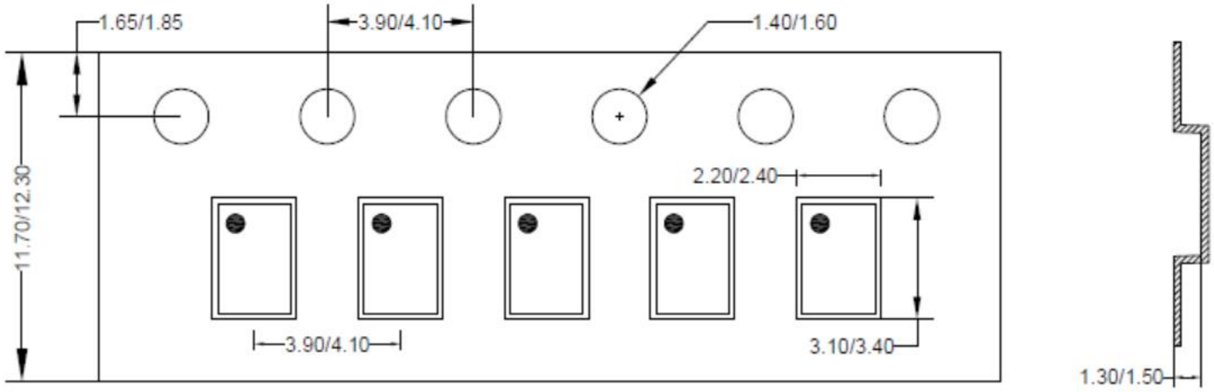


Recommended PCB layout
(Reference Only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

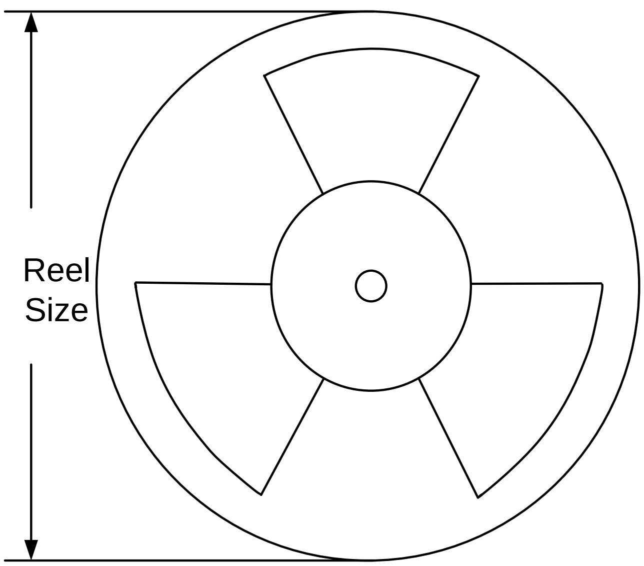
Taping & Reel Specification

1. Taping Orientation
MQFN2×3-13



Feeding Direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
MQFN2×3-13	12	4	7"	400	400	2500

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