SY21242

High Efficiency 6V, 1MHz, 2.5A Current Limit Step-Up Regulator

General Description

The SY21242 high efficiency step-up regulator operates using current mode control, over an input voltage range from 2V to 6V. It integrates an N-channel MOSFET with low 120mΩ $R_{DS(ON)}$ to minimize conduction loss.

The 1MHz switching frequency and internal compensation reduce external component count and save PCB space, and the built-in internal soft-start circuitry minimizes inrush current at startup.

The SY21242 is available in a compact SOT23-6 package.

Features

- Wide 2V to 6V Input Range
- Up to 6V Output Voltage
- Low $R_{DS(ON)}$ for Internal N-Channel MOSFET: 120mΩ
- 2.5A Minimum Switch Current Limit
- 1MHz Switching Frequency
- Minimum On-Time: 100ns Typical
- Minimum Off-Time: 100ns Typical
- Internal Soft-Start Limits Inrush Current
- ±2% 0.6V Reference
- RoHS-Compliant and Halogen-Free
- Compact SOT23-6 Package

Applications

- Solar Battery Charger
- Backup Battery

Typical Application

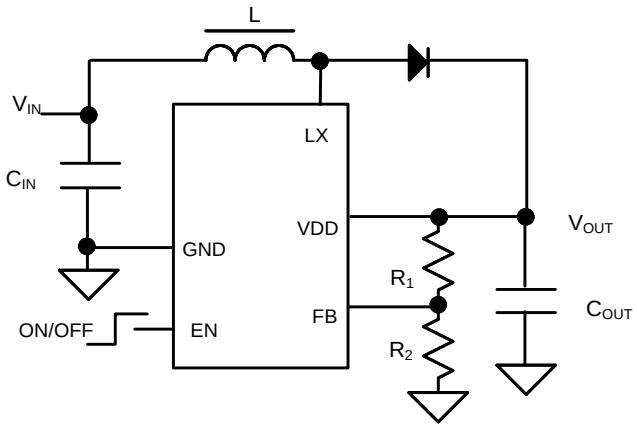


Figure 1. Typical Application Circuit

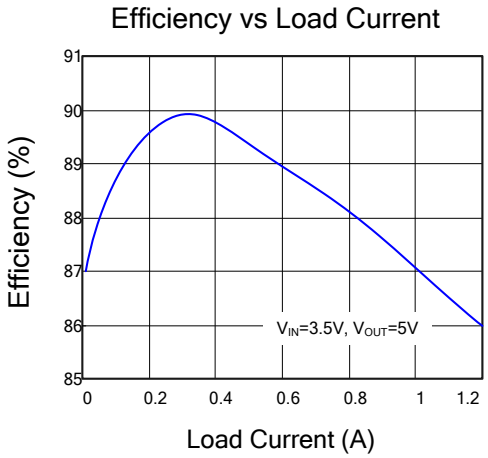


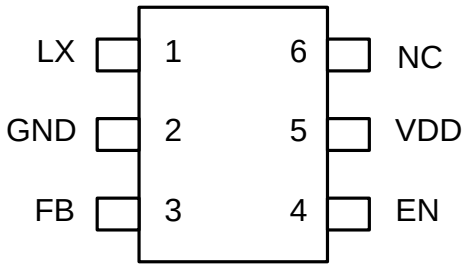
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY21242ABC	SOT23-6 RoHS-Compliant and Halogen-Free	**EX*xyz***

x = year code, y = week code, z = lot number code

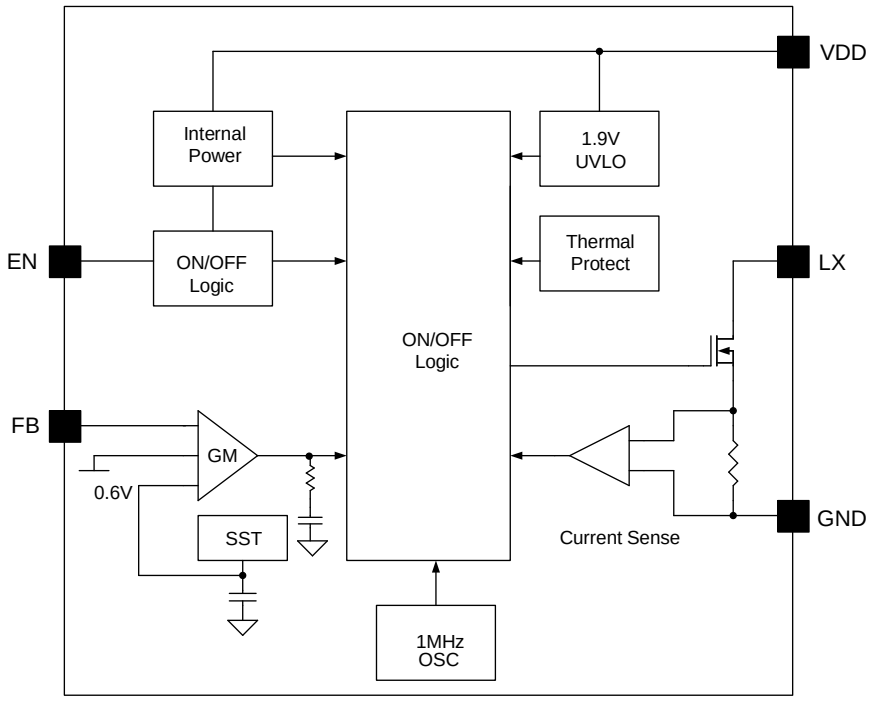
Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	LX	Inductor node. Connect an inductor between the IN and LX pins.
2	GND	Ground pin
3	FB	Feedback pin. Connect a resistor R1 between V_{OUT} and FB, and a resistor R2 between FB and GND to program the output voltage: V_{OUT} = 0.6V × (R1/R2+1).
4	EN	Enable pin. Drive low to disable the device, drive high to enable. Do not leave floating.
5	VDD	IC power supply input.
6	NC	No connection.

Block Diagram



Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
EN, VDD, LX	-0.3	7	V
FB	-0.3	3.6	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	200	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	130	
P_D Power Dissipation T_A = 25°C	0.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
V_{DD}	2	6	V
FB	0	1	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 3.3V, V_{OUT} = 5V, I_{OUT} = 100mA, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2		6	V
Quiescent Current	I_Q	V_{FB} = 0.66V		200		μA
Low Side Main FET R_{ON}	$R_{DS(ON)}$			120		mΩ
Main FET Current Limit	I_{LIM}		2.5			A
Switching Frequency	f_{sw}			1		MHz
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
IN UVLO Rising Threshold	$V_{IN,UVLO}$				1.9	V
Thermal Shutdown Temperature	T_{SD}			150		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

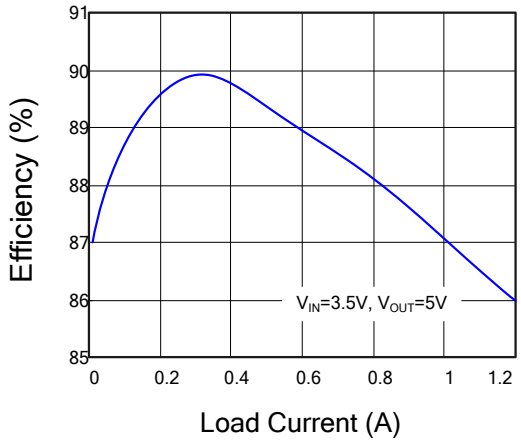
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

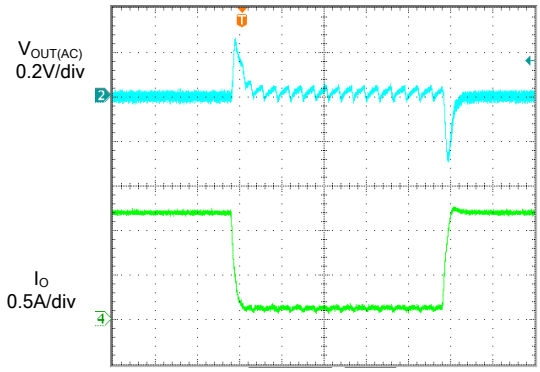
(T_A = 25°C, V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, C_{OUT} = 44µF, unless otherwise specified)

Efficiency vs Load Current



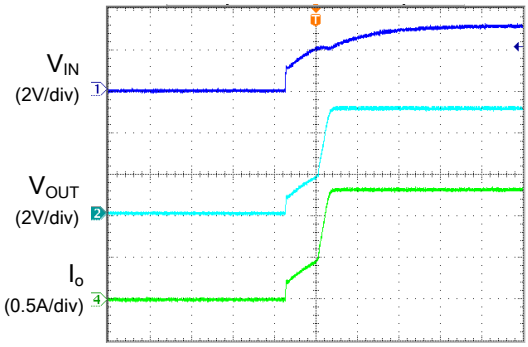
Load Transient

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=0.12~1.2A)



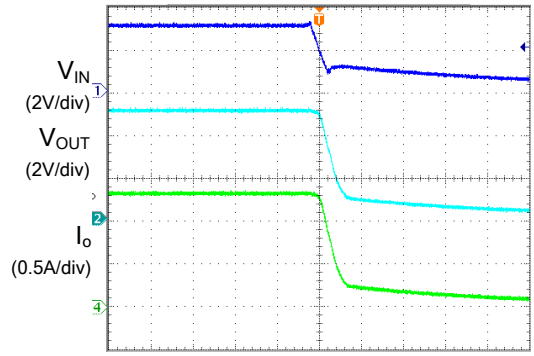
Startup from V_{IN}

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1.2A)



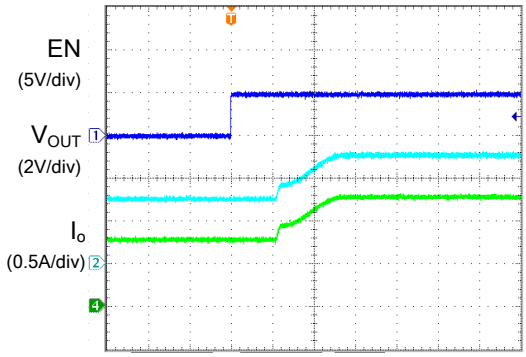
Shutdown from V_{IN}

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1.2A)



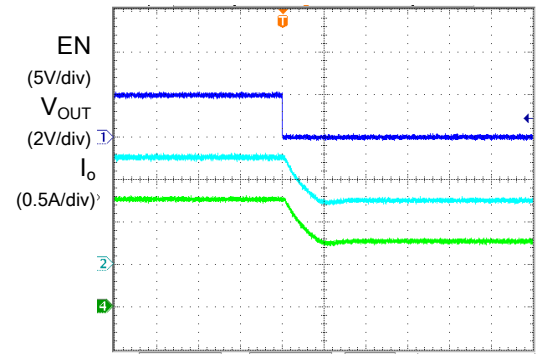
Startup from Enable

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1.2A)

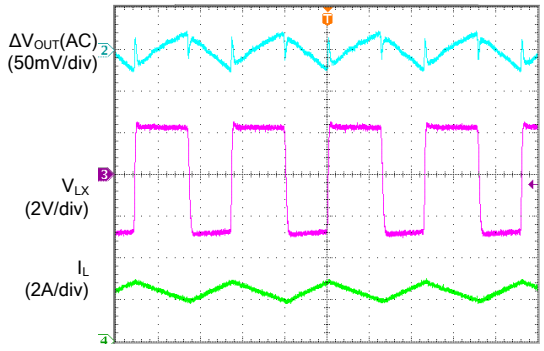


Shutdown from Enable

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1.2A)

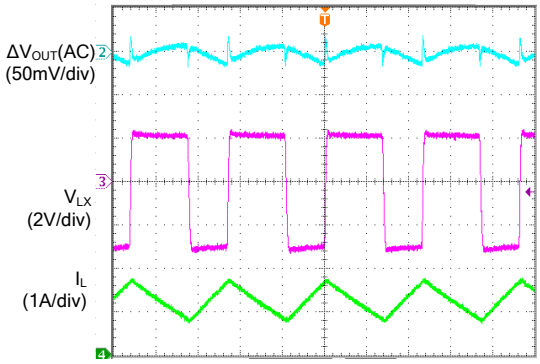


Output Ripple
(V_{IN}=3.3V, V_{OUT}=5V,I_O=1.2A)



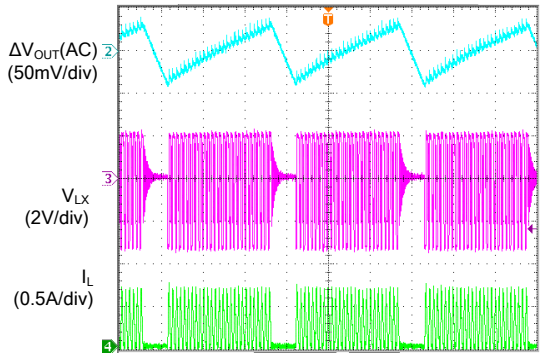
Time(400ns/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=5V,I_O=0.6A)



Time(400ns/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=5V,I_O=0.12A)



Time(10µs/div)

Detailed Description

The SY21242 high efficiency step-up regulator operates using current mode control over an input voltage range from 2V to 6V. It integrates an N-channel MOSFET with low 120mΩ $R_{DS(ON)}$ to minimize conduction loss.

The 1MHz switching frequency and internal compensation reduce external component count and save PCB space, and the built-in internal soft-start circuitry minimizes inrush current at startup.

Enable Operation

Driving the EN pin high (>1.5V) enables normal operation. Driving the EN pin low (<0.4V) places the device in shutdown. During shutdown mode, the SY21242 current drops to less than 10μA.

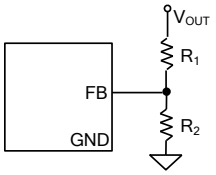
Application Information

The following paragraphs describe the selection process for the feedback resistors (R1 and R2), input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and diode D.

Feedback Resistor-Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R1 and R2 to minimize power consumption under light loads. If a value of 200kΩ is chosen for R1, then R2 can be calculated as:

$$R2 = \frac{0.6\text{V}}{V_{OUT}\text{-}0.6\text{V}} R1$$



Input Capacitor C_{IN}:

For the best performance, select a typical X5R or better grade ceramic capacitor with greater than 22μF capacitance. C_{IN} should be placed as close as possible to the module, while also minimizing the loop area formed by C_{IN} and the V_{DD}/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L\, f_{SW} \times V_{OUT}}$$

Output Capacitor C_{OUT}:

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use two X5R or better grade ceramic capacitors with 10V rating, and capacitance greater than 22μF each.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, both should be considered.

$$V_{RIPPLE,ESR1} = I_{LREAK} \times ESR$$

$$V_{RIPPLE,ESR2} = I_{LVALLEY} \times ESR$$

$$V_{RIPPLE,CAP} = \frac{I_{OUT} \times (1 - D)}{C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Boost Inductor L

Consider the following when choosing this inductor:

- Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

  where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

  The SY21242 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \frac{V_{OUT}}{V_{IN}} \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

- The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 10mΩ to achieve good overall efficiency.

Maximum Output Current Estimation

The maximum current that the converter can provide to the load depends on the output voltage / input voltage ratio.

Use the following formulas to evaluate an approximate max current that the converter can deliver when driving the load.

$$D=1-V_{IN(MIN)} \times \frac{\eta}{V_{OUT}}$$

Estimate the maximum output current:

$$I_{MAXOUT} = (IL_{MIN} - \frac{\Delta IL}{2}) \times \frac{\eta \times V_{IN(MIN)}}{V_{OUT}}$$

$$I_{MAXOUT} = \left(I_{LIM(MIN)} - \frac{\Delta IL}{2}\right) \times (1-D)$$

Where: $V_{IN(MIN)}$ is the minimum voltage at the boost input in the application, IL_{MIN} is the minimum device current datasheet limit (2.5 A for SY21242), ΔIL is the current ripple and η is the efficiency, which can be substituted with a value of 0.8 for simplicity.

Rectifier Diode

For high efficiency, choose a Schottky diode with low forward voltage drop and fast reverse recovery. The maximum current rating of the diode must be higher than the maximum input current, and the average current rating of the diode must be higher than the output current.

Applications with Large Bulk Capacitance

In applications with large bulk capacitance present on the output, a very high inrush current could flow through the inductor during power-on. In order to limit the current flowing into the device and prevent damage, a Zener diode connected from the power input to the output or an RC delay circuit added on the EN pin are recommended, as shown in Figure 3.

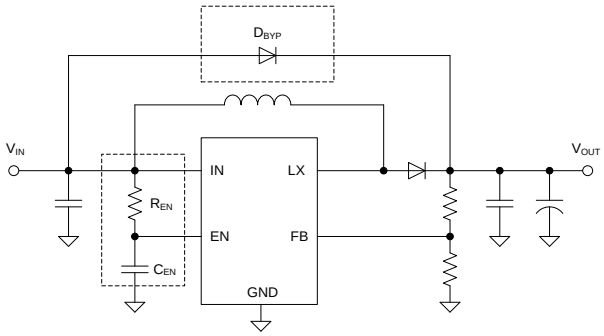


Figure 3. Application Circuit with Large Bulk Capacitance

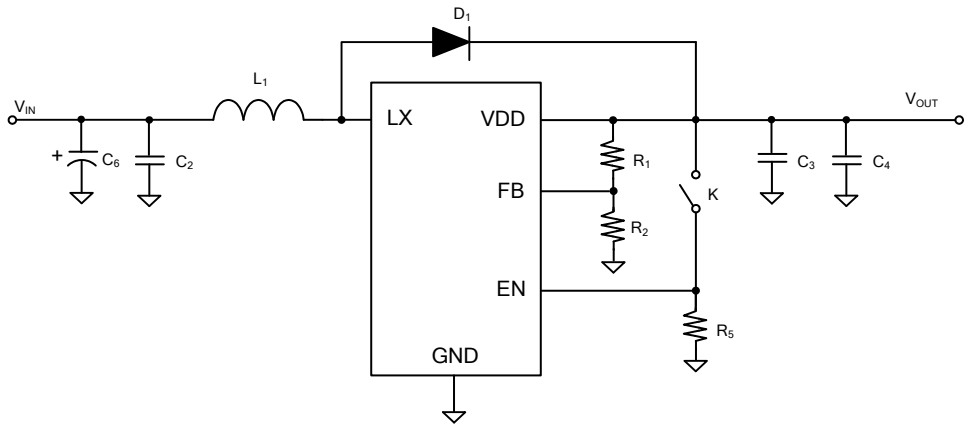
Thermal Protection

The SY21242 includes over temperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

Over Current Protection

The SY21242 provides a cycle-by-cycle overcurrent protection and turns off the main power MOSFET once the inductor current reaches the overcurrent limit threshold. During the overcurrent protection, the output voltage drops as a function of the load. If the output voltage drops below the input voltage, the current will directly flow through L and rectifier diode. In this case the current is only limited by the DC resistance in the path during the event. As soon as the overload condition is removed, the converter resumes operation.

Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage(V)	Input Current (A)
2–4.2	5	1

BOM List

Reference Designator	Description	Part Number	Manufacturer
L1	1.5μH/5.7A Inductor	VLC6045T-1R5N	TDK
C6	100μF/16V(electrolytic capacitor)		
C2	22μF/10V,1206, X5R	C3216X5R1A226M	TDK
C3 , C4	22μF/10V,1206, X5R	C3216X5R1A226M	TDK
R1	200kΩ, 1%, 0603		
R2	27.4kΩ, 1%, 0603		
R5	1MΩ, 1%, 0603		
D1	SS34		

Recommended Components for Typical Applications

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	L(μH)	C3
5	200	27.4	1.5	2×22μF/10V/X5R,1206

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- C_{IN} must be close to pins V_{DD} and GND. Minimize the loop area formed by C_{OUT}, LX, and GND.
- To reduce the switching noise, minimize the PCB copper area connected to the LX pin.
- In order to reduce crosstalk, R1, R2, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the IN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

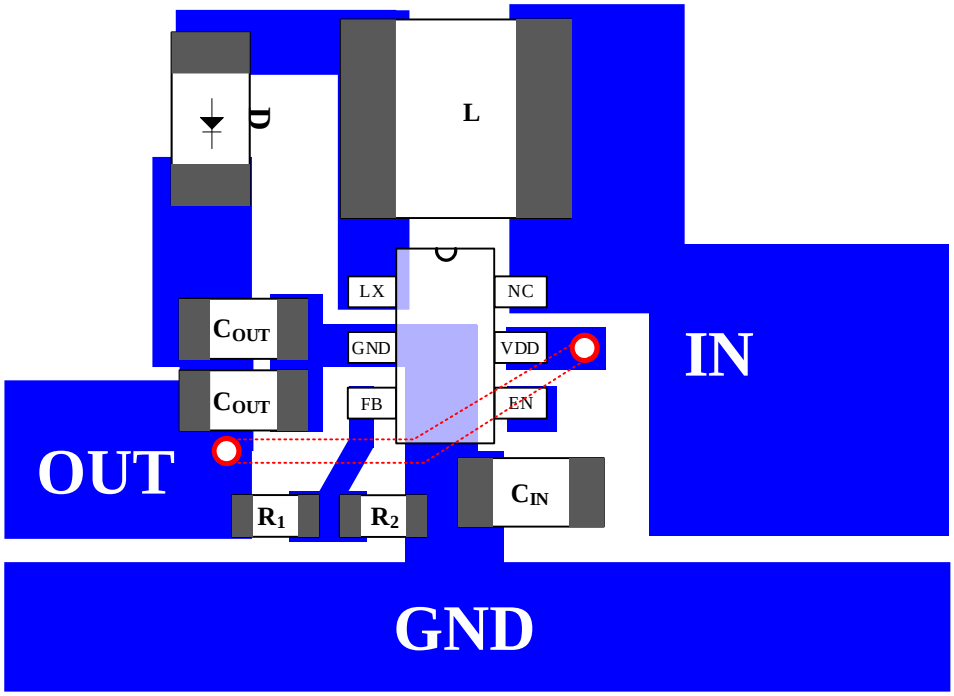
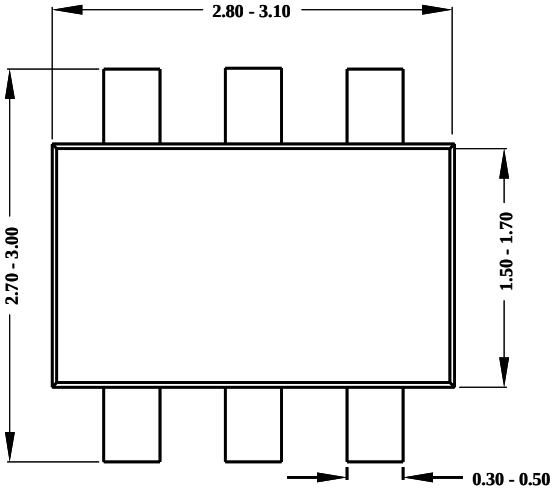
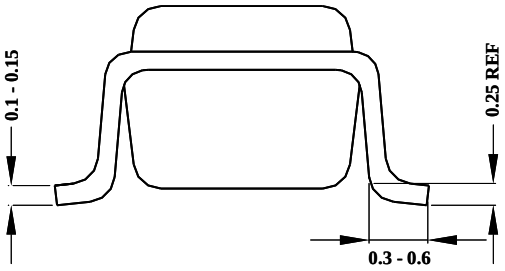


Figure 4. Suggested PCB Layout

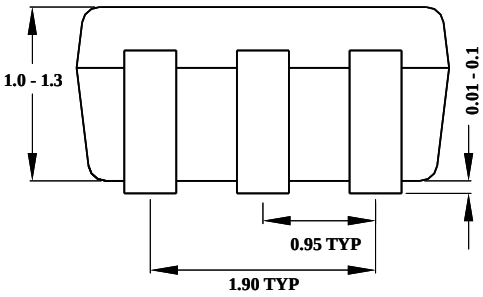
SOT23-6 Package Outline and PCB Layout



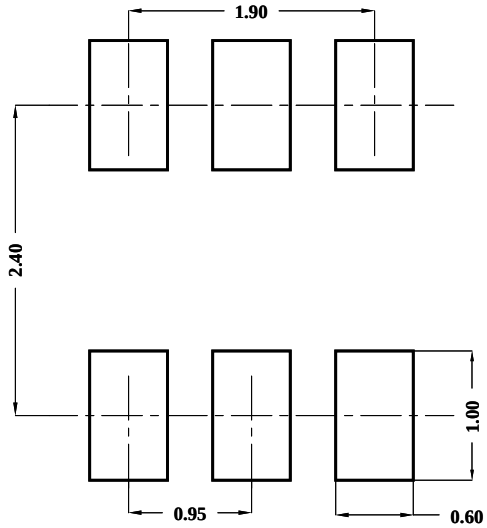
Top view



Side view



Side view

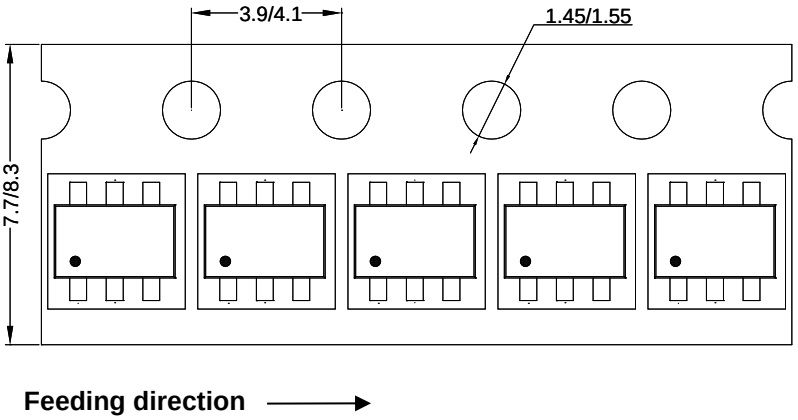


Recommended pad layout
(reference only)

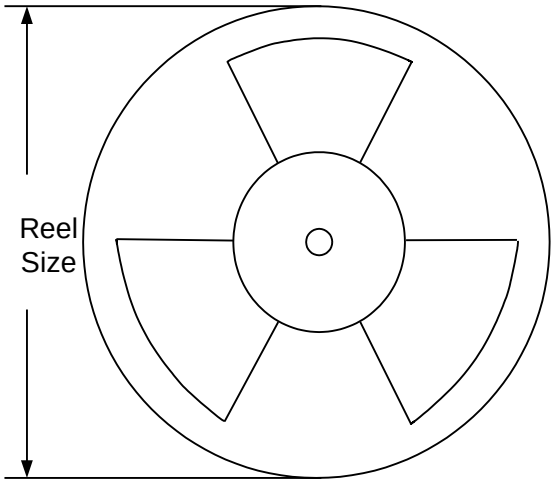
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

SOT23-6 taping orientation



Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Aug.18, 2023	Revision 1.0	Language improvements for clarity
Dec.18, 2011	Revision 0.9	Initial Release

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