

General Description

The SY21173 high-efficiency asynchronous Buck converter can deliver 3A output current over a wide input voltage range from 4.5V to 60V. The SY21173 employs a constant off-time and peak-current mode control strategy to achieve fast transient responses. It integrates a main switch with low $R_{DS(ON)}$ to minimize conduction loss.

The adjustable switching frequency permits low output-voltage ripple and reduces external inductor and capacitor sizes. The SY21173 also provides cycle-by-cycle current limiting, over temperature protection, and output short circuit protection.

The SY21173 is available in a compact SO8E package.

Features

- Low $R_{DS(ON)}$ for Internal N-Channel Power FET: 150m Ω
- 4.5V to 60V Input Voltage Range
- Up to 3A Output Current Capability
- Constant Off-Time and Peak-Current Mode Control
- Internal Soft-Start Limits the Inrush Current
- $\pm 1\%$ 0.8V Reference
- Adjustable Switching Frequency Range: 100kHz to 1MHz
- EN ON/OFF Control with Accurate Threshold
- Hiccup Mode Output Short Circuit Protection
- Cycle-by-Cycle Peak Current Limit
- RoHS-Compliant and Halogen-Free
- Compact Package: SO8E

Applications

- Non-Isolated Telecommunication Buck Regulator
- Secondary High-Voltage Post Regulator
- Automotive Systems
- Electric Bicycle

Typical Application

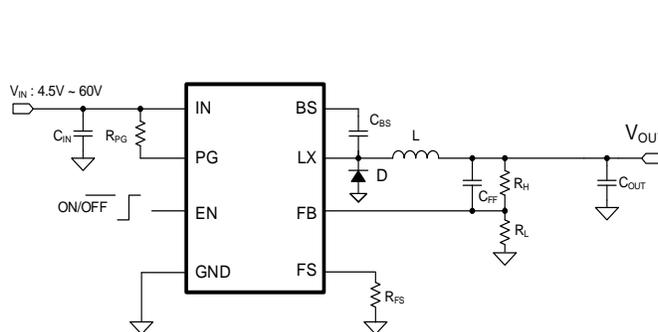


Figure 1. Schematic Diagram

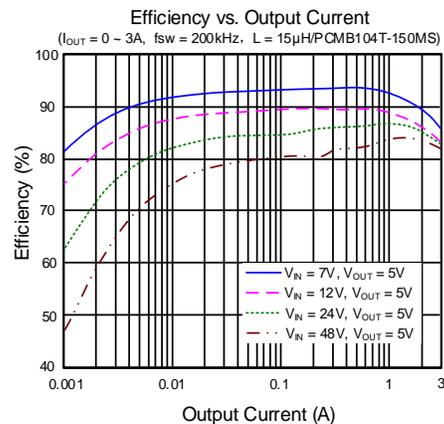


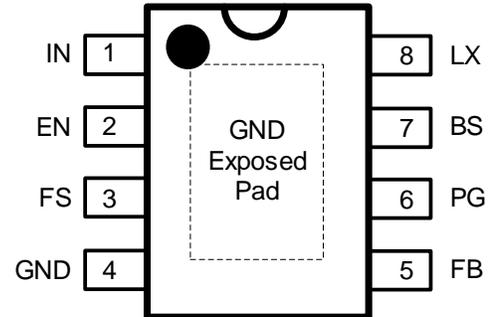
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21173FCC	SO8E RoHS-Compliant, Halogen-Free	DHAxyz

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	IN	Input pin. Decouple this pin to GND with at least a 1 μ F ceramic capacitor.
2	EN	Enable control. Pull this pin lower than EN falling threshold to disable the device, pull this pin higher than EN rising threshold to enable the device. Do not leave this pin floating.
3	FS	Frequency program pin. Connect a resistor to ground to program a switching frequency between 100kHz to 500kHz: $f_{sw}(kHz) = 10^5/R_{FS}(k\Omega)$.
4	GND	Ground pin.
5	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT} = 0.8V \times (1 + R_H/R_L)$.
6	PG	Power-good indicator. Open drain output when the output voltage is within 90% to 120% of the regulated value.
7	BS	Bootstrap pin. Supply for the power FET gate driver. Connect a 0.1 μ F ceramic capacitor between the BS pin and the LX pin.
8	LX	Inductor pin. Connect this pin to the switching node of the inductor.
EP	Exposed Pad	Exposed pad must be connected to the GND pin. Connect to system ground plane on application board for optimal thermal performance.

Block Diagram

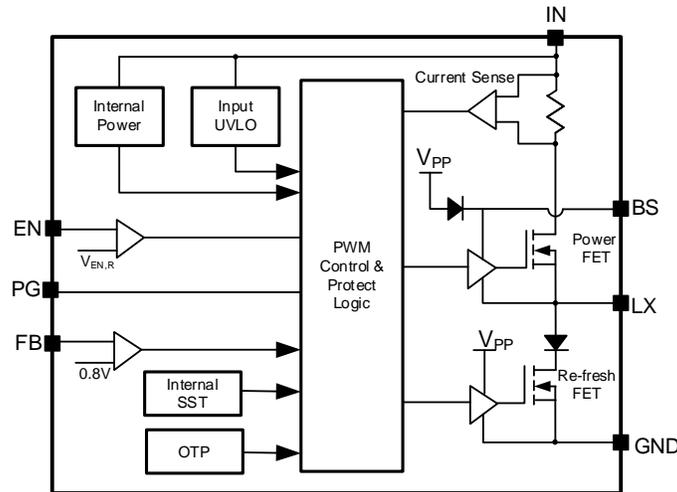


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	66	V
EN, FS, FB, PG	-0.3	IN + 0.3	
LX	-1	IN + 0.3	
BS-LX	-0.3	6	
LX, 10ns duration	GND - 5	IN + 3	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	42	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	4	
P_D Power Dissipation $T_A = 25^\circ\text{C}$	2.38	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	4.5	60	V
Output Current		3	A
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

($V_{IN} = 24V$, $V_{OUT} = 5V$, $L = 6.8\mu H$, $C_{OUT} = 22\mu F$, $T_A = 25^\circ C$, $I_{OUT} = 1A$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input	Voltage Range	V_{IN}	4.5		60	V	
	UVLO Rising Threshold	$V_{IN,UVLO}$	3.9	4.2	4.5	V	
	UVLO Hysteresis	$V_{IN,HYS}$	0.19	0.27	0.35	V	
	Quiescent Current	I_Q	$V_{FB} = 105\% \times V_{REF}$	70	100	130	μA
	Shutdown Current	I_{SHDN}	$V_{EN} = 0V$	2	6	16	μA
Output	Reference Voltage	V_{REF}	792	800	808	mV	
	FB input current	I_{FB}	$V_{FB} = 3.3V$	-50	50	nA	
	Soft-Start Time	t_{SS}	(Note 4)	2		ms	
	UVP Threshold	V_{UVP}	45	50	55	$\%V_{REF}$	
	UVP Delay	$t_{UVP,DLY}$		10		μs	
	UVP Hiccup On-Time	$t_{HICCUP,ON}$	(Note 4)	3		ms	
	UVP Hiccup Off-Time	$t_{HICCUP,OFF}$	(Note 4)	20		ms	
MOSFET	Power FET $R_{DS(ON)}$	$R_{DS(ON)}$	120	150	180	m Ω	
	Power FET Current Limit	I_{LMT}	3.8	4.5	5	A	
Enable (EN)	Rising Threshold	$V_{EN,R}$	1	1.1	1.2	V	
	Falling Threshold	$V_{EN,F}$	0.8	0.9	1	V	
	Leakage Current	$I_{EN,LKG}$	-1		1	μA	
COT	Switching Frequency Program Range	$f_{SW,RNG}$	$R_{FS} = 200k\Omega \sim 1M\Omega$ (Note 4)	100		500	kHz
	Switching Frequency Setting Accuracy	f_{SW}	$R_{FS} = 200k\Omega$	400	500	600	kHz
	Minimum On-time	$t_{ON,MIN}$		150		ns	
	Minimum Off-time	$t_{OFF,MIN}$		250		ns	
Power-Good	Rising Threshold	$V_{PG,R}$	V_{FB} rising, PG from low to high	91	95	98	$\%V_{REF}$
			V_{FB} falling, PG from low to high	111	115	118	$\%V_{REF}$
	Falling Threshold	$V_{PG,F}$	V_{FB} falling, PG from high to low	87	90	94	$\%V_{REF}$
			V_{FB} rising, PG from high to low	115	120	123	$\%V_{REF}$
	Delay time	$t_{PG,R}$	Low to high (Note 4)		200		μs
		$t_{PG,F}$	High to low (Note 4)		20		μs
Low voltage	$V_{PG,LOW}$	$I_{PG} = 2mA$			0.3	V	
Leakage current	$I_{PG,LKG}$				1	μA	
OTP	Temperature	T_{OTP}	(Note 4)	150		$^\circ C$	
	Temperature hysteresis	T_{HYS}	(Note 4)	15		$^\circ C$	

Note 1: Stresses beyond “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

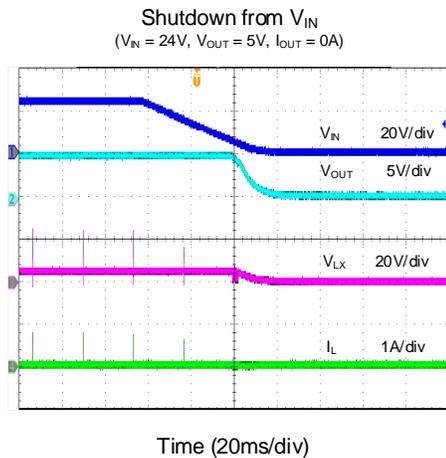
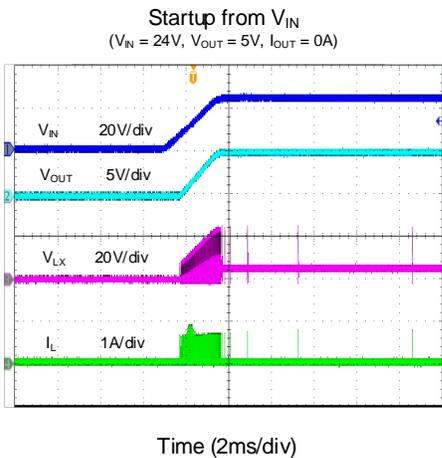
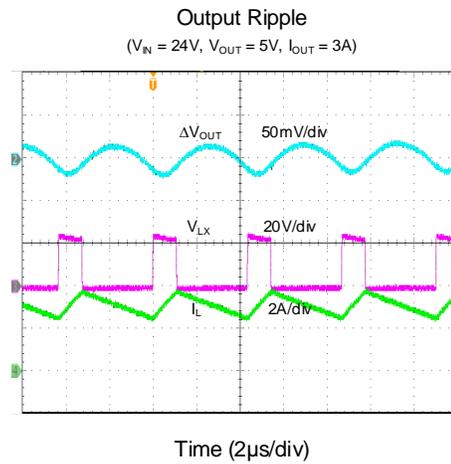
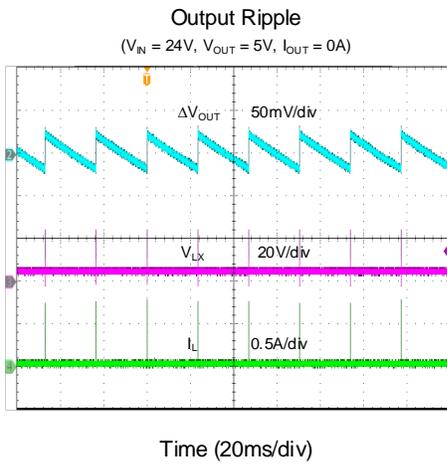
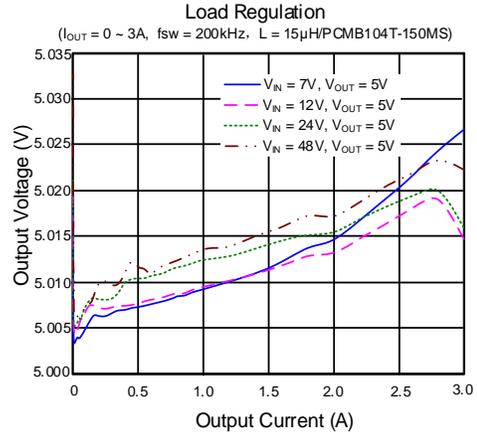
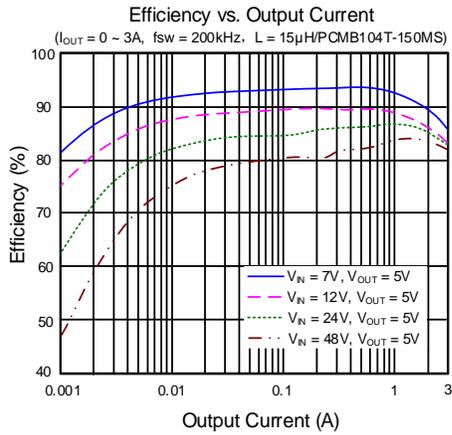
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a two-layer Silergy demo board.

Note 3: The device is not guaranteed to function outside its operating conditions.

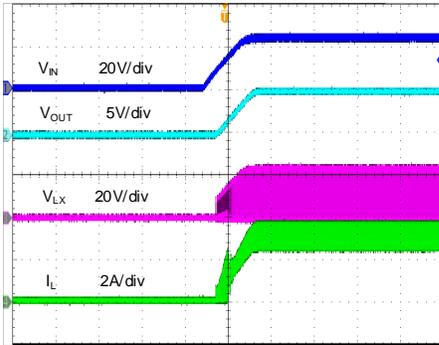
Note 4: Guaranteed by design.

Typical Performance Characteristics

($V_{IN} = 24V$, $V_{OUT} = 5V$, $L = 15\mu H$, $C_{OUT} = 22\mu F$, $T_A = 25^\circ C$, $I_{OUT} = 3A$, $f_{sw} = 200kHz$ unless otherwise specified)

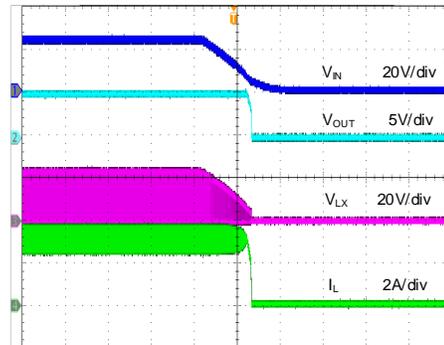


Startup from V_{IN}
($V_{IN} = 24V$, $V_{OUT} = 5V$, $I_{OUT} = 3A$)



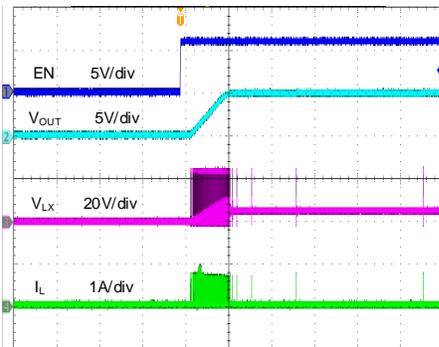
Time (2ms/div)

Shutdown from V_{IN}
($V_{IN} = 24V$, $V_{OUT} = 5V$, $I_{OUT} = 3A$)



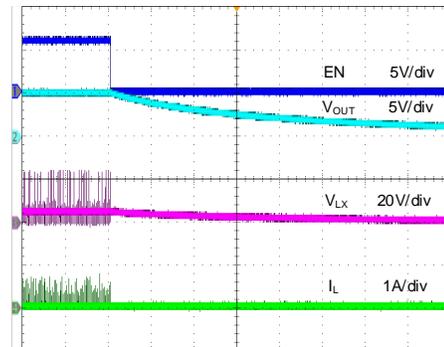
Time (20ms/div)

Startup from Enable
($V_{IN} = 24V$, $V_{OUT} = 5V$, $I_{OUT} = 0A$)



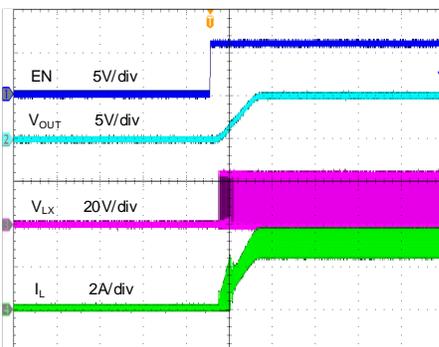
Time (2ms/div)

Shutdown from Enable
($V_{IN} = 24V$, $V_{OUT} = 5V$, $I_{OUT} = 0A$)



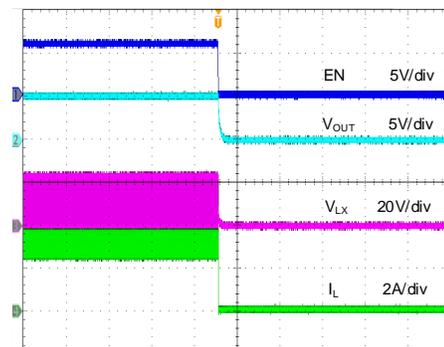
Time (1s/div)

Startup from Enable
($V_{IN} = 24V$, $V_{OUT} = 5V$, $I_{OUT} = 3A$)



Time (2ms/div)

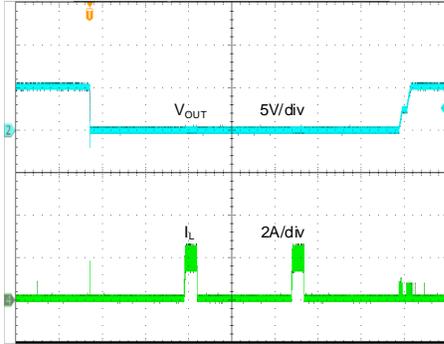
Shutdown from Enable
($V_{IN} = 24V$, $V_{OUT} = 5V$, $I_{OUT} = 3A$)



Time (2ms/div)

Short Circuit Protection

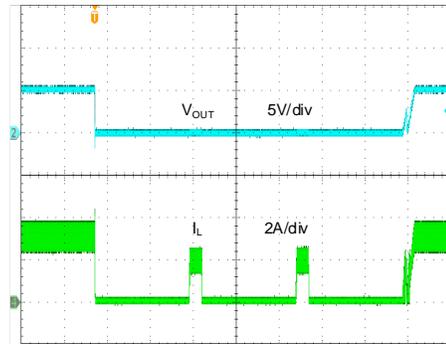
($V_{IN} = 24V$, $V_{OUT} = 5V$, $I_{OUT} = 0A \sim \text{Short}$)



Time (10ms/div)

Short Circuit Protection

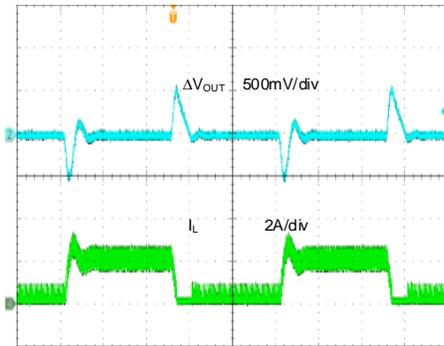
($V_{IN} = 24V$, $V_{OUT} = 5V$, $I_{OUT} = 3A \sim \text{Short}$)



Time (10ms/div)

Load transient

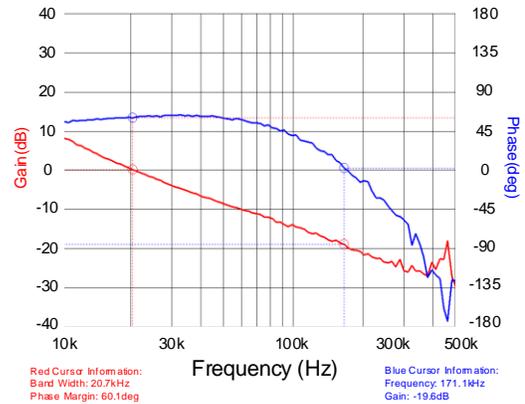
($V_{IN} = 24V$, $V_{OUT} = 5V$, $I_{OUT} = 0.2A \sim 2A$)



Time (200 μ s/div)

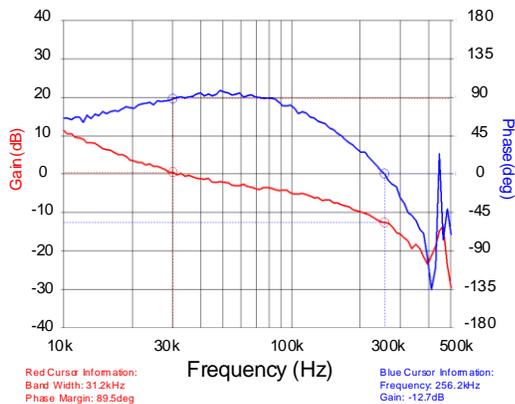
Bode Plot

($V_{IN} = 48V$, $V_{OUT} = 5V$, $I_{OUT} = 2A$, $f_{SW} = 500kHz$)



Bode Plot

($V_{IN} = 48V$, $V_{OUT} = 12V$, $I_{OUT} = 2A$, $f_{SW} = 500kHz$)



Detailed Description

General Features

The SY21173 high-efficiency asynchronous Buck converter can deliver 3A output current over a wide input voltage range from 4.5V to 40V. It integrates a power FET with low $R_{DS(ON)}$ to minimize conduction loss.

The adjustable switching frequency permits low output voltage ripple and reduces external inductor and capacitor sizes. The SY21173 also provides cycle-by-cycle current limiting, over temperature protection and output short circuit protection.

Constant Off-time Architecture

The SY21173 employs a constant off-time and peak-current mode control strategy. When the power FET's current-sense signal reaches internal V_{COMP} , the power FET turns off for a fixed period of time (constant off-time). t_{OFF} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{OFF} = \frac{1 - V_{OUT}/V_{IN}}{f_{SW}}$$

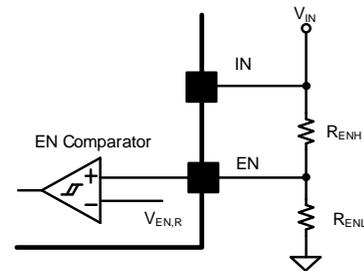
The power FET turns on after a period of t_{OFF} .

Input Under Voltage Lockout (UVLO)

To prevent operation before all internal circuitry is ready and to ensure that the top FET and bottom FET can be sufficiently enhanced, the SY21173 incorporates one input under-voltage lockout protections. The SY21173 remains in a low current state and all switching actions are inhibited until V_{IN} exceeds its rising threshold. At that time, if EN is enabled, the device will be turned on. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, switching actions will again be suppressed.

Enable and Adjusting Input Undervoltage Lockout

The EN pin provides programmable ON/OFF control by connecting an external resistor divider, and has an accurate rising and falling threshold. The converter will be turned on while the EN pin voltage exceeds the rising threshold. If the EN pin voltage is pulled below the falling threshold, the converter will stop switching and enter shutdown state.



If the input UVLO threshold is low for some high input UVLO threshold requirement applications, use EN to adjust the input UVLO by adopting two external divided resistors.

$$V_{IN,UVLO,ADJ} = \frac{R_{ENL} + R_{ENH}}{R_{ENL}} V_{EN,R}$$

It is not recommended to connect EN to the IN node directly. A resistor with a value between 1kΩ and 1MΩ is recommended if the EN pin is pulled high to the IN node.

Soft-start

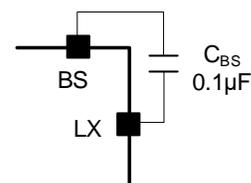
The device has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC startup. The typical soft-start time is 2ms.

Power-Good Indication

PG is an open drain output pin. This pin will be pulled to ground if the output voltage is lower than 90% of regulated value or higher than 120% of regulated value. Otherwise, this pin will go to a high impedance state.

External Bootstrap Capacitor

This external bootstrap capacitor provides the gate driver voltage for internal power MOSFET. A 0.1μF low-ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



Adjustable Switching Frequency

The FS pin is used for setting the switching frequency of the device by connecting a resistor from the FS pin to GND. The switching frequency of the device is adjustable from 100 kHz to 500kHz:

$$f_{SW} (kHz) = 10^5 / R_{FS} (k\Omega)$$

The SY21173 linearly folds back the switching frequency when the FB voltage is within 0 ~ 50% of the reference voltage during soft-start and the SCP event. The minimum switching frequency is clamped to 50kHz.

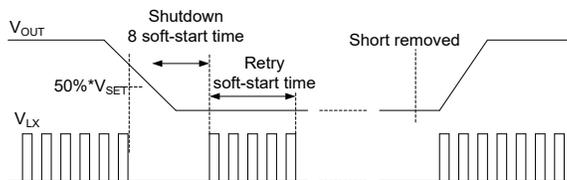
Fault-Protection Modes

Output Current Limit

With load current increasing, as soon as the power FET current exceeds the peak current-limit threshold, the power FET will turn off. If the load current continues to increase, the output voltage will drop.

Output Under Voltage Protection

With output current increasing, as soon as the power switch current exceeds the peak current limit threshold, the power switch will turn off. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 50% of the regulated value for approximately 10 μ s, the output undervoltage protection will be activated and the device will operate in hiccup mode. The hiccup on-time is 2ms, and the hiccup off-time is 20ms. If the hard short condition is removed, the device will return to normal operation.



Overtemperature Protection (OTP)

The device includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools by approximately 15°C, the device will resume normal operation after a complete soft-start

cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

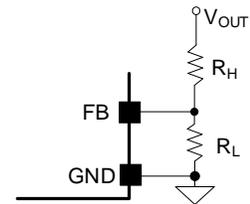
Application Information

The following paragraphs describe the selection process for the feedback resistors (R_H and R_L), input capacitor C_{IN} , output inductor L , output capacitor C_{OUT} , bootstrap capacitor and rectifier diode D .

Feedback Resistor-Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. Choose large resistance values between 10k Ω and 1M Ω for both R_H and R_L to minimize power consumption under light loads. If V_{OUT} is 5V, a value of 105k Ω is chosen for R_H , then using the following equation, R_L can be calculated as 20k Ω :

$$R_L = \frac{0.8V}{V_{OUT} - 0.8V} R_H$$



Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 100V rating and at least 1 μ F capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum, or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at $D = 0.5$, then

$$I_{CIN_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN_RIPPLE,CAP} = \frac{I_{OUT}}{f_{sw} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at $D = 0.5$, then

$$V_{CIN_RIPPLE,CAP} = \frac{I_{OUT}}{4 \times f_{sw} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 1 μ F X5R capacitor is sufficient in most applications.

Output Inductor L

Consider the following when choosing this inductor:

- 1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{sw} is the switching frequency and the $I_{OUT,MAX}$ is the maximum load current.

The SY21173 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- 2) The inductor's saturation current rating must be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{sw} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency. Choose an inductor with DCR less than 50m Ω to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or better grade ceramic capacitor with a 25V rating, and capacitance greater than 22 μ F.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

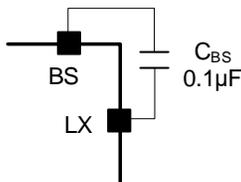
$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

External Bootstrap Capacitor

This external bootstrap capacitor provides the gate driver voltage for internal power MOSFET. A 0.1μF low-ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

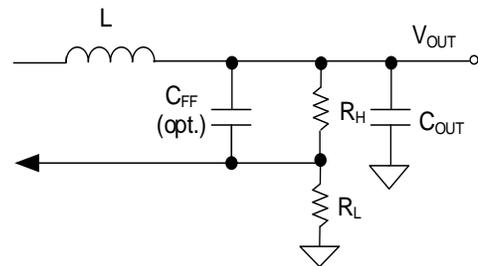


Rectifier Diode

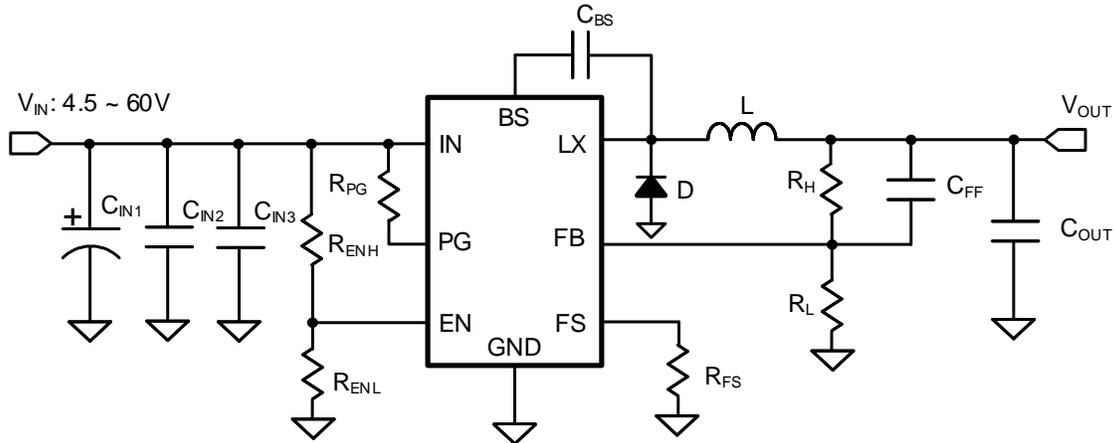
To accommodate the device high switching speed, choose a Schottky diode with low forward voltage and fast switching speed. The diode's voltage rating must be higher than the Buck converter maximum input voltage, and the diode's average and peak current rating should be greater than the Buck converter output average current and peak current.

Load Transient Consideration

The device integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic capacitor in parallel with R_H may further speed up the load transient response. It is recommended for applications with large load transient step requirements.



Application Schematic ($V_{OUT} = 5V$)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C _{IN1}	47μF/50V (electrolytic capacitor)		
C _{IN2}	2.2μF/100V/X7R, 1206	C3216X7R2A225KT	TDK
C _{IN3}	0.1μF/100V/X5R, 0603	C3216X5R2H104KT	TDK
C _{OUT}	22μF/25V/X5R, 1206	C3216X5R1E226M	TDK
C _{BS}	100nF/50V/X7R, 0603	C1608X7R1H104K	TDK
C _{FF}	22pF/50V/C0G, 0603	C1608C0G1H220J	TDK
L	15μH/Inductor	PCMB104T-150MS	CYNTEC
D	3A/100V	SS310	
R _H	105kΩ, 1%, 0603		
R _L	20kΩ, 1%, 0603		
R _{ENH}	10kΩ, 1%, 0603		
R _{ENL}	1MΩ, 1%, 0603		
R _{FS}	510kΩ, 1%, 0603		
R _{PG}	100kΩ, 1%, 0603		

Recommended Component Values for Typical Applications

V _{OUT} (V)	R _H (kΩ)	R _L (kΩ)	C _{FF} (pF)	L/Part Number	C _{OUT}
5	105	20	22	15μH/PCMB104T-150MS	22μF/25V, 1206, X5R
12	105	7.5	22	33μH/PCMB104T-330MS	22μF/25V, 1206, X5R

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- Input Capacitors:** Place the input capacitors close to the IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND using wide copper areas.
- Output Capacitor:** Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- Feedback Network:** Place the feedback components (R_H , R_L , and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.
- LX Connection:** Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.
- EN Signals:** It is not recommended to connect EN signal directly to V_{IN} . Use a resistor with a value between $1k\Omega$ and $1M\Omega$ if the lines are pulled high to V_{IN} .
- GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place multiple GND vias on it for heat dissipation.
- PCB Board:** To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.

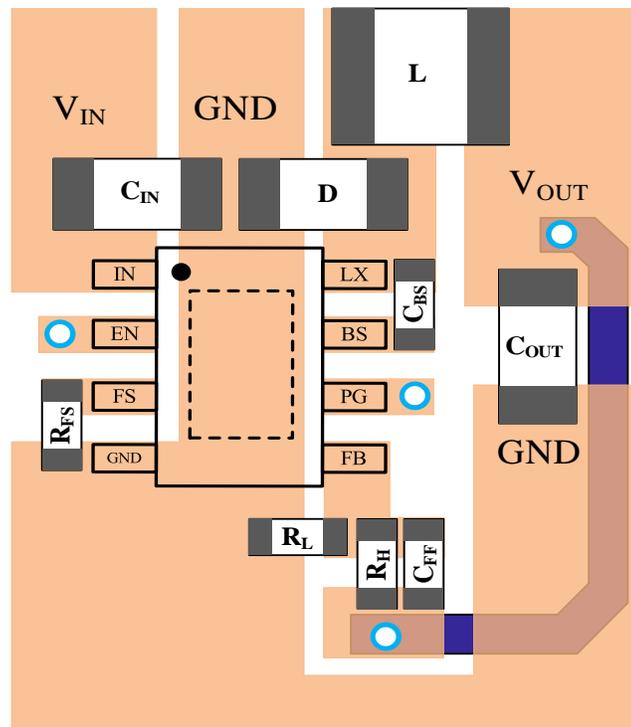
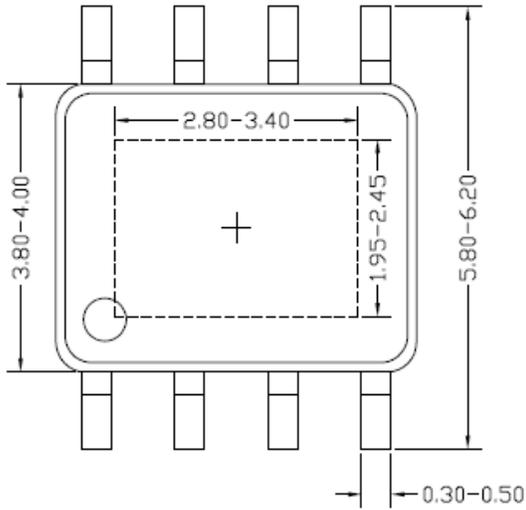
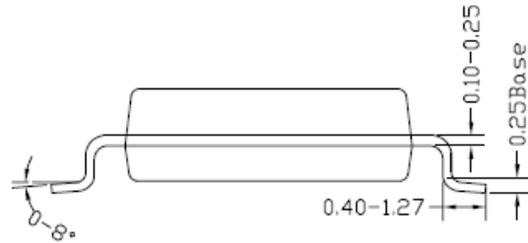


Figure 4. Suggested PCB Layout

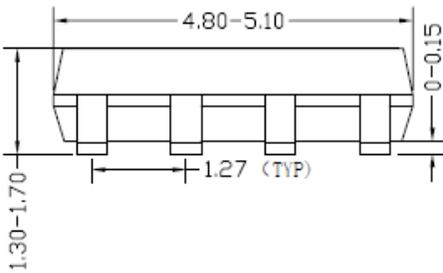
SO8E Package Outline and PCB Layout



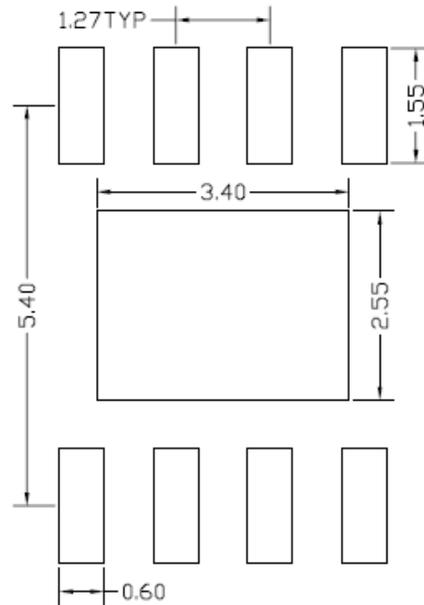
Top view



Side view



Front view

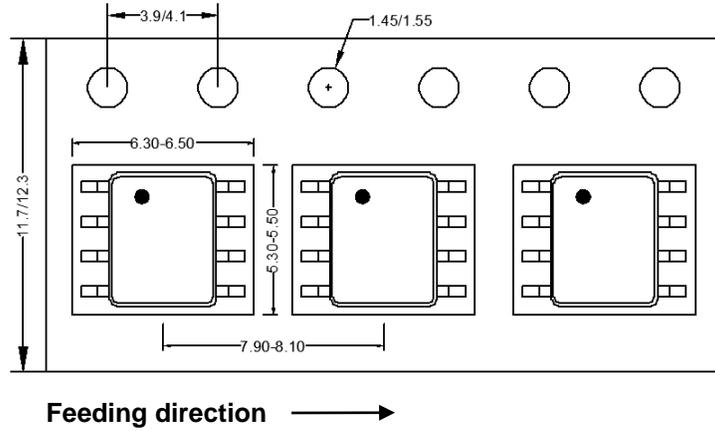


Recommended PCB layout (reference only)

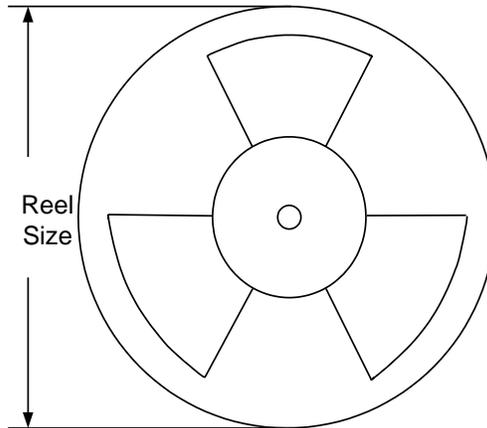
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping and Reel Specification

SO8E taping orientation



Carrier tape and reel specification for packages



Package Type	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
SO8E	12	8	13"	400	400	2500

Others: NA



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Aug.30, 2023	Revision 1.0	Language improvements for clarity.
Sep.29, 2020	Revision 0.9	Initial Release



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