Application Note: AN_SY6827

Dual Channel 6A, Ultra Low Loss Smart Bridge

General Description

SY6827 is a dual 6A ultra-low loss Smart Bridge for the intelligent power distribution in the computers or portable electronics. It reduces the number of point of load regulators required in a system and minimizes the power consumption at standby mode. Tiny DFN2x2 package also minimizes the solution size and PCB cost. Programmable turn-on delay allows the proper power sequencing during the transition of different operation modes. Programmable ramp-up time minimizes the inrush current. Integrated over-temperature protection and short circuit protection improve the reliability of the overall system.

Ordering Information

SY6827 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6827DFC	DFN2x2-8	

Features

- Low $R_{DS(ON)}$ for internal bridge FET: 15mΩ
- Maximum output current per channel: 6A
- Distribution voltages: 0.6V~5.5V
- Compact Package: DFN2x2-8
- Programmable turn on delay
- Over-temperature protection
- Short circuit protection
- Programmable ramp-up time
- Automatic output discharge at shutdown
- Short circuit protection
- Thermal protection
- RoHS Compliant and Halogen Free

Applications

- Notebook PC or Tablet PC or Net PC
- Desktop PC
- Server
- Set Top Box
- E-Book or MID
- Smart TV
- Router
- Industrial PC

Typical Applications

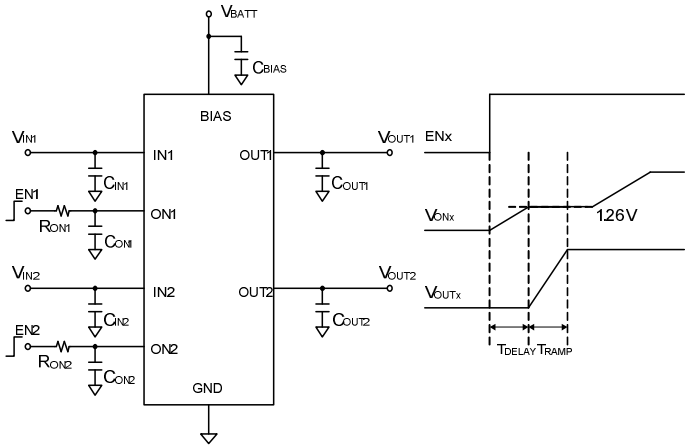
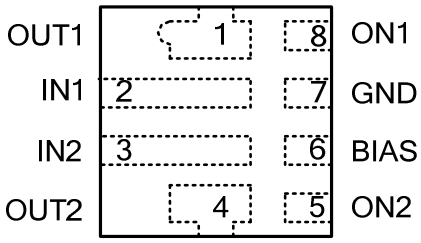


Figure 1. Schematic Diagram

Pinout (top view)



(DFN2x2-8)

Top mark: **EI*xyz*** for SY6827 (Device code: EI, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN1	2	Input pin for channel 1.
IN2	3	Input pin for channel 2.
GND	7	Ground pin
OUT1	1	Output pin for channel 1.
OUT2	4	Output pin for channel 2.
ON1	8	ON/OFF control pin for channel 1. When ON>0.6V, the internal bias is turned on. Connect this pin to RC circuit (as shown in Figure 1) to control the ramp-up time and turn on delay. The ramp-up time is controlled by R_{ON1}, and the delay is programmable by C_{ON1} and $R_{ON1.}$
ON2	5	ON/OFF control pin for channel 2. When ON>0.6V, the internal bias is turned on. Connect this pin to RC circuit (as shown in Figure 1) to control the ramp-up time and turn on delay. The ramp-up time is controlled by R_{ON2}, the delay time is programmable by C_{ON2} and $R_{ON2.}$
BIAS	6	Bias pin. Bias supply for overdriving the gate of the bridge between input and output. Recommend the BIAS voltage to be at least 3V above INx rails.

Absolute Maximum Ratings (Note 1)

BIAS Pin ---------- 30V
All other pins---------- ---------- 6V
Power Dissipation, PD @ TA = 25°C DFN2x2-8 FC, ---------- 2W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 62.5°C/W
θ_{JC} ---------- 10°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- 65°C to 150°C

Recommended Operating Conditions (Note 3)

IN, OUT ---------- 0.6V to 5.5V
BIAS---------- V_{IN}+3V to 28V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{BIAS}=12V,V_{IN} = 3.3V, T_A = 25°C unless otherwise specified)

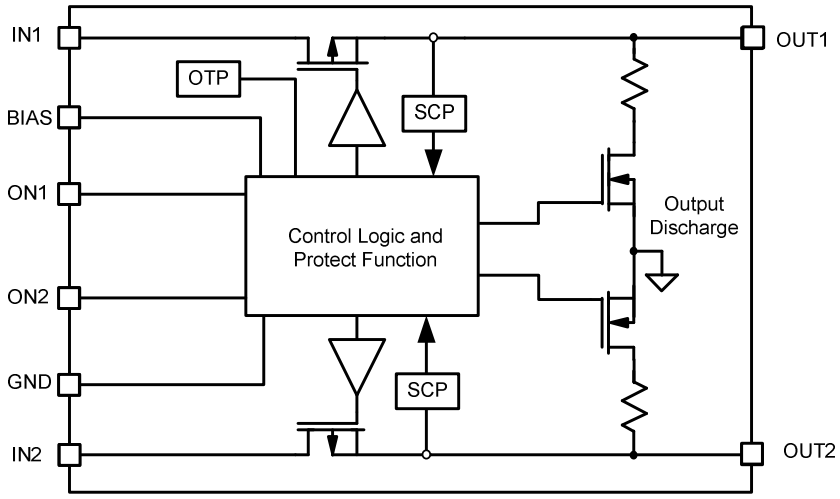
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		0.6		5.5	V
Bias Voltage Range	V_{BIAS}		V_{IN}+3		28	V
Bias current	I_{BIAS}	V_{ON}=3.3V, I_{OUT}=0		20		uA
Shutdown Bias Current	I_{SHDN}	V_{ON}=0		2		μA
FET RON	$R_{DS(ON)}$			15		mΩ
ON Clamping Threshold	Von,clp		1.16	1.26	1.36	V
(BIAS-IN) UVLO Threshold	$V_{BIAS-IN,UVLO}$				3	V
(BIAS-IN) UVLO Hysteresis	$V_{BIAS-IN,HYS}$			0.2		V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. The device is not guaranteed to function outside its operating conditions

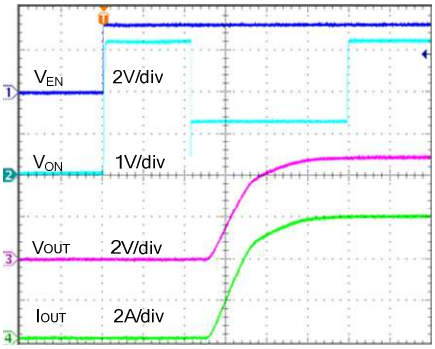
Block Diagram



Typical Operating Characteristics

Startup From Enable

V_{IN}=5V,V_{BIAS}=12V,V_{EN}=3.3V,R_{LOAD}=0.825Ω,
R_{ON}=300kΩ,C_{ON}=NULL



Time (400us/div)

Startup From Enable

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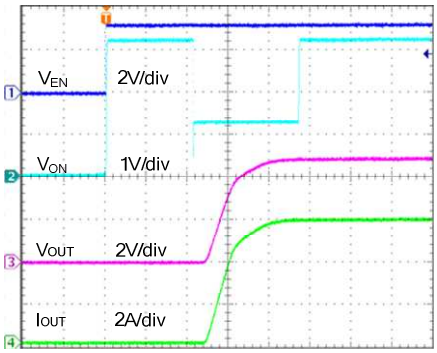
R_{ON}=200kΩ,C_{ON}=NULL



Time (400us/div)

Startup From Enable

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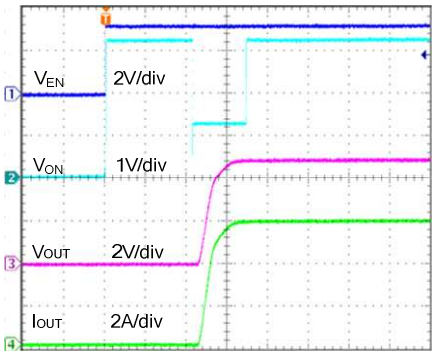
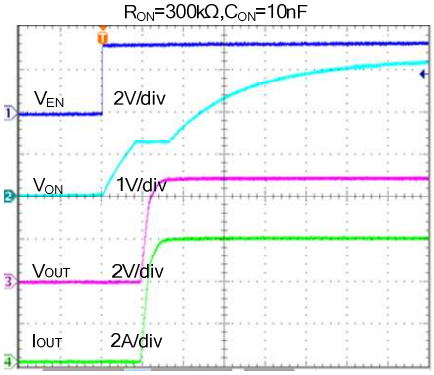
R_{ON}=100kΩ,C_{ON}=NULL



Time (400us/div)

Startup From Enable

V_{IN}=5V,V_{BIAS}=12V,V_{EN}=3.3V,R_{LOAD}=0.825Ω,
R_{ON}=300kΩ,C_{ON}=10nF



Time (2ms/div)

Startup From Enable

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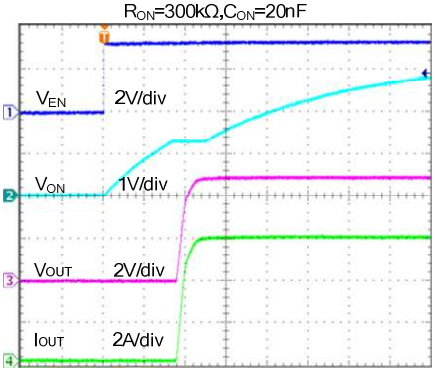
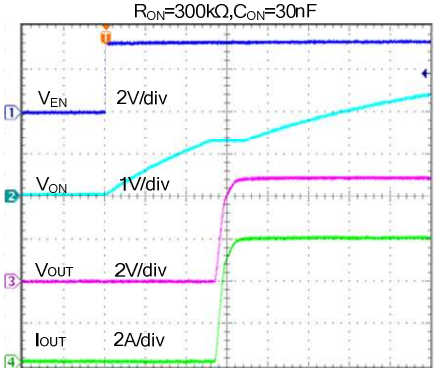
R_{ON}=300kΩ,C_{ON}=20nF



Time (2ms/div)

Startup From Enable

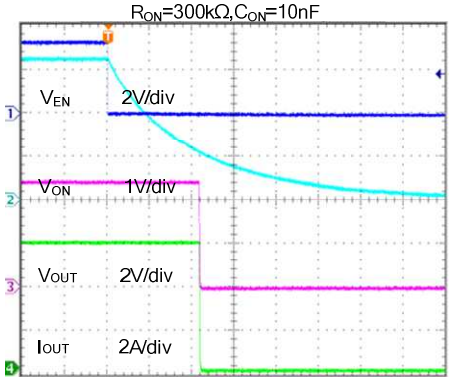
V_{IN}=5V,V_{BIAS}=12V,V_{EN}=3.3V,R_{LOAD}=0.825Ω,
R_{ON}=300kΩ,C_{ON}=30nF



Time (2ms/div)

Shutdown From Enable

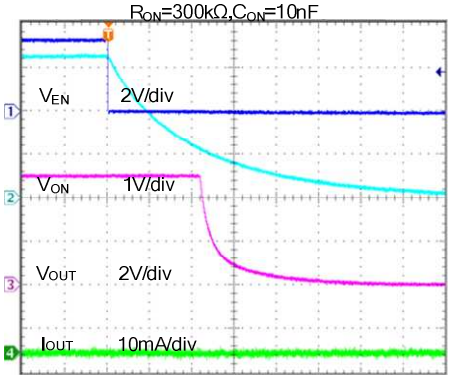
V_{IN}=5V,V_{BIAS}=12V,V_{EN}=3.3V,R_{LOAD}=0.825Ω,
R_{ON}=300kΩ,C_{ON}=10nF



Time (2ms/div)

Shutdown From Enable

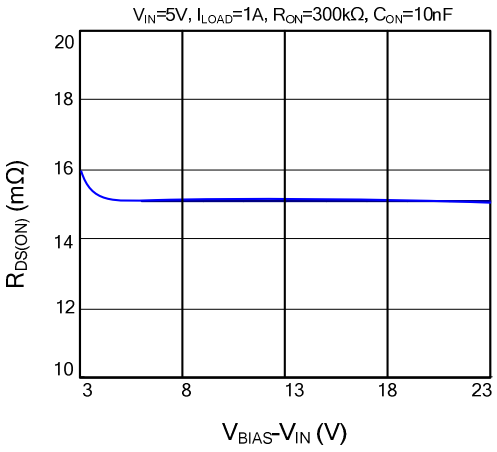
V_{IN}=5V,V_{BIAS}=12V,V_{EN}=3.3V,R_{LOAD}=NULL,
R_{ON}=300kΩ,C_{ON}=10nF



Time (2ms/div)

$R_{DS(ON)}$ VS. (V_{BIAS}-V_{IN})

V_{IN}=5V, I_{LOAD}=1A, R_{ON}=300kΩ, C_{ON}=10nF



Operation

SY6827 is a dual 6A, ultra low loss Smart Bridge. The internal N-channel MOSFET bridge can support as high as 6A maximum continuous current over an input voltage range of 0.6V to 5.5V. The turn on delay time and rise time can be programmed by R_{ON} and C_{ON} connected to EN pin.

Applications Information

Supply Filter Capacitor:

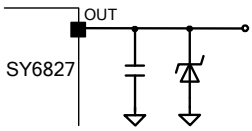
In order to limit the voltage drop on the input supply during hot-plug events, a 10uF ceramic capacitor placed close to IN and GND pins is recommended. Higher values of C_{IN} can be used to further reduce the voltage drop during high current application.

Bias Filter Capacitor:

A 0.1uF ceramic capacitor should be place between BIAS and GND pins to bypass the high frequency noise of bias supply.

Output Filter Capacitor:

A 10uF output ceramic capacitor is recommended to be placed close to the IC and output connector to reduce voltage drop during load transient. Higher values of C_{OUT} can be use to further reduce the voltage drop during high current application. If long cables are connected to the output terminals, an anti-parallel schottky diode is suggested to be placed on the output terminal to absorb the negative ringing caused by the cable inductance.



Output Turn on Delay and Rise Time:

Turn on delay time and rise time can be easily programmed by R_{ON} and C_{ON}. The delay time can be calculated using following equation:

$$T_{Delay} = R_{ON} \times C_{ON} \times \ln\left(\frac{V_{EN}}{V_{EN} - 1.26}\right)$$

The minimum delay time is 860uS.

The rise time is proportional to $\frac{R_{ON}}{V_{EN} - 1.26}$, where V_{EN} is the control input voltage. The typical rise time is 380uS when R_{ON}=300kΩ,V_{EN}=3.3V.

Output Discharge:

When the bridge MOSFET is off, a 100Ω on-chip load resistor is connected to the output to quickly discharge the output.

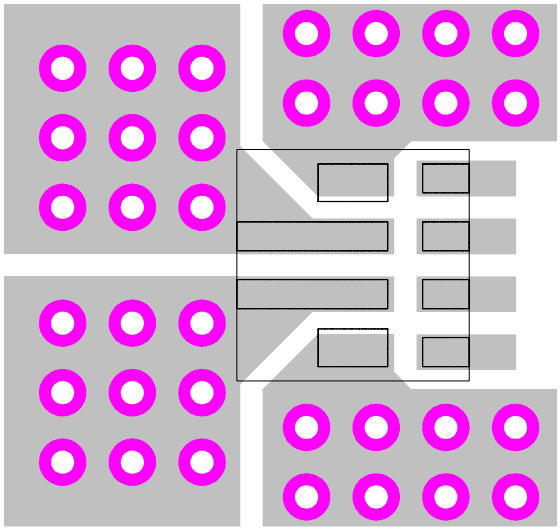
Short Circuit Protection:

When the V_{DS} of the bridge MOSFET exceeds 300mV, a hard short condition is detected. The device will latch off until ON pin is reset.

PCB Layout Guide

For best performance of the SY6827, the following guidelines must be strictly followed:

1. Keep all power trace as short and wide as possible. And it is desirable to use 4-layer or 6-layer board for thermal performance and better capability of current flow. At least 6 vias are suggested to put around each power pin to distribute current to different PCB layer. These power pins include IN1, IN2, OUT1, and OUT2.
2. Place input capacitor close to the IC, and output capacitor close to the IC and connectors for better transient performance.
3. Place bias capacitor close to the IC to reduce the noise on bias supply.



EVB Schematic

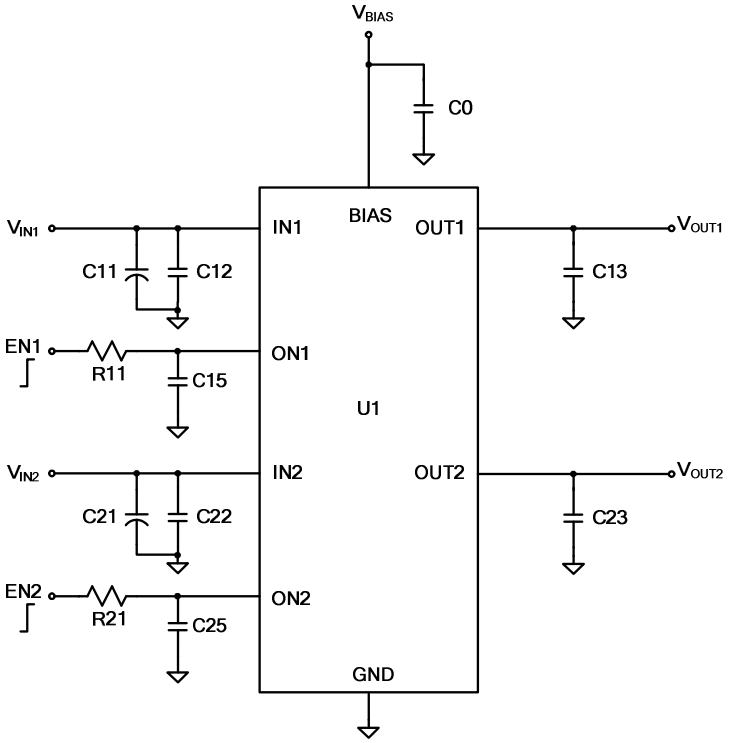


Figure2. Schematic Diagram

Quick Start Guide (Refer to Figure 3)

1. Connect the output load to V_{OUT} and GND output connectors. Preset the load current to between 0A and 6A.
2. Preset the input supply to a voltage between 0.6V and 5.5V. Turn the supply off. Connect the input supply to V_{IN} and GND input connectors.
3. Preset the bias supply to a Voltage between V_{IN}+3V and 28V. Turn the supply off. Connect the bias supply to V_{BIAS} and GND input connectors.
4. Turn on the bias and input supply , then measure the output voltage.

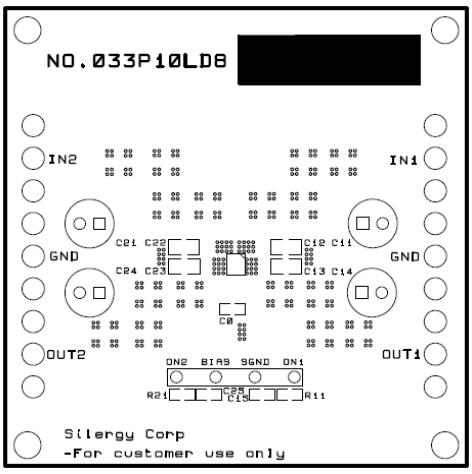
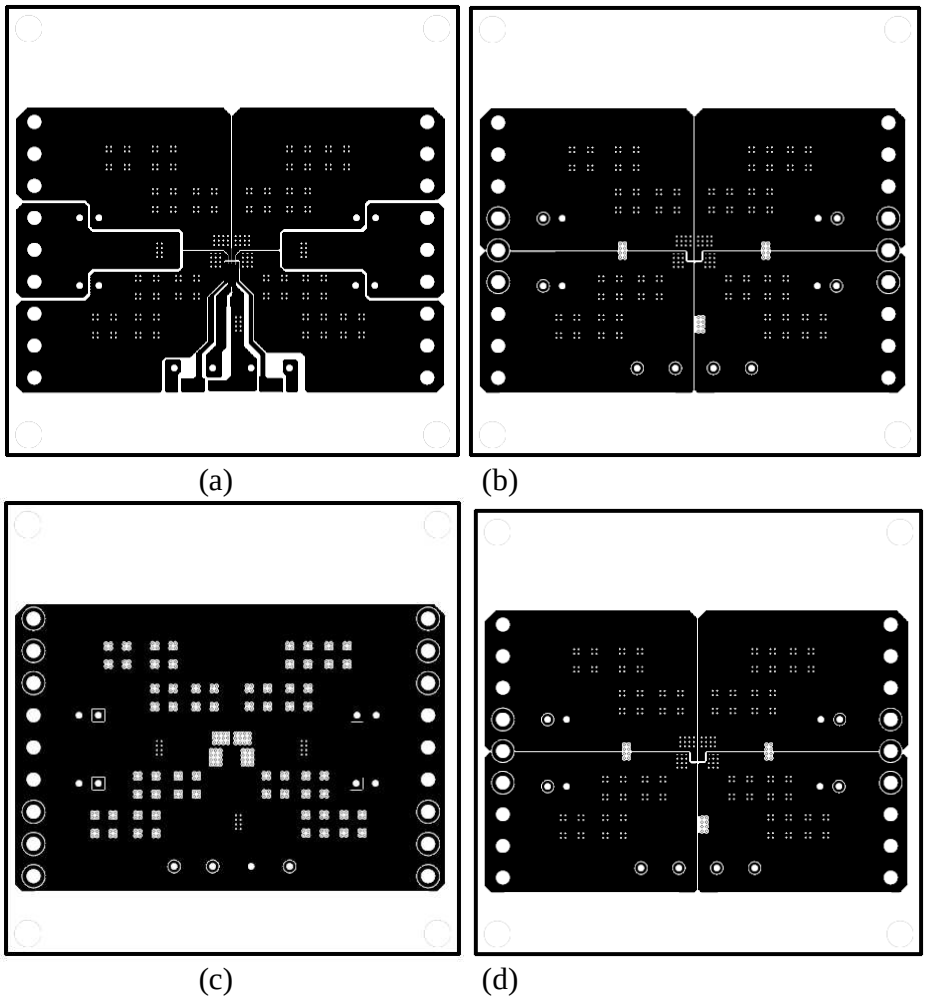


Figure 3. Top Silkscreen

PCB Layout



(a) (b)

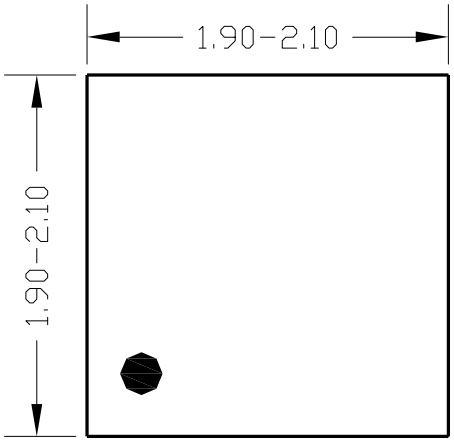
(c) (d)

Figure 4. PCB Layout Plots: (a) top layer, (b)Middle layer 1 (c) Middle layer 2, (d) Bottom layer

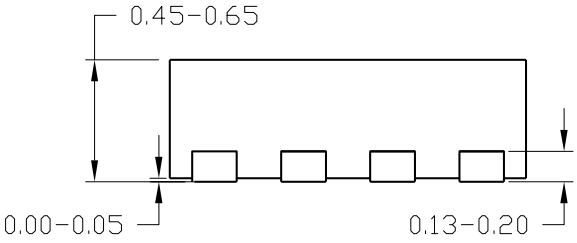
BOM List

Reference Designator	Description	Part Number	Manufacturer
U1	Dual 6A Ultra-Low Loss Smart Bridge	SY6827DFC	Silergy
C0	0.1uF/50V, 0603, X7R	0.1uF/50V, 0603, X7R	TDK
C11, C21	470uF/10V(electrolytic capacitor)		
C12, C13, C22, C23	22uF/6.3V, 0805, X5R	C2012X5R0J226M	TDK
C15, C25	10nF/50V, 0603, X7R	C1608X7R1H103K	
R11, R21	300kΩ, 1%, 0603		

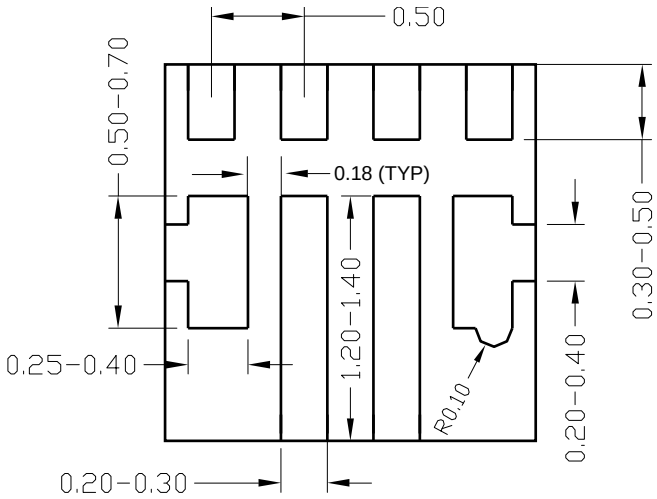
DFN2x2-8 (FC) Package Outline



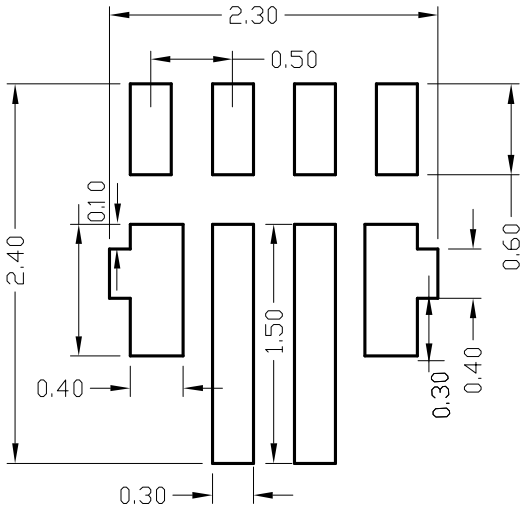
Top View



Side View



Bottom View

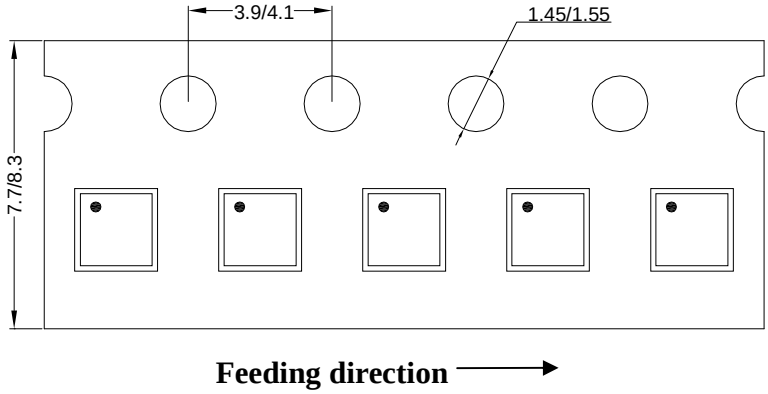


Recommended PCB

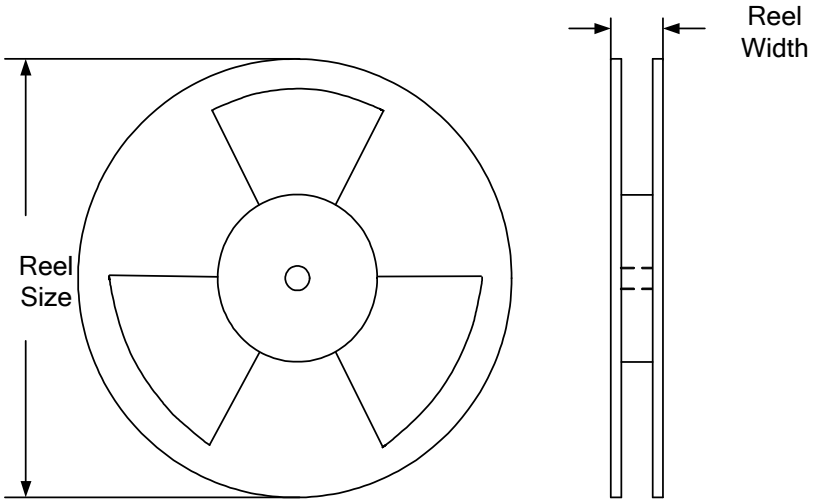
Notes: **All dimension in MM**
All dimension do not include mold flash & metal burr

Taping & Reel Specification

1. DFN2x2-8(FC) taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2x2	8	4	7"	8.4	400	160	3000

3. Others: NA