SY6827

Dual Channel 6A, Ultra Low Loss Smart Bridge

General Description

SY6827 is a dual 6A ultra-low loss Smart Bridge for the intelligent power distribution in the computers or portable electronics. It reduces the number of point of load regulators required in a system and minimizes the power consumption at standby mode. Tiny DFN2x2 package also minimizes the solution size and PCB cost. Programmable turn-on delay allows the proper power sequencing during the transition of different operation modes. Programmable ramp-up time minimizes the inrush current. Integrated over-temperature protection and short circuit protection improve the reliability of the overall system.

Ordering Information

SY6827 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6827DFC	DFN2x2-8	

Features

- Low $R_{DS(ON)}$ for internal bridge FET: 15mΩ
- Maximum output current per channel: 6A
- Distribution voltages: 0.6V~5.5V
- Compact Package: DFN2x2-8
- Programmable turn on delay
- Over-temperature protection
- Short circuit protection
- Programmable ramp-up time
- Automatic output discharge at shutdown
- Short circuit protection
- Thermal protection
- RoHS Compliant and Halogen Free

Applications

- Notebook PC or Tablet PC or Net PC
- Desktop PC
- Server
- Set Top Box
- E-Book or MID
- Smart TV
- Router
- Industrial PC

Typical Applications

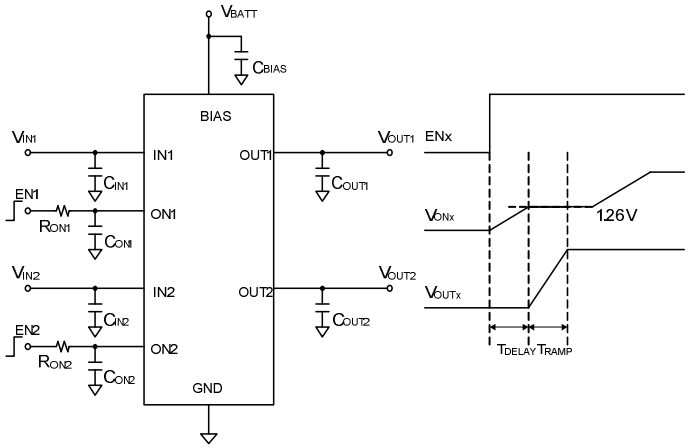
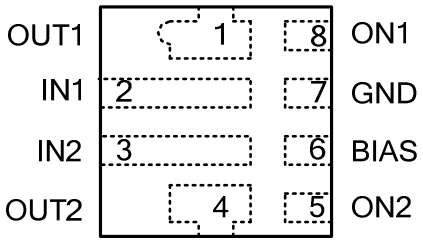


Figure 1. Schematic Diagram

Pinout (top view)



(DFN2x2-8)

Top mark: **EI*xyz*** for SY6827 (Device code: EI, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN1	2	Input pin for channel 1.
IN2	3	Input pin for channel 2.
GND	7	Ground pin
OUT1	1	Output pin for channel 1.
OUT2	4	Output pin for channel 2.
ON1	8	ON/OFF control pin for channel 1. When ON>0.6V, the internal bias is turned on. Connect this pin to RC circuit (as shown in Figure 1) to control the ramp-up time and turn on delay. The ramp-up time is controlled by R_{ON1}, and the delay is programmable by C_{ON1} and $R_{ON1.}$
ON2	5	ON/OFF control pin for channel 2. When ON>0.6V, the internal bias is turned on. Connect this pin to RC circuit (as shown in Figure 1) to control the ramp-up time and turn on delay. The ramp-up time is controlled by R_{ON2}, the delay time is programmable by C_{ON2} and $R_{ON2.}$
BIAS	6	Bias pin. Bias supply for overdriving the gate of the bridge between input and output. Recommend the BIAS voltage to be at least 3V above INx rails.

Absolute Maximum Ratings (Note 1)

BIAS Pin ---------- 30V
All other pins---------- ---------- 6V
Power Dissipation, PD @ TA = 25°C DFN2x2-8 FC, ---------- 2W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 62.5°C/W
θ_{JC} ---------- 10°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- 65°C to 150°C

Recommended Operating Conditions (Note 3)

IN, OUT ---------- 0.6V to 5.5V
BIAS---------- V_{IN}+3V to 28V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{BIAS}=12V,V_{IN} = 3.3V, T_A = 25°C unless otherwise specified)

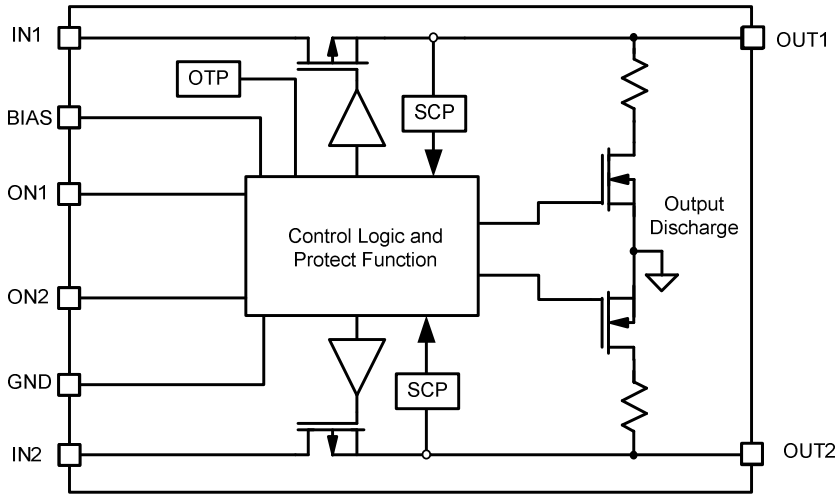
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		0.6		5.5	V
Bias Voltage Range	V_{BIAS}		V_{IN}+3		28	V
Bias current	I_{BIAS}	V_{ON}=3.3V, I_{OUT}=0		20		uA
Shutdown Bias Current	I_{SHDN}	V_{ON}=0		2		μA
FET RON	$R_{DS(ON)}$			15		mΩ
ON Clamping Threshold	Von,clp		1.16	1.26	1.36	V
(BIAS-IN) UVLO Threshold	$V_{BIAS-IN,UVLO}$				3	V
(BIAS-IN) UVLO Hysteresis	$V_{BIAS-IN,HYS}$			0.2		V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

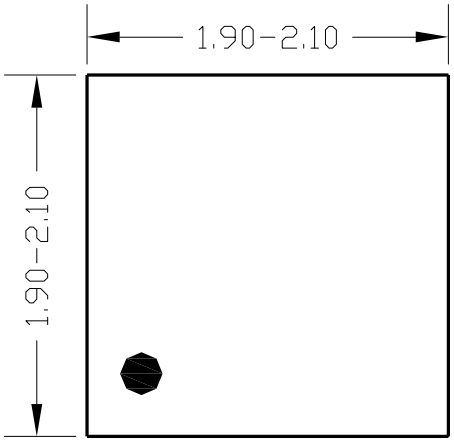
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. The device is not guaranteed to function outside its operating conditions

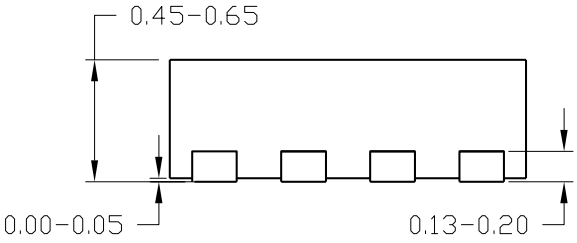
Block Diagram



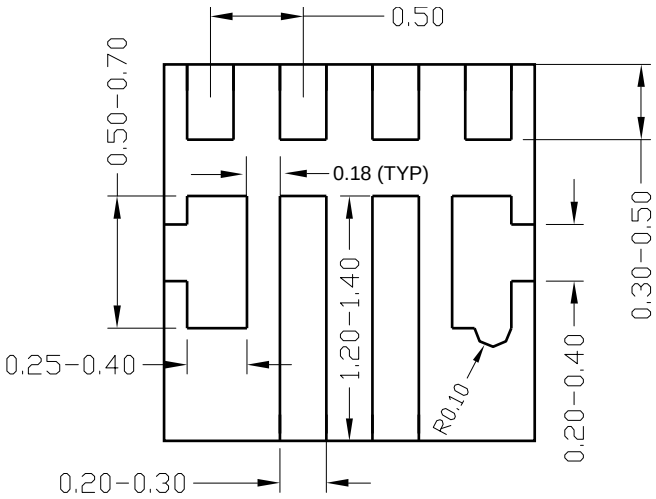
DFN2x2-8 (FC) Package Outline



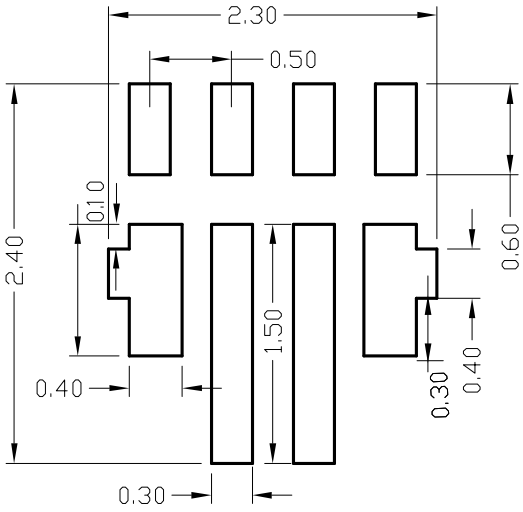
Top View



Side View



Bottom View

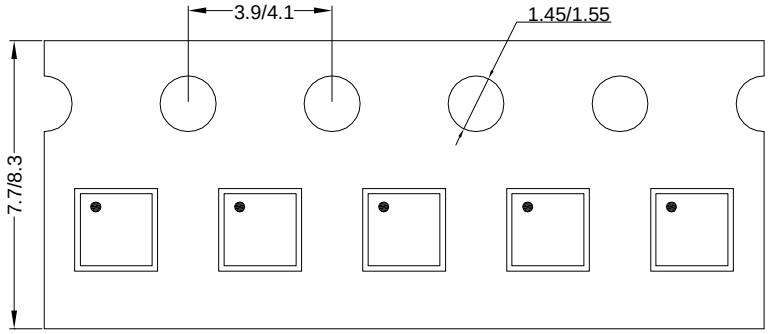


Recommended PCB

Notes: **All dimension in MM**
All dimension do not include mold flash & metal burr

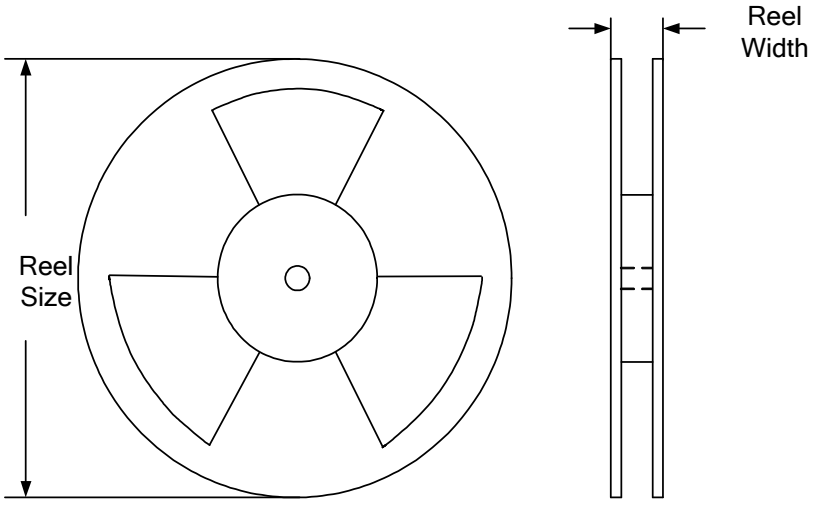
Taping & Reel Specification

1. DFN2x2-8(FC) taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2x2	8	4	7"	8.4	400	160	3000

3. Others: NA