Application Note: SY8286

High Efficiency Fast Response, 6A, 23V Input Synchronous Step Down Regulator

General Description

The SY8286 develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A continuous, 12A peak current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. SY8286 also integrates a bypass switch which allows the IC to be powered by external DC source.

The SY8286 operates over a wide input voltage range from 4V to 23V. The DC-DC regulator adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500kHz under heavy load conditions to minimize the size of inductor and capacitor. SY8286 is optimized for lower than 2.5V_{OUT} application

Ordering Information

SY8286 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8286RAC	QFN3×3-20	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 38/19 mΩ
- Wide Input Voltage Range: 4-23V
- Output Voltage Range: 0.6~2.5V
- External Bypass Input
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal 400μs Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 500kHz
- 6A Continuous/12A Peak Output Current Capability
- ±1.0% 0.6V Reference
- Programmable Valley Current Limit
- Power Good Indicator
- Output Discharge Function
- Short Circuit Latch Off Protection
- Over Voltage Latch Off Protection
- Thermal Shutdown
- Input UVLO
- RoHS Compliant and Halogen Free
- Compact package: QFN3×3-20

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

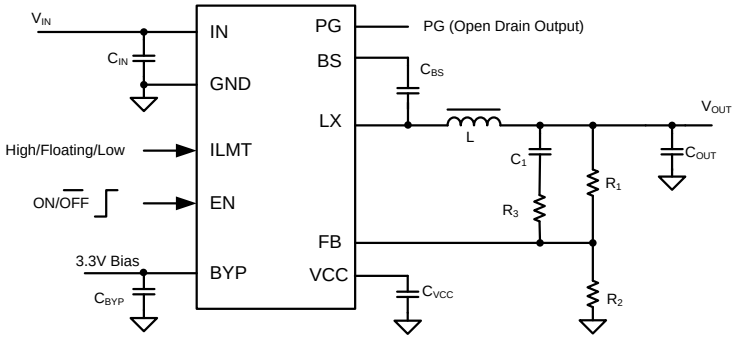
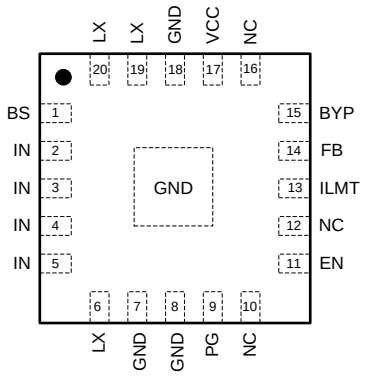


Figure1 Schematic

Pinout (top view)



(QFN3×3-20)

Top Mark: BAA*xyz*, (Device code: BAA, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Decouple this pin to the LX pin with a 0.1μF ceramic capacitor.
IN	2,3,4,5	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
LX	6,19,20	Inductor pin. Connect this pin to the switching node of the inductor.
GND	7,8,18,EP	Ground pin.
PG	9	Power good Indicator. Open drain output when the output voltage is within 90% to 120% of regulation point.
EN	11	Enable pin. Pull this pin high to turn on the IC. Do not leave this pin floating.
NC	10,12,16	Not connected.
ILMT	13	Output current limit threshold selection.
FB	14	Output feedback pin. Connect to the center point of the resistor divider.
BYP	15	External 3.3V bypass power supply input. Decouple this pin to GND with a 1μF ceramic capacitor. Leave this pin floating if it is not used.
VCC	17	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with a 2.2μF ceramic capacitor.

Block Diagram

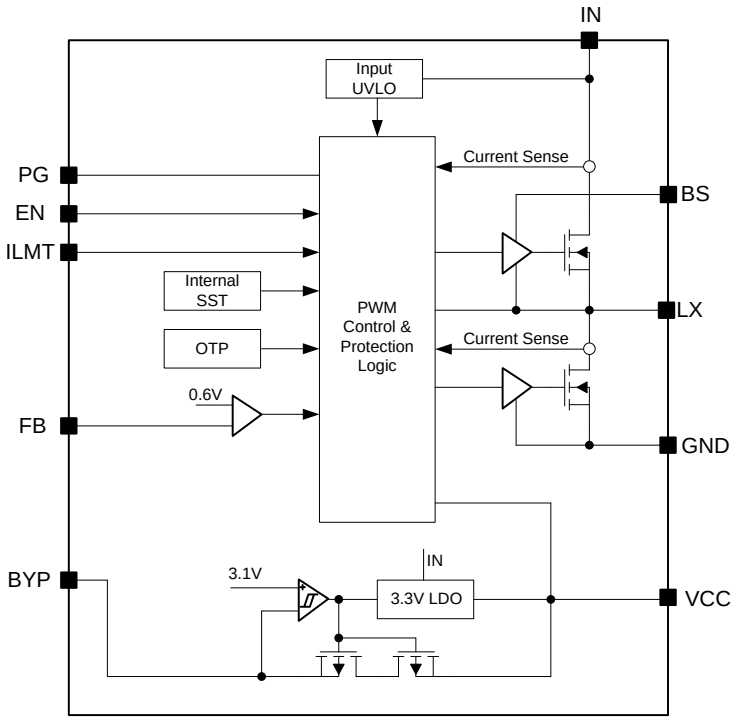


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, LX, PG ---------- 25V
BS-LX ---------- 4V
EN, ILMT ---------- 25V
FB, VCC ---------- 4V
BYP ---------- 6V
Power Dissipation,
P_D @ T_A = 25℃ QFN3×3-20 ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA}, QFN3×3-20 ---------- 30℃/W
θ_{JC}, QFN3×3-20 ---------- 4.5℃/W
Junction Temperature Range ---------- 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃
Dynamic LX voltage in 10ns duration ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 23V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 12V, C_{OUT} = 100uF, T_A = 25℃, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.0		23	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		120	140	μA
Shutdown Current	I_{SHDN}	EN=0		6	10	μA
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET R_{ON}	$R_{DS(ON)1}$			38		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			19		mΩ
Output Discharge Current	I_{DIS}			100		mA
Top FET Current Limit	$I_{LMT,TOP}$		18	20	22	A
Bottom FET Current Limit	$I_{LIM,BOT}$	ILMT='0'	6.5	7.5	8.5	A
		ILMT=Floating	9.5	10.5	11.5	
		ILMT='1'	12.5	13.5	14.5	
ILMT Rising Threshold	V_{ILMTH}		Vcc-0.8			V
ILMT Falling Threshold	V_{ILMTL}				0.8	V
Soft-start Time	t_{SS}			400		μs
EN Rising Threshold	V_{ENH}		0.8			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				3.9	V
UVLO Hysteresis	V_{HYS}			0.3		V
Oscillator Frequency	F_{OSC}		425	500	575	kHz
Min ON Time	$t_{ON,MIN}$	V_{IN}=V_{INMAX}		50		ns
Min OFF Time	$t_{OFF,MIN}$			200		ns
VCC Output	V_{CC}	V_{IN}=4V	3.2	3.3	3.4	V
Output Over Voltage Protection Threshold		V_{FB} Rising	115	120	125	%V_{REF}
Output Over Voltage Protection Hysteresis				5		%V_{REF}
Output OVP Delay				20		μs
Output Under Voltage Protection Threshold			55	60	65	%V_{REF}
Output UVP Delay				200		us
Power Good Threshold		V_{FB} Rising (Good)	88	90	92	%V_{REF}
Power Good Hysteresis				5		%V_{REF}
Power Good Delay		Low to high		200		μs
		High to low		10		μs
Bypass Switch R_{ON}	R_{BYP}			1		Ohm
Bypass Switch Turn-on Voltage	$V_{BYP,ON}$		2.97	3.1		V
Bypass Switch Switchover Hysteresis	$V_{BYP,HYS}$			0.2		V
Bypass Switch OVP				120		%V_{CC}
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

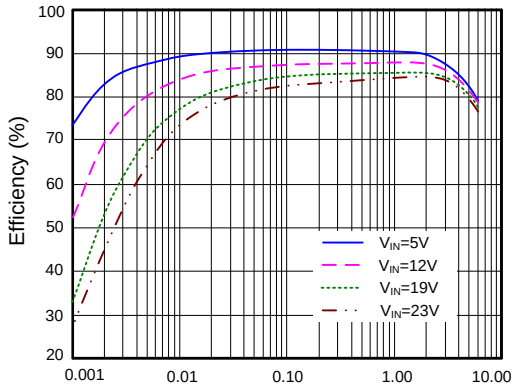
Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

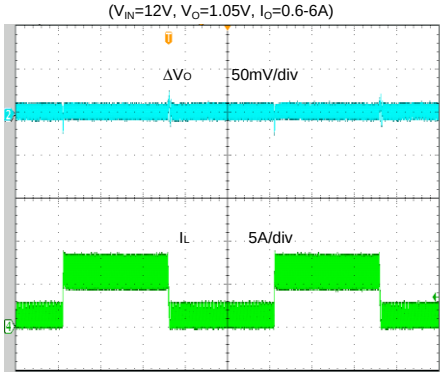
Efficiency vs. Load Current

(Vo=1.05V)



Load Transient

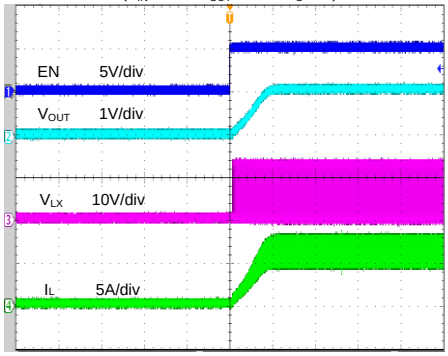
(V_{IN}=12V, V_O=1.05V, I_O=0.6-6A)



Time (200μs/div)

Startup from Enable

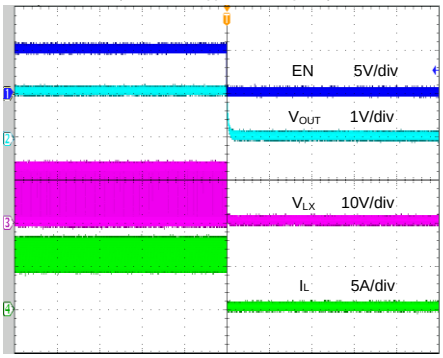
(V_{IN}=12V, V_{OUT}=1.05V, I_O=6A)



Time (800μs/div)

Shutdown from Enable

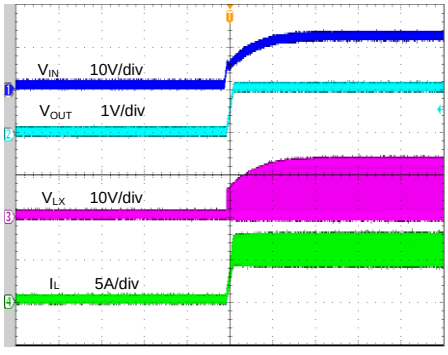
(V_{IN}=12V, V_{OUT}=1.05V, I_O=6A)



Time (800μs/div)

Startup from VIN

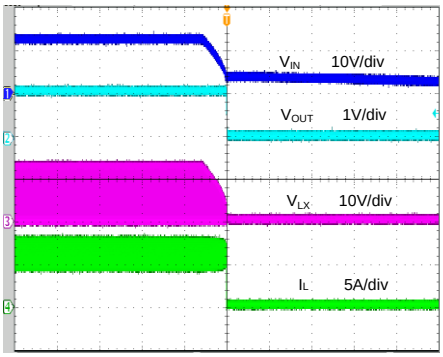
(V_{IN}=12V, V_{OUT}=1.05V, I_O=6A)



Time (4ms/div)

Shutdown from VIN

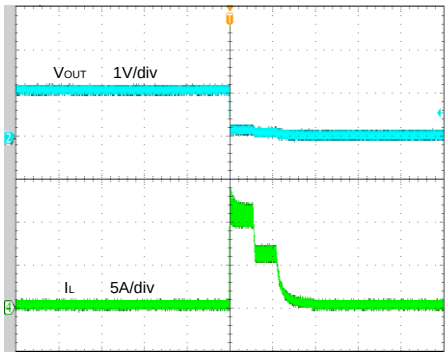
(V_{IN}=12V, V_{OUT}=1.05V, I_O=6A)



Time (4ms/div)

Short Circuit Protection

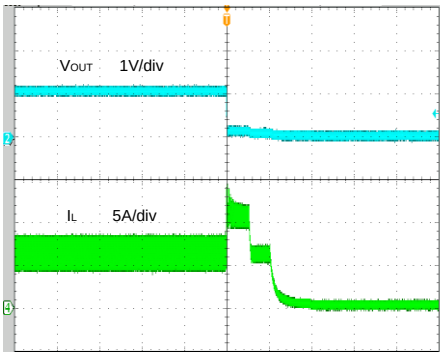
(V_{IN}=12V, V_{OUT}=1.05V, 0A to Short)



Time (200μs/div)

Short Circuit Protection

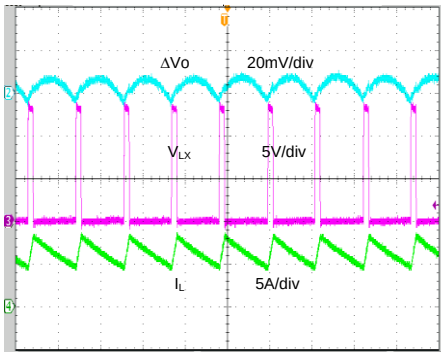
(V_{IN}=12V, V_{OUT}=1.05V, 6A to Short)



Time (200μs/div)

Output Ripple

(V_{IN}=12V, V_O=1.05V, I_O=6A)



Time (2μs/div)

Operation

The SY8286 develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A continuous, 12A peak current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. SY8286 also integrates a bypass switch which allows the IC to be powered by external DC source.

The SY8286 operates over a wide input voltage range from 4V to 23V. The DC-DC regulator adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500kHz under heavy load conditions to minimize the size of inductor and capacitor.

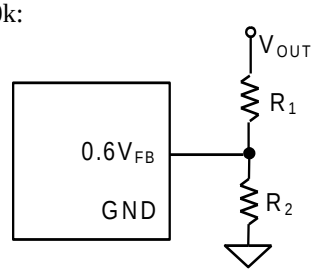
Applications Information

Because of the high integration in the SY8286 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If Vout is 1.2V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 100k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input Capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} \cdot$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For most applications, an X5R or better grade ceramic capacitor greater than 66μF capacitance can work well. The capacitance derating with DC voltage must be considered.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8286 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Current Limit Setting

The current limit is set to 6A, 9A or 12A when ILMT pin is pull low, floating or pull high respectively.

Soft-start

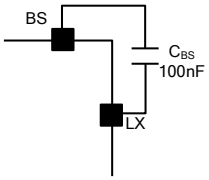
The SY8286 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC start-up. The typical soft-start time is 400μs.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY8286 shutdown current drops to lower than 10uA, Driving the EN pin high (>0.8V) will turn on the IC again.

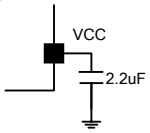
External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



VCC LDO

The 3.3V VCC LDO provides the power supply for internal control circuit. Bypass this pin to ground with a 2.2uf ceramic capacitor.



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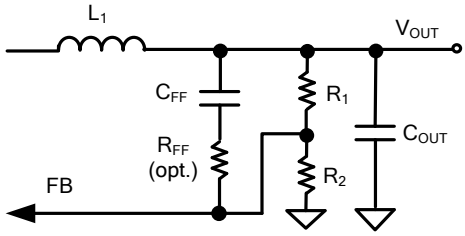
Power Good Indication

PG is an open-drain output pin. This pin will pull to ground if output voltage is lower than 90% of regulation voltage. Otherwise this pin will go to a high impedance state.

Load Transient Considerations:

The SY8286 regulator IC adopts the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC network R_{FF} and C_{FF} parallel with R1 may further speed up the load transient responses.



Layout Design:

The layout design of SY8286 regulator is relatively simple. For the best efficiency and minimum noise promblem, we should place the following components close to the IC: C_{IN}, C_{VCC}, L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

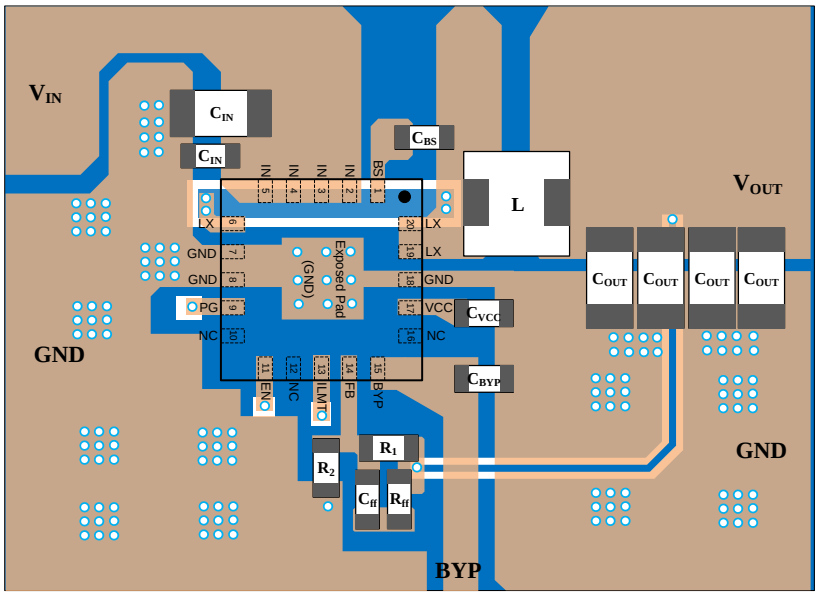
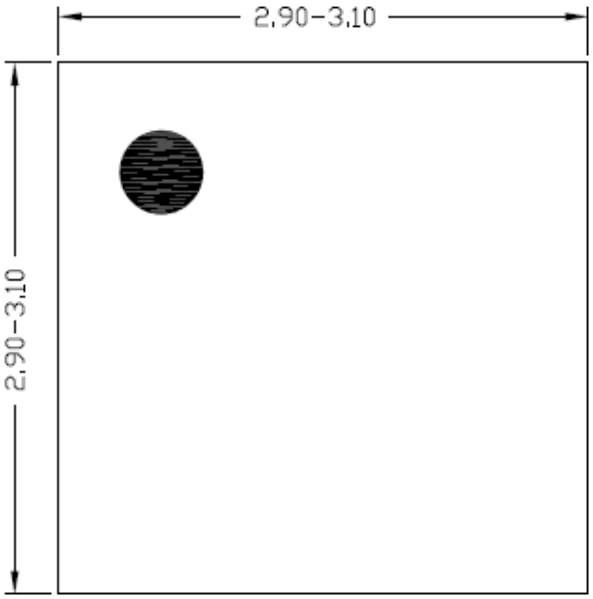
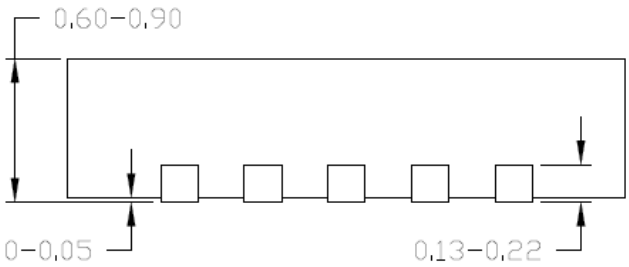


Figure3. PCB Layout Suggestion

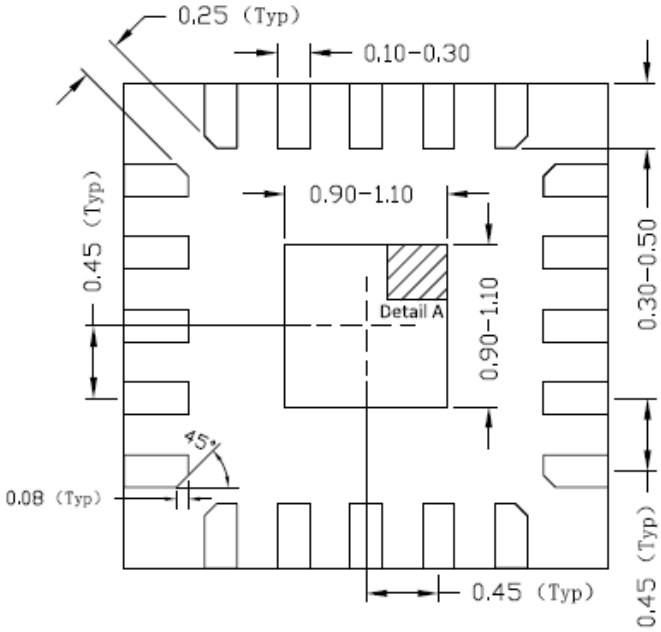
QFN3×3-20 Package Outline

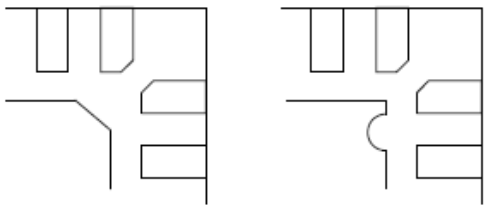


Top view



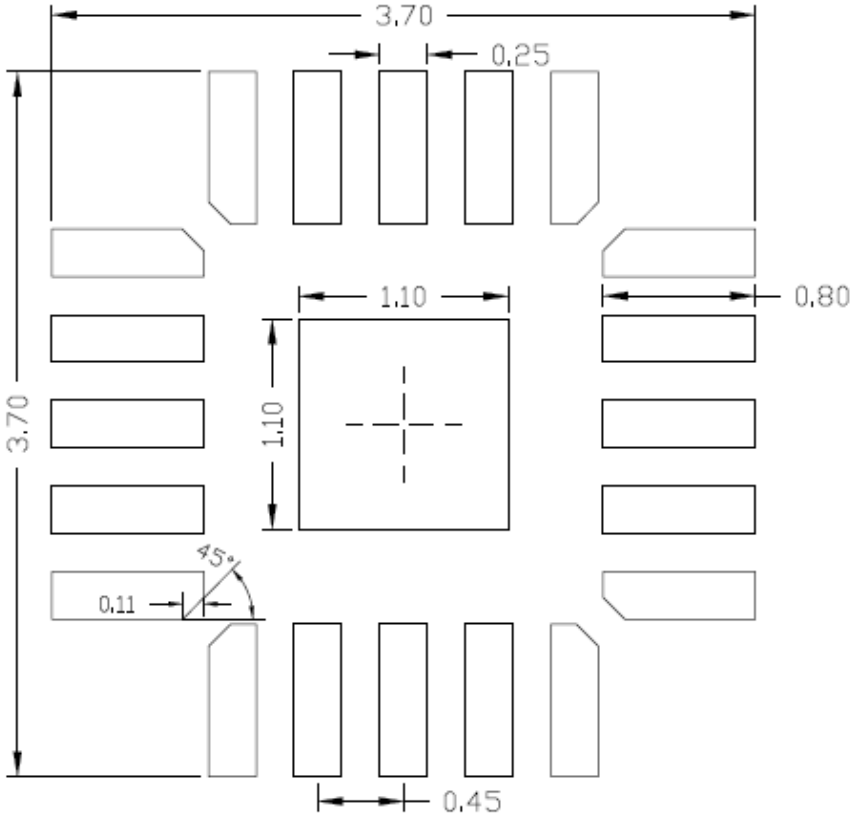
Side view





Detail A
Pin1 Identifier: two options

Bottom view

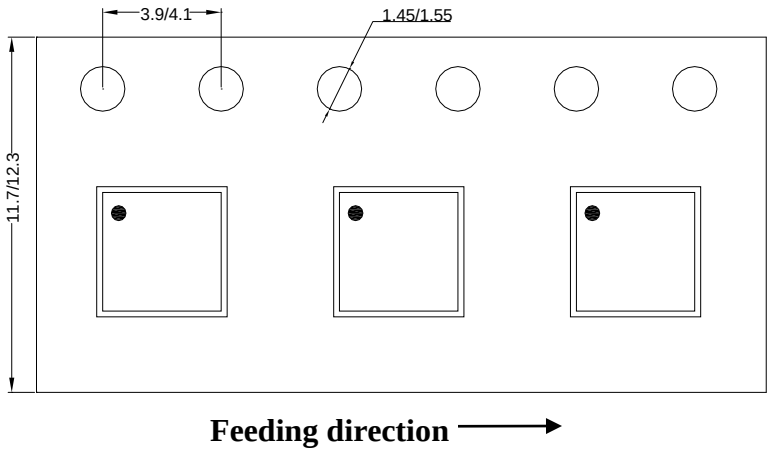


Recommended PCB layout
(Reference only)

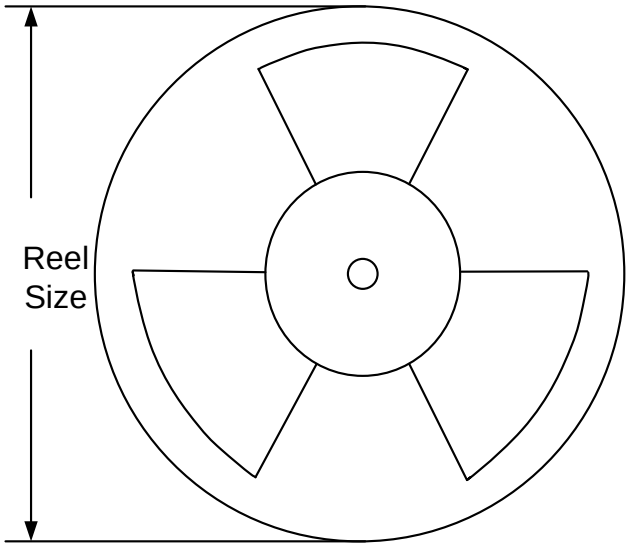
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. QFN3×3-20 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA

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