Application Notes: SY8286C

High Efficiency Fast Response, 6A, 23V Input Synchronous Step Down Regulator

General Description

The SY8286C develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8286C has a fixed 5V DC/DC output and integrates a 5V 100mA LDO with bypass switch and individual enable control.

The SY8286C operates over a wide input voltage range from 5.5V to 23V. The DC/DC regulator adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 600kHz under heavy load conditions to minimize the size of inductor and capacitor.

Ordering Information

SY8286 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8286CRAC	QFN3x3-20	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 38/19 mΩ
- Wide Input Voltage Range: 5.5-23V
- 5V LDO with Individual Enable Control and Bypass Switch
- Integrated Bypass Switch: 1.5Ω
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal 1.2ms Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 600kHz.
- 6A Output Current Capability
- +/-1.5% Output Voltage Accuracy
- Power Good Indicator
- Output Discharge Function
- Output Current Limit Protection
- Short Circuit Latch Off Protection
- Output Over Voltage Latch Off Protection
- Input UVLO
- Over Temperature Protection
- RoHS Compliant and Halogen Free
- Compact Package: QFN3x3-20

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

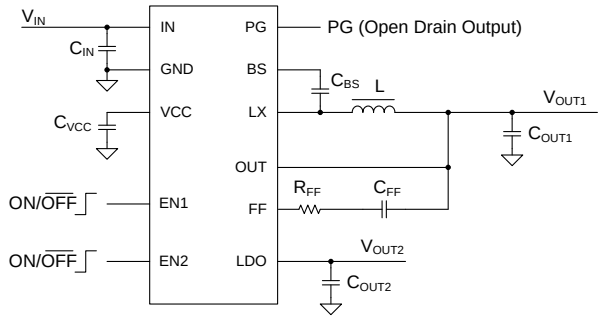


Figure1. Schematic

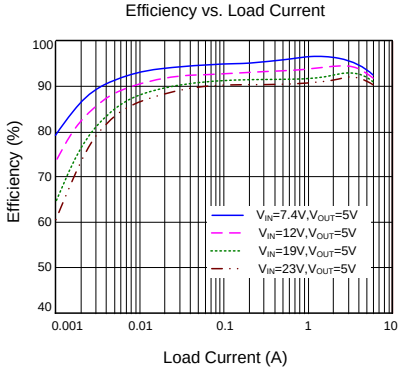
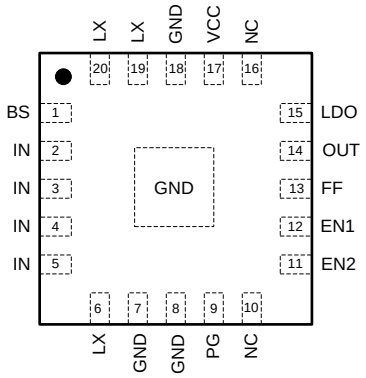


Figure2. Efficiency vs. Load Current

Pinout (top view)



(QFN3x3-20)

Top Mark: AWW***xyz***, **(**Device code: AWW, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Decouple this pin to LX pin with a 0.1μF ceramic capacitor.
IN	2,3,4,5	Input pin. Decouple this pin to GND pin with at least a 10μF ceramic cap.
LX	6,19,20	Inductor pin. Connect this pin to the switching node of inductor.
GND	7,8,18,EP	Ground pin.
PG	9	PG is an open-drain output pin. This pin is externally pulled high when the output voltage is within 90% to 120% of regulation voltage range. Otherwise this pin is internally pull low.
NC	10,16	Not connected.
EN2	11	Enable control of the IC and internal LDO. Pull this pin high to turn on the IC and internal LDO. Do not leave this pin floating.
EN1	12	Enable control of the DC/DC regulator. Pull this pin high to turn on the regulator. Do not leave this pin floating.
FF	13	Output feed forward pin. Connect RC network from the output to this pin.
OUT	14	Output pin. Connect to the output of DC/DC regulator. The pin also provides the bypass input for internal LDO.
LDO	15	5V LDO output. Decouple this pin to ground with at least a 4.7μF capacitor.
VCC	17	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with a 2.2μF ceramic capacitor.

Block Diagram

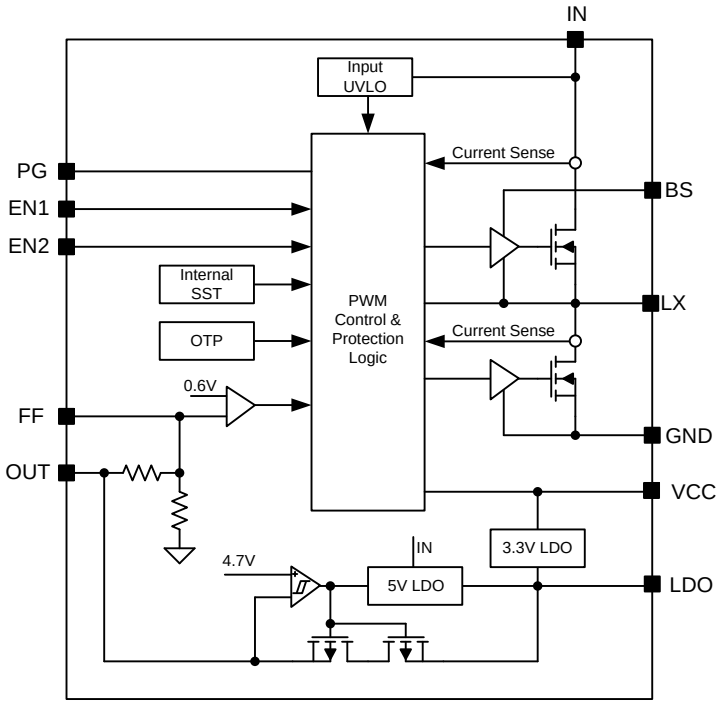


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, LX, PG ---------- 25V
BS-LX ---------- 4V
EN1, EN2 ---------- 25V
VCC ---------- 4V
LDO ---------- 6V
OUT ---------- 6V
FF ---------- 6V
Power Dissipation,
P_D @ T_A = 25℃ QFN3x3-20 ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA}, QFN3x3-20 ---------- 30℃/W
θ_{JC}, QFN3x3-20 ---------- 4.5℃/W
Junction Temperature Range ---------- 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃
Dynamic LX Voltage in 10ns Duration ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 5.5V to 23V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 12V, C_{OUT} = 100μF, T_A = 25℃, I_{OUT} = 1A, unless otherwise specified)

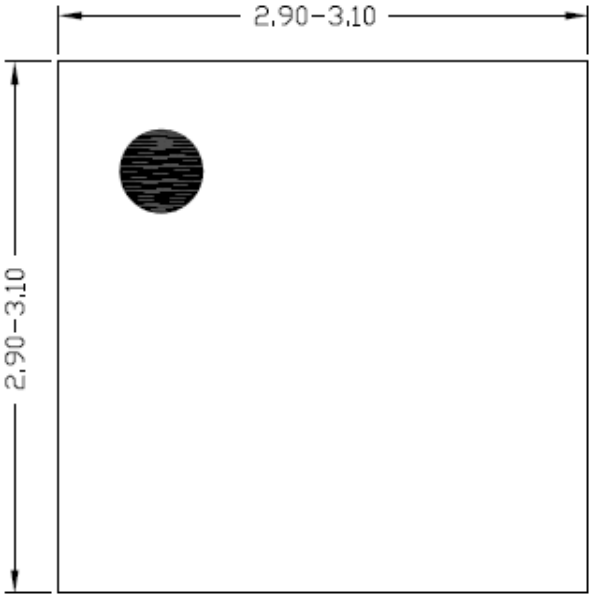
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		5.5		23	V
Quiescent Current	I_Q	I_{OUT}=0, V_{OUT}=V_{SET}×105%		108	145	μA
Shutdown Current 1	I_{SHDN1}	EN1=0, EN2=1		59	70	μA
Shutdown Current 2	I_{SHDN2}	EN1=0, EN2=0		6	10	μA
Output Voltage Set-point	V_{SET}		5.023	5.1	5.177	V
Top FET RON	$R_{DS(ON)1}$			38		mΩ
Bottom FET RON	$R_{DS(ON)2}$			19		mΩ
Output Discharge Current	I_{DIS}			70		mA
HSFET FET Current Limit	$I_{LMT,HSFET}$		12			A
Bottom FET Current Limit	$I_{LMT,LSFET}$		8			A
Soft-start Time	t_{SS}			1.2		ms
EN Rising Threshold	V_{ENH}		1			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				5	V
UVLO hysteresis	V_{HYS}			0.3		V
Switching Frequency	F_{OSC}		510	600	690	kHz
Min ON Time	$T_{ON,MIN}$	V_{IN}=V_{INMAX}		50		ns
Min OFF Time	$T_{OFF,MIN}$			150		ns
VCC Output	V_{CC}	V_{IN}=4V	3.2	3.3	3.4	V
Output Over Voltage Threshold		V_{OUT} rising	115	120	125	%V_{SET}
Output Over Voltage Hysteresis				2		% V_{SET}
Output OVP Delay				20		μs
Output Under Voltage Protection Threshold			45	50	55	% V_{SET}
Output UVP Delay				200		us
Power Good Threshold	V_{PG}	V_{FB} rising (good)	80	84	88	% V_{REF}
Power Good Hysteresis	$V_{PG, HYS}$			2		% V_{REF}
Power Good Delay	$t_{PG, RISING}$	Low to high		200		μs
	$t_{PG, FALLING}$	High to low		10		μs
LDO Output Voltage	V_{LDO}	V_{IN}=12V， no load	4.85	5	5.15	V
LDO Dropout Voltage	$V_{DROPOUT}$	I_{LDO}=100mA		200		mV
LDO Output Current Limit	I_{LMTLDO}		150		300	mA
Bypass Switch RON	R_{BYP}			1.5		Ω
Bypass Switch Turn-on Voltage	V_{BYP}		4.5	4.7	4.9	V
Bypass Switch Switchover Hysteresis				0.2		V
Bypass Switch OVP				120		%V_{LDO}
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

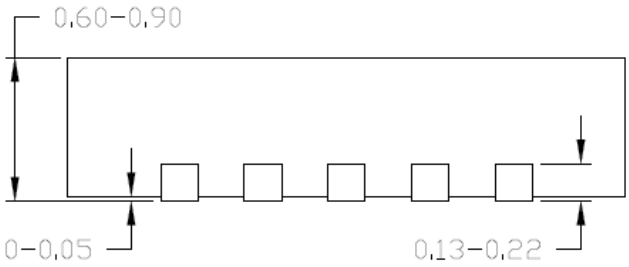
Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

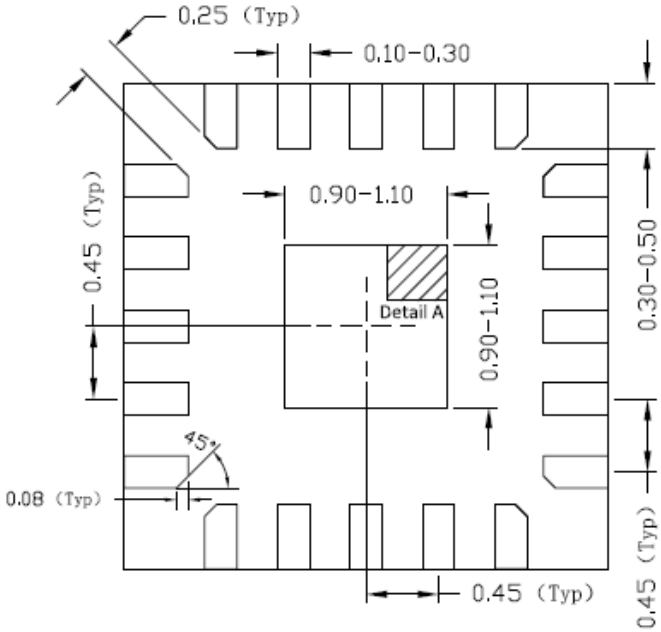
QFN3×3-20 Package Outline



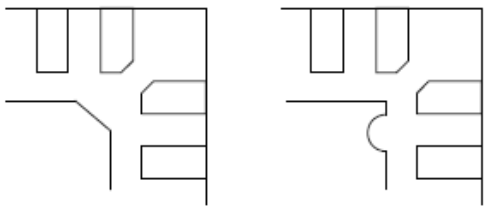
Top view



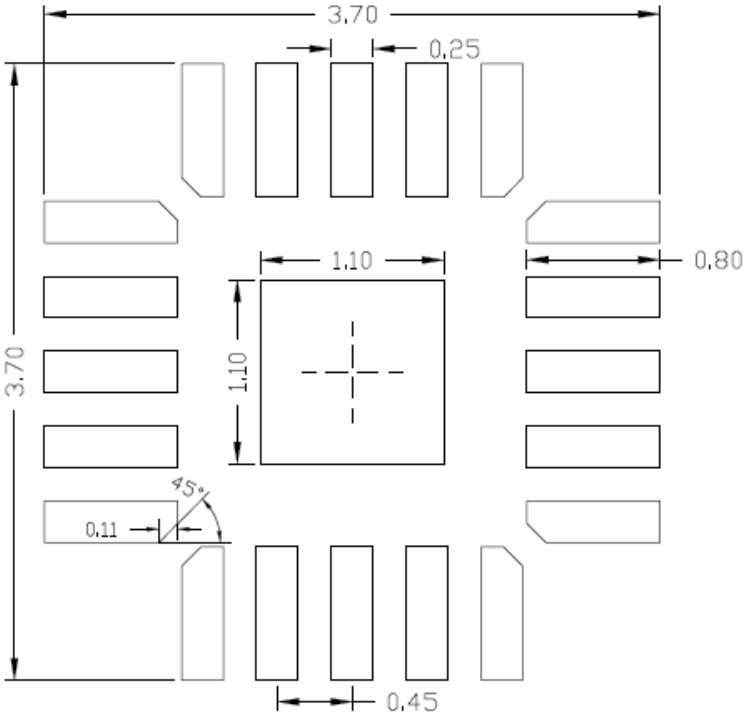
Side view



Bottom view



Detail A
Pin1 Identifier: two options

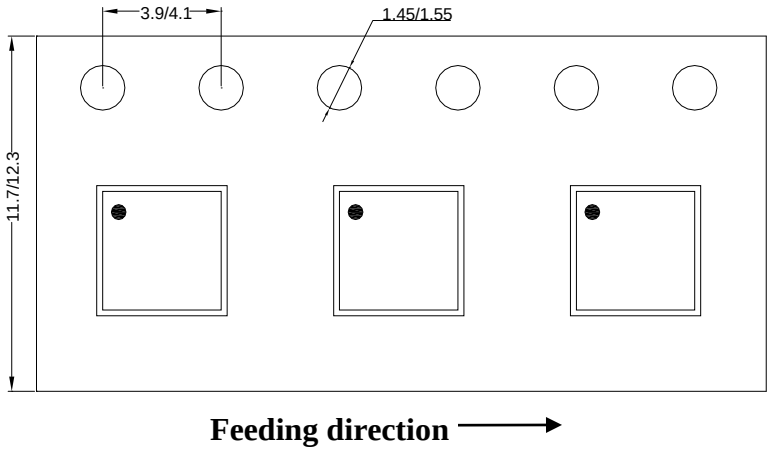


Recommended PCB layout
(Reference only)

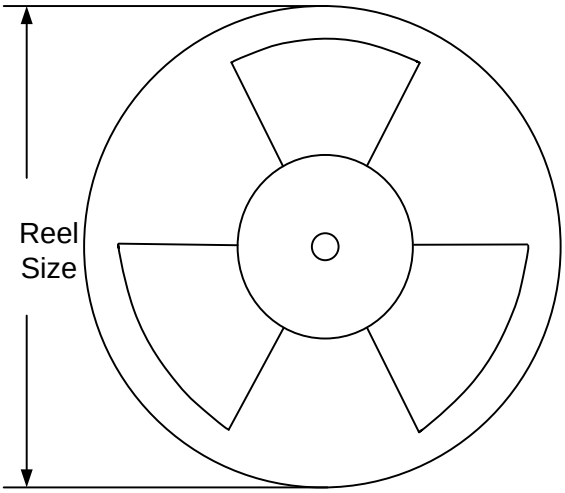
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. QFN3×3-20 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA