

## Low Capacitance TVS Protection

### Features

 Transient protection for high-speed data lines IEC 61000-4-2 (ESD) ±30kV (Air) ±30kV (Contact)

IEC 61000-4-5 (Surge) 7.5A (8/20µs)

- Small package (2.9mm × 2.4mm × 1.0mm)
- Protects two data lines
- Low capacitance: 1.2pF Typical (I/O-GND)
- Low leakage current: 0.01µA @ V<sub>RWM</sub> (Typical)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge

## Description

SYT04L05AWC is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 1.2pF only, SYT04L05AWC is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD) (±30kV air, ±30kV contact discharge), IEC 61000-4-5 (Surge) (7.5A, 8/20µs), etc.

SYT04L05AWC uses small SOT-143 package. Each SYT04L05AWC device can protect two high-speed data lines. The combined features of low capacitance, small size and high ESD robustness make SYT04L05AWC ideal for high-speed data ports and high-frequency lines (e.g., VGA) applications. The low clamping voltage of the SYT04L05AWC guarantees a minimum stress on the protected IC.

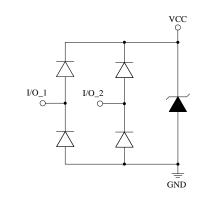
## Applications

- Desktops, Servers and Notebooks
- USB2.0 Power and Data Line Protection
- IEEE 1394 Firewire Ports
- Video Graphics Cards
- SIM Ports

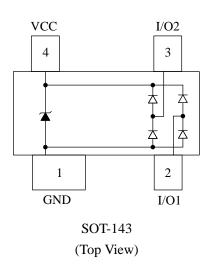
## **Mechanical Characteristics**

- SOT-143 package
- Marking: Device code, Date code
- Packaging: Tape and Reel

# Circuit Diagram



# **Pin Configuration**



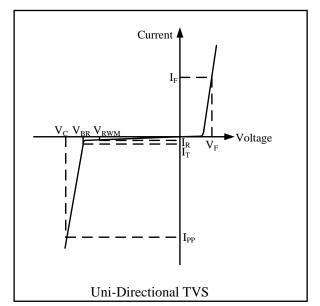


# **Absolute Maximum Rating**

Symbol	Parameter	Value	Units	
I <sub>PP</sub>	Maximum Peak Pulse Current (8/20µs)	7.5	А	
P <sub>PK</sub>	Maximum Peak Pulse Power (8/20µs)	100	Watts	
V <sub>ESD</sub>	ESD per IEC 61000-4-2 (Air)	±30	kV	
	ESD per IEC 61000-4-2 (Contact)	±30		
T <sub>OPT</sub>	Operating Temperature	-40/+125	°C	
T <sub>STG</sub>	Storage Temperature	-55/+150	°C	

# Electrical Characteristics ( $T_A = 25^{\circ}C$ )

Symbol	Parameter	
V <sub>RWM</sub>	Nominal Reverse Working Voltage	
I <sub>R</sub>	Reverse Leakage Current @ V <sub>RWM</sub>	
V <sub>BR</sub>	Reverse Breakdown Voltage @ $I_T$	
I <sub>T</sub>	Test Current for Reverse Breakdown	
V <sub>C</sub>	Clamping Voltage @ IPP	
$I_{PP}$	Maximum Peak Pulse Current	
C <sub>ESD</sub>	Parasitic Capacitance	
V <sub>R</sub>	Reverse Voltage	
f	Small Signal Frequency	
$I_{\rm F}$	Forward Current	
$V_{\rm F}$	Forward Voltage @ I <sub>F</sub>	



Symbol	Test Condition	Minimum	Typical	Maximum	Units
V <sub>RWM</sub>				5.0	V
I <sub>R</sub>	$V_{RWM} = 5V, T_A = 25^{\circ}C$ From I/O to GND		0.01	0.1	μΑ
$V_{\text{BR}}$	$I_T = 1 mA$ From I/O to GND	6.0	8.0	10.0	V
$V_{\rm F}$	$I_F = 1 m A$ From GND to I/O	0.4	0.7	1.2	V
$Vc^1$	$I_{PP} = 7.5A$ , $t_p = 8/20\mu s$ From I/O to GND		12.5	13.5	V
$Vc^1$	$I_{PP} = 16A$ , $t_p = 10/100$ ns From I/O to GND		12		V
$R_{DYN}^{1,2}$	$t_p = 10/100$ ns From I/O to GND		0.25		Ω
$C_{ESD}^{1}$	$V_R = 2.5V, f = 1MHz$ From I/O to GND		1.20	1.50	pF
$C_{ESD}^1$	$V_R = 2.5V, f = 1MHz$ Between I/O and I/O		0.60	0.75	pF

#### NOTES

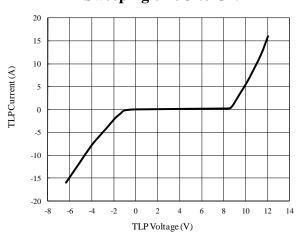
<sup>1</sup>Guaranteed by design and not subject to production test.

 $^2R_{\rm DYN}$  calculated based on Ipp=8A to Ipp=16A,  $t_p$  = 10/100ns.

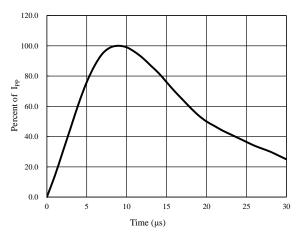
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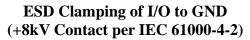


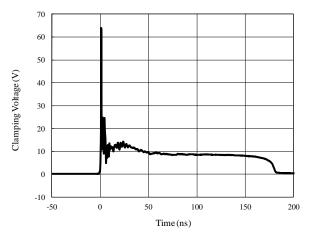
TLP Sweeping of I/O to GND



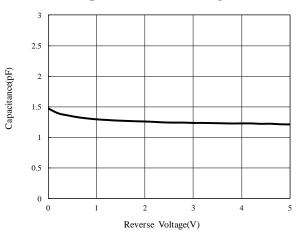
**Pulse Waveform** 



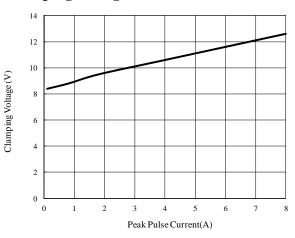




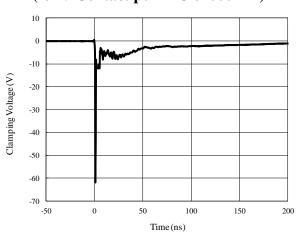
**Capacitance vs. Voltage** 



**Clamping Voltage vs. Peak Pulse Current** 



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)





## **Application Information**

#### **Pin Connection in PCB**

SYT04L05AWC is capable to provide ESD protection for two data lines simultaneously. The pin connection is shown in Figure 1.

Two parallel data lines, from inner IC to I/O port connector, could connect to SYT04L05AWC two I/O pins directly. Pin 1 of SYT04L05AWC is the negative reference pin, which should connect to the GND of PCB. The connection wires should be as short as possible in order to minimize the parasitic inductance.

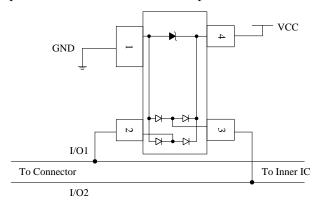


Figure 1 SYT04L05AWC pin connection in PCB

# PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- SYT04L05AWC GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting SYT04L05AWC VCC & GND pins to the PCB VCC & GND should be wide.
- Place SYT04L05AWC as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

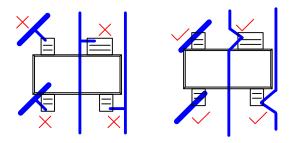
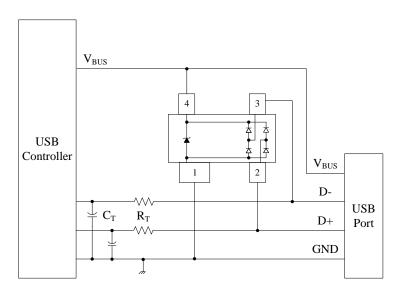


Figure 2 SYT04L05AWC Layout Guideline

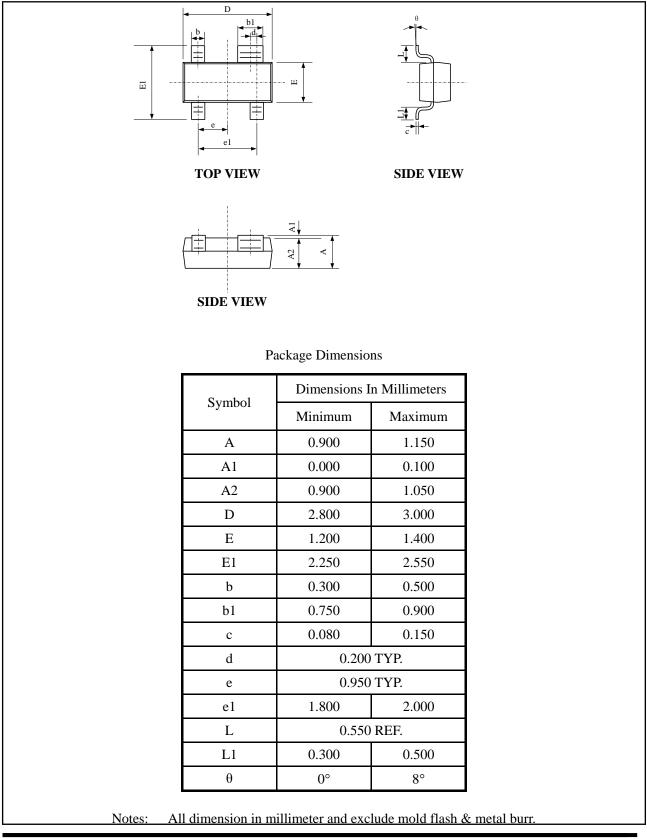


#### **Universal Serial Bus ESD Protection**



## **Package Outline**

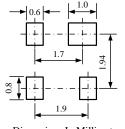
SOT-143 package •



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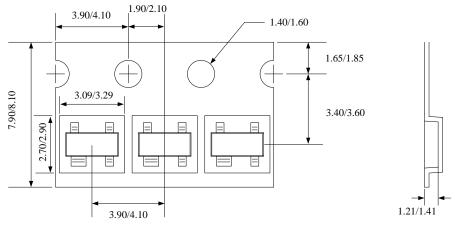


# **PCB Layout Pattern**



Dimensions In Millimeters

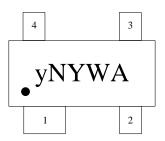
# **Tape and Reel Specification**



Feeding direction

Package types	Tape width	Pocket pitch	Reel size	Qty per reel
	(mm)	(mm)	(Inch)	(pcs)
SOT-143	8	4	7"	3000

## **Marking Codes**



# **Ordering Information**

Part Number	Working	Quantity	Reel
	Voltage	Per Reel	Size
SYT04L05AWC	5V	3,000	7 Inch

#### Note:

- (1) "yN" is device code, fixed.
- (2) "YWA" is date code.



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