

### Features

- Transient protection for high-speed data lines  
IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (Air)  
 $\pm 30\text{kV}$  (Contact)  
IEC 61000-4-5 (Surge) 50A (8/20 $\mu\text{s}$ )
- Package optimized for high-speed lines
- Provides protection for two line pairs
- Low capacitance: 1.2pF @ 3.0V (Typical)
- Low leakage current: 0.01 $\mu\text{A}$  @  $V_{\text{RWM}}$  (Typical)
- Low operating and clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for  $\pm 8\text{kV}$  contact discharge

### Description

SYS42L02FAC is an ultra low-capacitance Transient Voltage Suppressor (TVS) array designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 1.2pF only, SYS42L02FAC is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD,  $\pm 30\text{kV}$  air,  $\pm 30\text{kV}$  contact discharge), IIEC 61000-4-5 (Surge) (50A, 8/20 $\mu\text{s}$ ), etc.

SYS42L02FAC is in an SOP-8 package. Each SYS42L02FAC device can protect two high-speed line pairs. The “flow-thru” design minimizes trace inductance and reduces voltage overshoot associated with ESD events. The combined features of low capacitance and high ESD robustness make SYS42L02FAC ideal for high-speed data port and high-frequency line (e.g., Gigabit Ethernet Ports) applications. The low clamping voltage of the SYS42L02FAC guarantees a minimum stress on the protected IC.

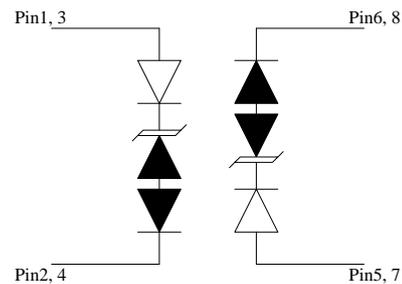
### Applications

- 10/100/1000M Ethernet Ports
- WAN/LAN Equipment
- Desktops, Servers and Notebooks
- Cellular Phones
- Switching Systems
- Audio/Video Inputs

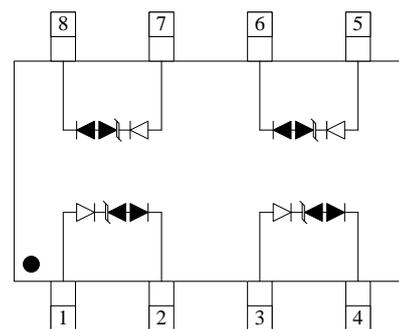
### Mechanical Characteristics

- SOP-8 package
- Marking: Device code, date
- Packaging: Tape and Reel

### Circuit Diagram



### Pin Configuration



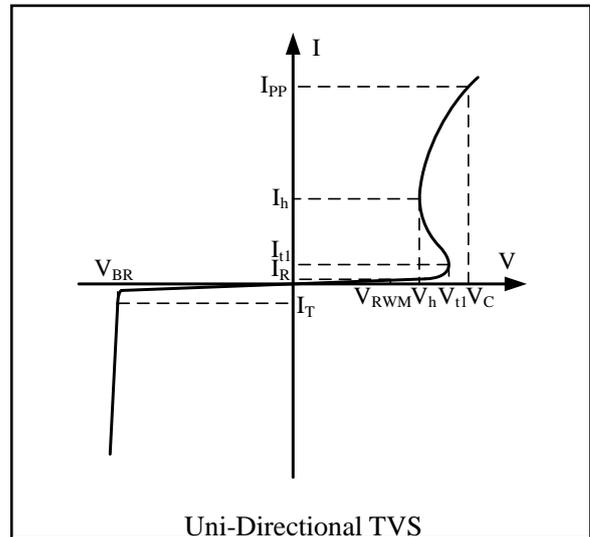
SOP-8  
(Top View)

**Absolute Maximum Rating**

Symbol	Parameter	Value	Units
$I_{PP}$	Peak Pulse Current (8/20 $\mu$ s)	50	A
$P_{PK}$	Peak Pulse Power (8/20 $\mu$ s)	1000	Watts
$V_{ESD}$	ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	$\pm 30$ $\pm 30$	kV
$T_{OPT}$	Operating Temperature	-55 to +125	$^{\circ}$ C
$T_{STG}$	Storage Temperature	-55 to +150	$^{\circ}$ C
$T_{LST}$	Lead Soldering Temperature	260 (10 seconds)	$^{\circ}$ C

**Electrical Characteristics ( $T_A = 25^{\circ}$ C)**

Symbol	Parameter
$V_{RWM}$	Nominal Reverse Working Voltage
$I_R$	Reverse Leakage Current @ $V_{RWM}$
$V_{t1}$	Trigger Voltage
$I_{t1}$	Trigger Current @ $V_{t1}$
$V_h$	Holding Voltage
$I_h$	Holding Current @ $V_h$
$V_C$	Clamping Voltage @ $I_{PP}$
$I_{PP}$	Maximum Peak Pulse Current
$V_{BR}$	Breakdown Voltage @ $I_T$
$C_{ESD}$	Parasitic Capacitance

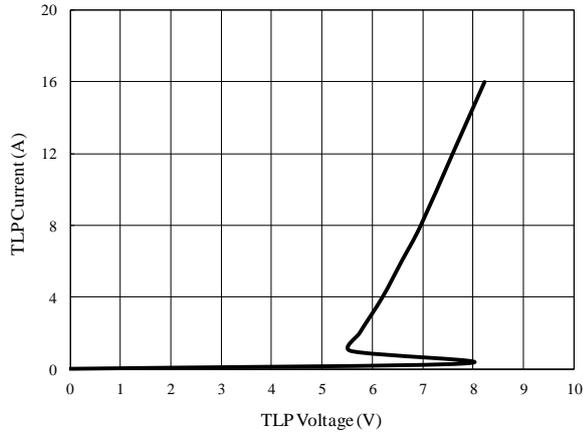


Symbol	Test Condition	Minimum	Typical	Maximum	Units
$V_{RWM}$				2.8	V
$I_R$	$V_{RWM} = 2.8V, T_A = 25^{\circ}C$		0.01	0.1	$\mu$ A
$V_h$	$I_h = 10mA$	3.0			V
$V_C^1$	$I_{PP} = 2A, t_p = 8/20\mu s$ (Each Line)			5.5	V
$V_C^1$	$I_{PP} = 10A, t_p = 8/20\mu s$ (Each Line)			10.0	V
$V_C^1$	$I_{PP} = 50A, t_p = 8/20\mu s$ (Each Line)			18.0	V
$C_{ESD}^1$	$V_R = 3.0V, f = 1MHz$ (Each Line)		1.2	2.0	pF

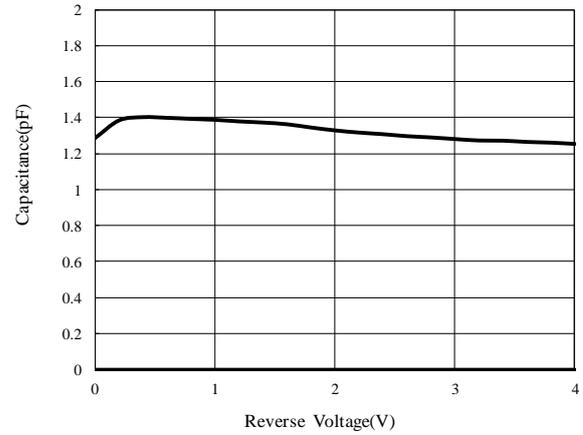
**NOTES**

<sup>1</sup>Guaranteed by design and not subject to production test.

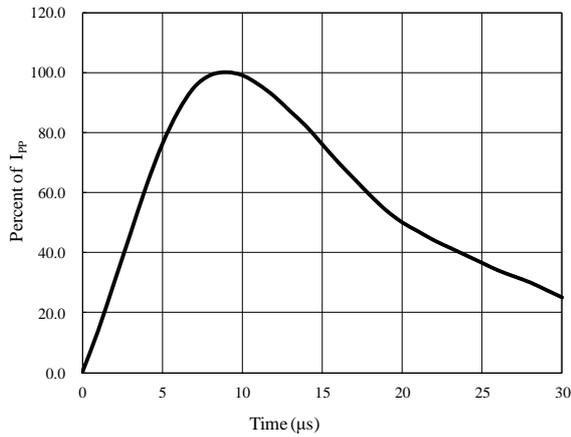
### TLP Testing of Pin1, 8 to 2, 7 & Pin3, 6 to Pin4, 5



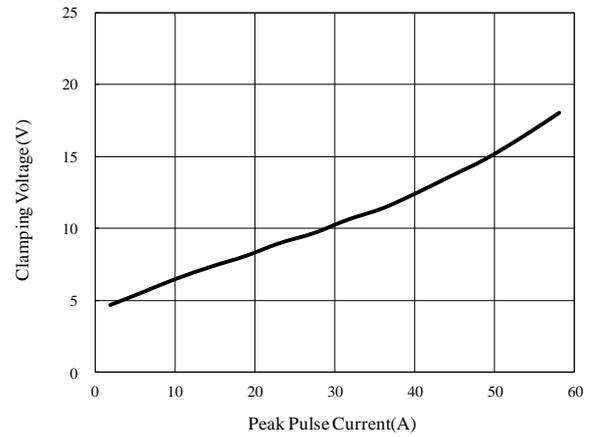
### Capacitance vs. Reverse Voltage Pin1, 8 to 2, 7 & Pin3, 6 to Pin4, 5



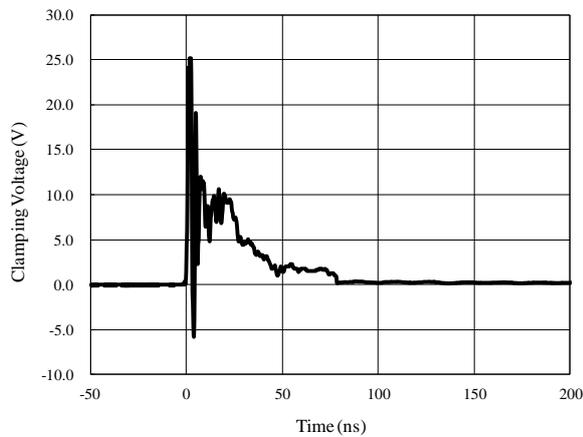
### 8/20µs Pulse Waveform



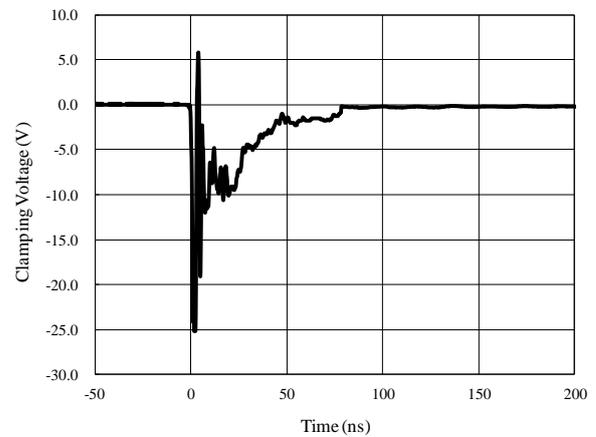
### Clamping Voltage vs. Peak Pulse Current



### ESD Clamping of Pin1, 8 to 2, 7 & Pin3, 6 to Pin4, 5 (+8kV Contact per IEC 61000-4-2)



### ESD Clamping of Pin1, 8 to 2, 7 & Pin3, 6 to Pin4, 5 (-8kV Contact per IEC 61000-4-2)



## Application Information

Electronic equipment is susceptible to damage caused by a variety of sources, including Electrostatic Discharge (ESD), Electrical Fast Transients (EFT) and Lightning strikes. The SYS42L02FAC was designed to protect the sensitive equipment from damage which may be induced by such transient events. This product can be configured in different connections to meet the requirement of common-mode and differential-mode as follows:

### Two Lines Bidirectional Protection

The SYS42L02FAC can provide bidirectional protection for two high speed data lines as depicted in figure 2: Pin 1 & 4 is connected to Line 1  
 Pin 5 & 8 is connected to Line 2  
 Pin 2, 3, 6 and 7 are connected to ground

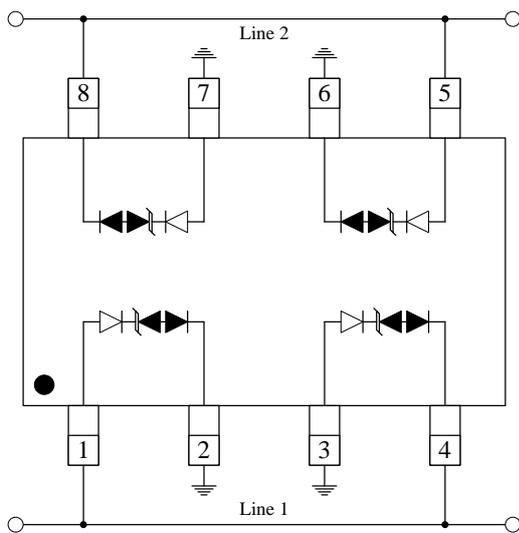


Figure 2 Two lines bidirectional protection

### Two Line Pairs Differential Protection

The SYS42L02FAC can provide differential protection for two high speed data line pairs as depicted in figure 3:

Pin 1, 2, 7 and 8 are connected to Line Pair 1  
 Pin 3, 4, 5 and 6 are connected to Line Pair 2

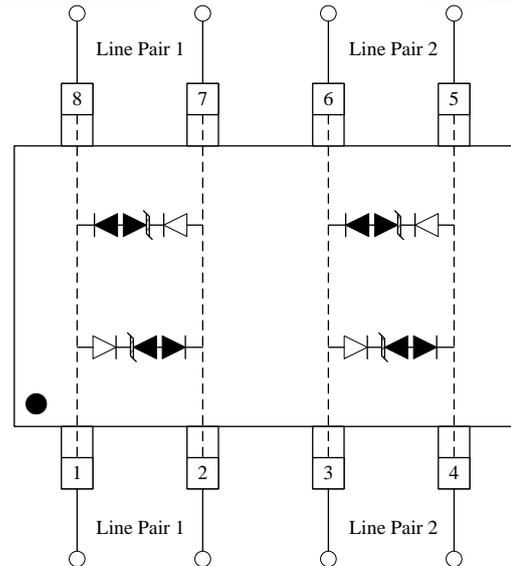
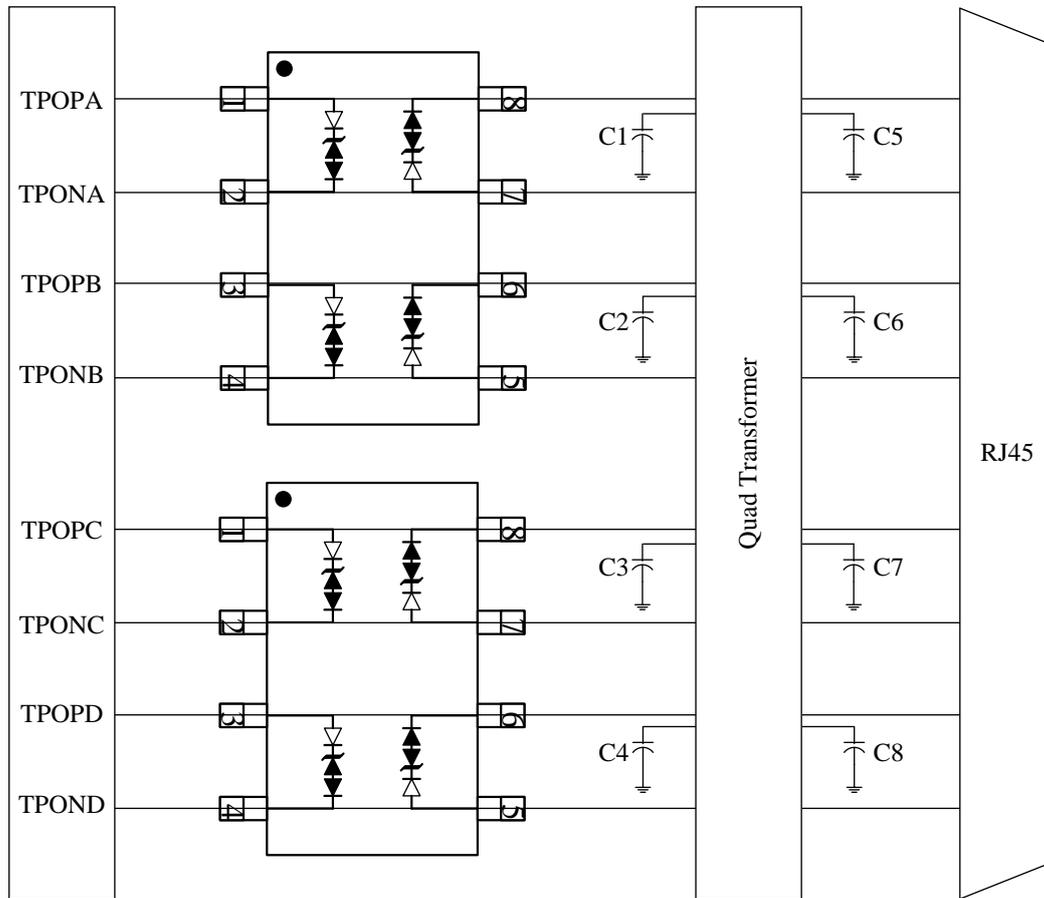


Figure 3 Two line pairs differential protection

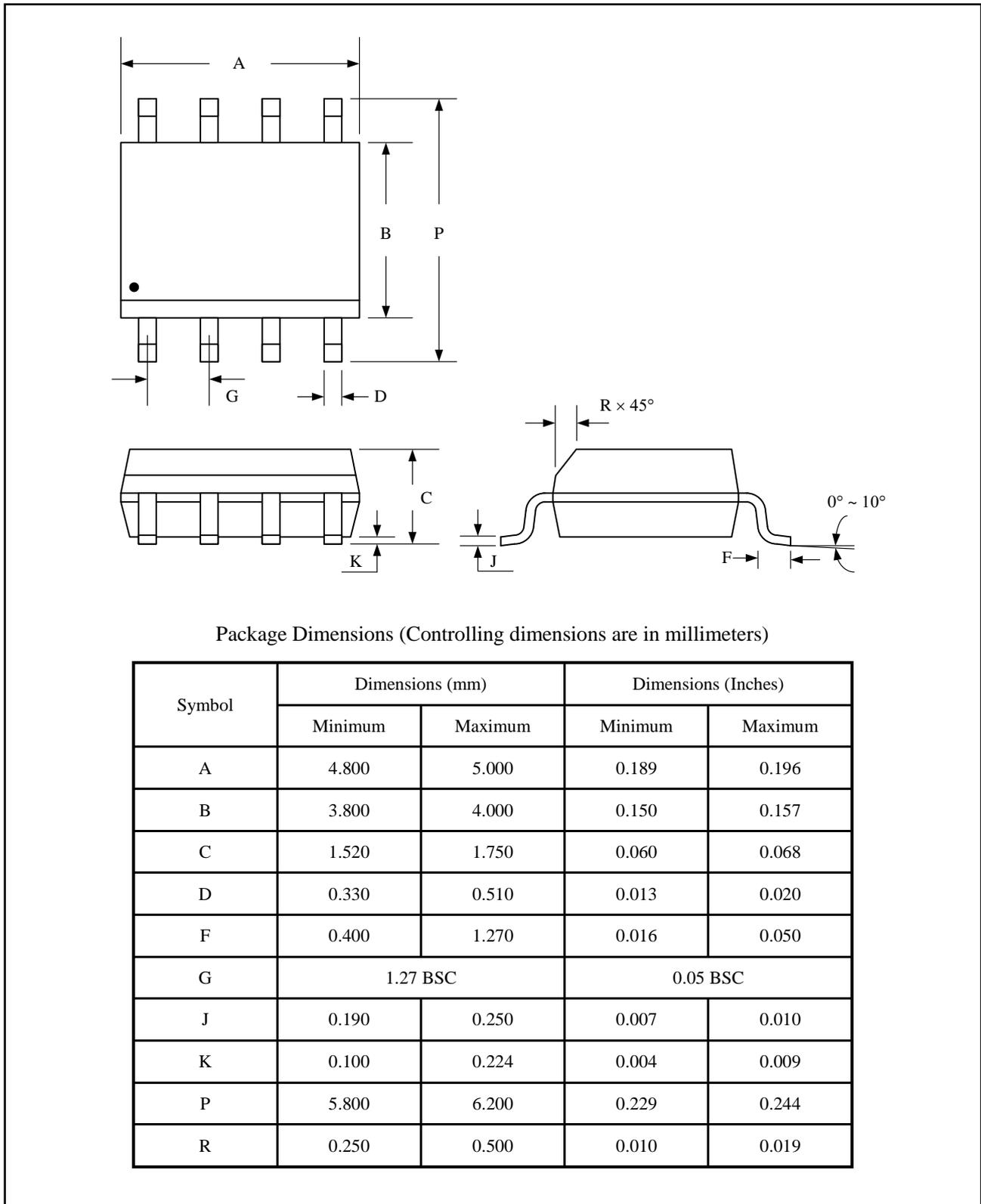
## Application Information



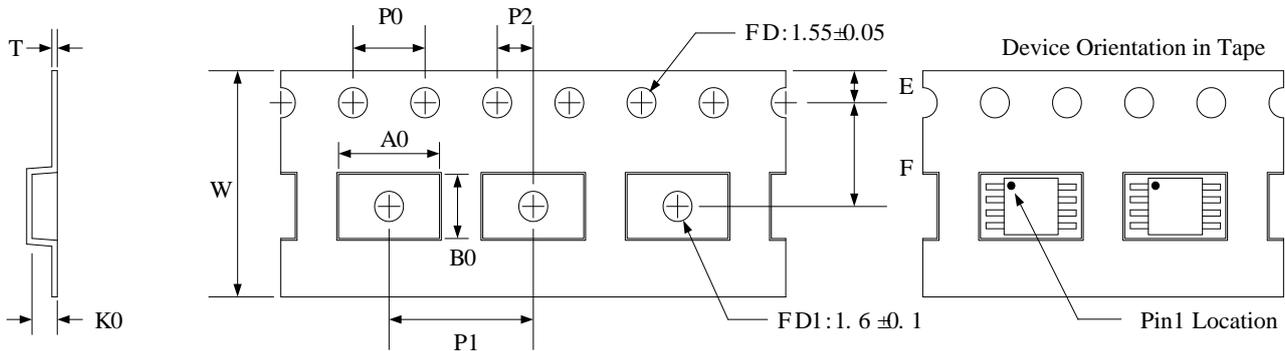
Schematic Diagram for Gigabit Ethernet ESD/ Surge Protection

**Package Outline**

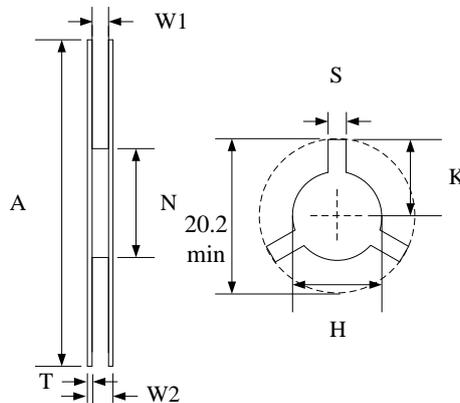
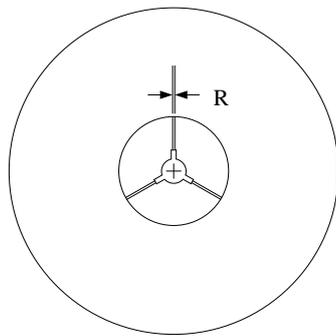
- SOP-8 package



## Tape and Reel Specification



Symbol	W	A0	B0	K0	E	F	P1	P0	P2	T
Dimensions (mm)	12.00±0.3	6.40±0.1	5.2±0.1	2.10±0.1	1.75±0.1	5.50±0.1	8.00±0.1	4.0±0.1	2.0±0.1	0.3±0.05



Symbol	Reel Size	A	N	W2	W1	H	T	S	K	R
Dimensions (mm)	Φ330	330.0±2.0	100.0±2.0	18.4 max	12.4+2.0 -0.0	13.0+0.5 -0.2	2.0±0.2	1.5 min	10.1 min	2.5 min

## Marking Codes



### Note:

- (1) "DBK" is the device code, fixed.
- (2) "YWA" is date code.

## Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
SYS42L02FAC	2.8V	2,500	13 Inch



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