# SY6982E1

## High Efficiency, 2A, Two-Cell Boost Li-Ion Battery Charger

## General Description

SY6982E1 is a 3.6-5.5$V_{IN}$, 2A two-cell synchronous boost Li-Ion battery charger integrates 1MHz switching frequency and full protection functions. The charge current up to 2A can be programmed by using the external resistor for different portable applications and indicates the charger current information simultaneous. It also has a programmable charge timeout for safety battery charge operation and a programmable input voltage threshold for adaptive input current limit. SY6982E1 can disconnect output when there is output short circuit or shutdown happens. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

SY6982E1 along with small QFN3x3 footprint provides small PCB area application.

## Ordering Information

SY6982 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

| Ordering Number | Package type | Note |
|---|---|---|
| SY6982E1QDC | QFN3x3-16 | |

## Features

- Low Profile QFN3x3 Package
- Integrated Synchronous Boost with 18V Rating Low $R_{DSON}$ FETs for High Charge Efficiency
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Programmable Input Voltage Threshold for Adaptive Current Limit.
- Maximum 2A Constant Charge Current
- Charge Current Information Indication.
- Programmable Charge Timeout
- Programmable Constant Charge Current
- Selectable Constant Voltage
- ±0.5% Battery Voltage Accuracy
- Thermal Regulation Protection
- External Shutdown Function
- Input Voltage UVLO and OVP
- Over Temperature Protection
- Output Short Circuit Protection
- Charge Status Indication
- Normal Synchronous Boost Operation When Battery Removed

## Applications

- Cellular Telephones, PDA, MP3 Players, MP4 Players
- Digital Cameras
- Bluetooth Applications
- PSP Game Players, NDS Game Players
- Notebook

## Typical Applications

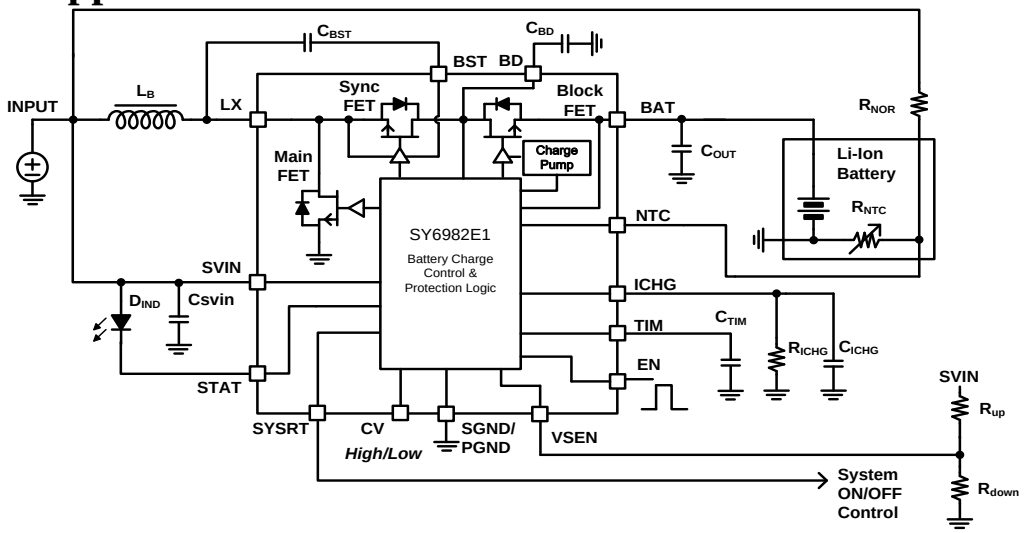
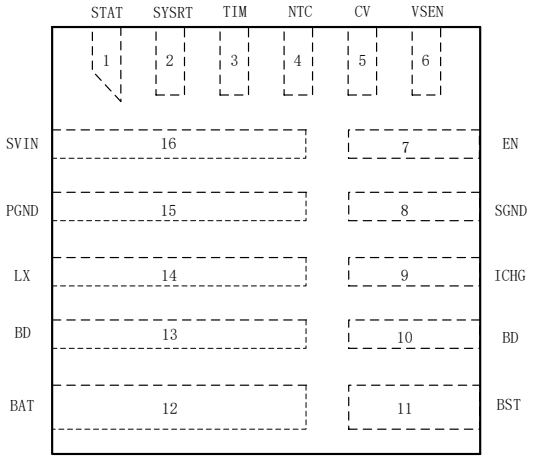



**Figure1. Schematic Diagram**

## Pinout (top view)




(QFN3x3-16)

Top Mark: **BMU*xyz***, (Device code: BMU, ***x=year code, y=week code, z= lot number code***)

| Name | Pin Number | Description |
|---|---|---|
| STAT | 1 | Charge status indication pin. It is open drain output pin and pull high to SVIN thru a LED to indicate the charge in process. When the charge is done, LED is off. |
| SYSRT | 2 | System ON/OFF control pin. When $V_{BAT}$ is lower than 6V, SYSRT pin outputs low logic to turn off the system operation; when $V_{BAT}$ is high than 6V, SYSRT pin outputs high logic to turn on the system operation. |
| TIM | 3 | Charge time limit pin. Connect this pin with a capacitor to ground. Internal current source charge the capacitor for TC mode and CC mode's charge time limit. TC charge time limit is about 1/9 of CC charge time. |
| NTC | 4 | Thermal protection pin. UTP threshold is typical 75%$V_{SVIN}$ and OTP threshold is typical 30%$V_{SVIN}$. Pull up to SVIN can disable charge logic and make the IC operate as normal boost regulator. Pull down to ground can shutdown the IC. |
| CV | 5 | Battery CV voltage selection pin. Program 2 different CV thresholds by setting different voltage on the pin. The detailed information is shown in description section. |
| VSEN | 6 | Voltage sense of SVIN. If the voltage drops to internal 1.195V reference voltage, the SVIN will be clamped to setting value and input current will be limited. |
| EN | 7 | Enable control pin. High logic for enable on, and low logic for enable off. |
| SGND | 8 | Signal ground pin. |
| ICHG | 9 | Charge current program pin, pull down to GND with a Resistor $R_{ICHG.}$ The mirror current about 1/10000 of the blocking FET current will dump into the external RC network thru ICHG pin and compared to the internal reverence 1V. So $I_{CC}$=(1V/ $R_{ICHG}$)x10000, $I_{TC}$=(1V/ $R_{ICHG}$)x1000. |
| BD | 10, 13 | Connect to the Drain of internal Blocking FET. Bypass at least 4.7uF ceramic cap to GND. |
| BST | 11 | Boost-Strap pin. Supply Rectified FET's gate driver. Decouple this pin to LX with 0.1uF ceramic cap. |
| BAT | 12 | Battery positive pin. |
| LX | 14 | Switch node pin. Connect to external inductor. |
| PGND | 15 | Power ground pin. |
| SVIN | 16 | Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area. |

## Absolute Maximum Ratings

STAT, NTC, CV, VSEN, EN, ICHG, BD, BAT, LX, SVIN ---------- 18V
SYSRT, TIM, BST-LX ---------- 4V
LX Pin current continuous ---------- 5A
Power Dissipation, $P_D$ @ $T_A$ = 25℃, QFN3x3 ---------- 2.6W
Package Thermal Resistance
$\theta_{JA}$ ----------38℃/W
$\theta_{JC}$ ----------4℃/W
Junction Temperature Range ---------- -40℃ to +125℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 125℃

## Recommended Operating Conditions

SVIN ---------- 3.6V to 5.5V
STAT, NTC, CV, VSEN, EN, ICHG, BD, BAT, LX ---------- -0.3V to 16V
SYSRT, TIM, BST-LX ---------- -0.3V to 3.3V
LX Pin current continuous ---------- 5A
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

## Electrical Characteristics

$T_A$=25 ℃, $V_{IN}$=5V, GND=0V, $C_{IN}$=4.7uF, L=0.68uH, $R_{ICHG}$=10kΩ, $C_{TIM}$=470nF, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Bias Supply ($V_{SVIN}$)** | | | | | | |
| $V_{SVIN}$ | Supply voltage | | 3.6 | | 16 | V |
| $V_{UVLO}$ | $V_{SVIN}$ under voltage lockout threshold | $V_{SVIN}$ rising and measured from $V_{SVIN}$ to GND | | | 3.6 | V |
| $\Delta V_{UVLO}$ | $V_{SVIN}$ under voltage lockout hysteresis | Measured from $V_{SVIN}$ to GND | | 100 | | mV |
| $V_{OVP}$ | Input overvoltage protection | $V_{SVIN}$ rising and measured from $V_{SVIN}$ to GND | 5.8 | | | V |
| $\Delta V_{OVP}$ | Input overvoltage protection hysteresis | Measured from $V_{SVIN}$ to GND | | 0.5 | | V |
| **Quiescent Current** | | | | | | |
| $I_{BAT}$ | Battery discharge current | Shutdown IC, EN=NTC=0 | | | 10 | uA |
| $I_{IN}$ | Input quiescent current | Disable Charge, EN=1,NTC=0 | | | 1.5 | mA |
| **Oscillator and PWM** | | | | | | |
| $f_{SW}$ | Switching frequency | | | 1000 | | kHz |
| $T_{MINOFF}$ | Main N-FET minimum off time | With 18V rating | | 100 | | ns |
| $T_{MAXOFF}$ | Main N-FET maximum off time | With 18V rating | | 30 | | us |
| $T_{MINON}$ | Main N-FET minimum on time | With 18V rating | | 100 | | ns |
| **Power MOSFET** | | | | | | |
| $R_{NFET\_M}$ | $R_{DS(ON)}$ of Main N-FET | | | 80 | | mΩ |
| $R_{NFET\_R}$ | $R_{DS(ON)}$ of Rectified N-FET | | | 40 | | mΩ |
| $R_{NFET\_B}$ | $R_{DS(ON)}$ of Blocking N-FET | | | 40 | | mΩ |
| **Voltage Regulation** | | | | | | |
| $V_{CV}$ | 2-Cell CV charge mode voltage | $V_{CV}$<1V | 8.457 | 8.5 | 8.542 | V |
| | | $V_{CV}$>2V | 8.756 | 8.8 | 8.844 | |
| $V_{CVH}$ | High level logic for CV | | 2 | | | V |
| $V_{CVL}$ | Low level logic for CV | | | | 1 | V |
| $\Delta V_{RCH}$ | 2-Cell Recharge Voltage | | 100 | 200 | 300 | mV |
| $V_{TRK}$ | 2-cell TC charge mode battery voltage threshold | Rising edge threshold | 5.4 | 5.6 | 5.8 | V |
| **Battery Connect Detection** | | | | | | |
| $V_{DET}$ | NTC voltage threshold for Battery detect | NTC Falling Edge | 85% | | 95% | $V_{SVIN}$ |
| $t_{DET}$ | Detect delay time | | | 30 | | ms |
| **Charge Current** | | | | | | |
| | Internal charge current accuracy for Constant Current Mode | $I_{CC}$=1000mA | -10% | | 10% | |
| | Internal charge current accuracy for Trickle Current Mode | $I_{TC}$=100mA | -50% | | 50% | |
| $I_{TERM}$ | Termination current | $I_{CC}$=1000mA | 50 | 100 | 150 | mA |
| **Output Voltage OVP** | | | | | | |
| $V_{OVP}$ | Output voltage OVP threshold | | 105% | 110% | 115% | $V_{CV}$ |
| **Input Voltage Threshold for Adaptive Current Limit** | | | | | | |
| $V_{Threshold}$ | Voltage reference of VSEN | | 1.176 | 1.2 | 1.224 | V |
| **Timer** | | | | | | |

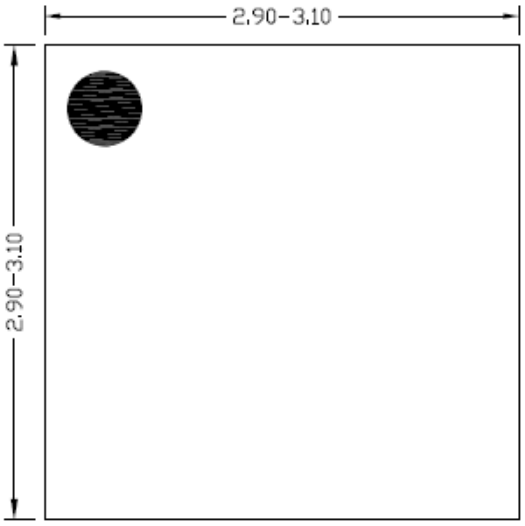
| | | | | | | |
|---|---|---|---|---|---|---|
| $T_{TC}$ | Trickle current charge timeout | $C_{TIM}$=330nF | 0.23 | 0.5 | 0.67 | hour |
| $T_{CC}$ | Constant current charge timeout | | 3.0 | 4.5 | 6 | hour |
| $T_{MC}$ | Charge mode change delay time | | | 30 | | ms |
| $T_{TERM}$ | Termination delay time | | | 30 | | ms |
| $T_{RCHG}$ | Recharge time delay | | | 30 | | ms |
| **Short Circuit Protection** | | | | | | |
| $V_{SHORT}$ | Output short protection threshold | | 1.70 | 2.00 | 2.30 | V |
| **System ON/OFF Control** | | | | | | |
| $V_{HSYSRT}$ | High logic of system ON/OFF control | | 2.1 | | | V |
| $V_{LSYSRT}$ | Low logic of system ON/OFF control | | | | 0.6 | V |
| **Linear charger Mode** | | | | | | |
| $I_{LCHG}$ | Battery Charger current when the blocking FET is in linear mode | $V_{BAT}$<$V_{SHORT}$ | | 5% | | $I_{CC}$ |
| $V_{BD}$ | Bus voltage regulation | | 5.8 | 6 | 6.2 | V |
| $V_{TRON}$ | Blocking FET fully turn on threshold $V_{TRON}$=$V_{BAT}$-$V_{IN}$ | $V_{BAT}$ > $V_{TRK}$ | | 100 | | mV |
| **Enable ON/OFF Control** | | | | | | |
| $V_{ENH}$ | High level logic for enable control | | 1.5 | | | V |
| $V_{ENL}$ | Low level logic for enable control | | | | 0.4 | V |
| **Battery Thermal Protection NTC** | | | | | | |
| UTP | Under temperature protection | | 70% | 75% | 80% | $V_{SVIN}$ |
| | Under temperature protection hysteresis | Falling edge | | 5% | | |
| OTP | Over temperature protection | | 28% | 30% | 32% | |
| | Over temperature protection hysteresis | Rising edge | | 2% | | |
| **Thermal Regulation And Thermal shutdown** | | | | | | |
| $T_{REG}$ | Thermal regulation threshold | Rising Threshold | | 120 | | ℃ |
| $T_{REGHYS}$ | Thermal regulation hysteresis falling edge | | | 20 | | ℃ |
| | Thermal regulation fold back ratio | | | 0.25 | | $I_{CC}$ |
| $T_{SD}$ | Thermal shutdown temperature | Rising Threshold | | 160 | | ℃ |
| $T_{SDHYS}$ | Thermal shutdown temperature hysteresis | | | 30 | | ℃ |

**Note 1**: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

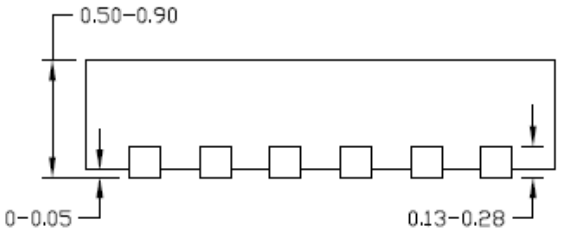
**Note 2**: $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25℃ on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 3**: The device is not guaranteed to function outside its operating conditions

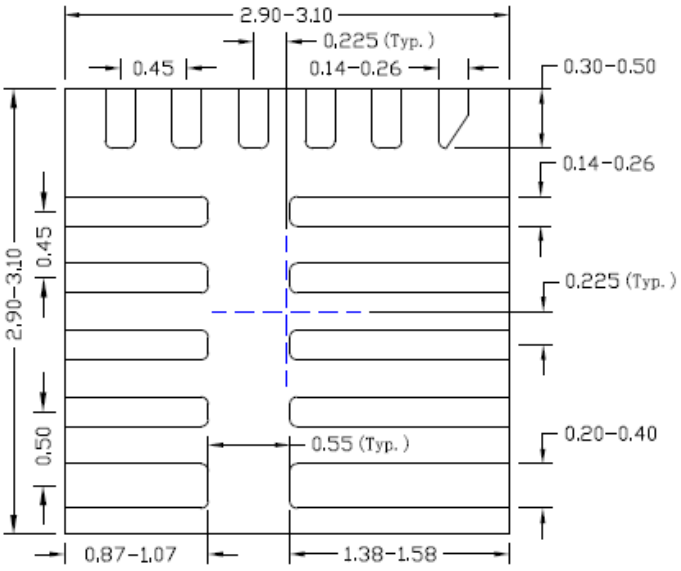
# QFN3x3-16 Package Outline Drawing



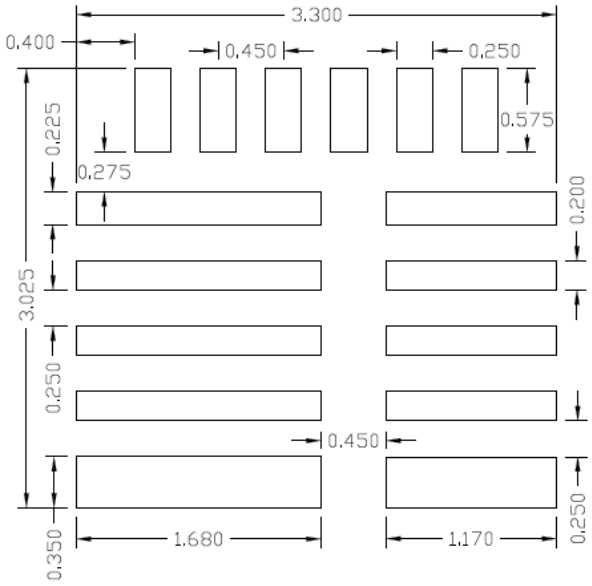

Top View




Side View




Bottom View



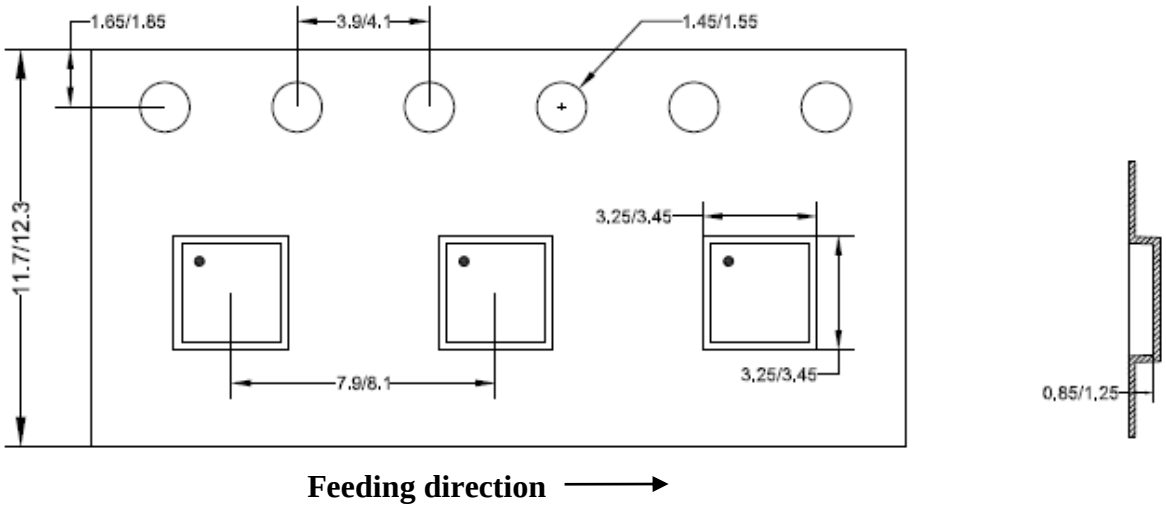

Recommended PCB layout
(Reference only)

**Notes:** **All dimension in millimeter and exclude mold flash & metal burr**

# Taping & Reel Specification

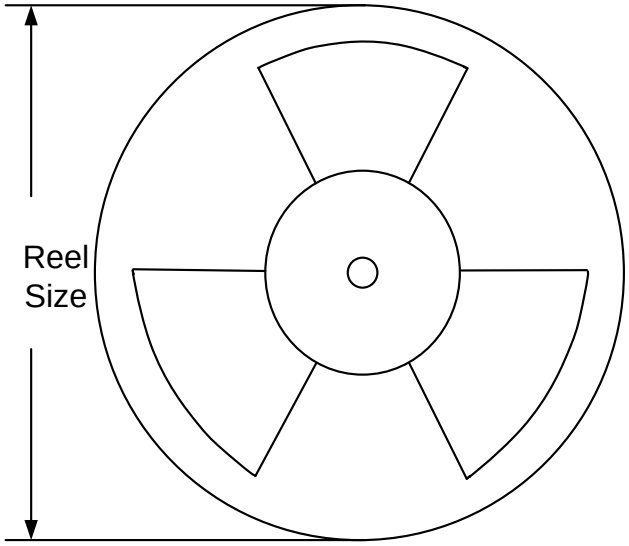
## 1. Taping orientation

**QFN3x3**




**Feeding direction** ⟶

## 2. Carrier Tape & Reel specification for packages




| Package type | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|
| QFN3x3 | 12 | 8 | 13" | 400 | 400 | 5000 |

## 3. Others: NA