SY20213B

High Efficiency3.0MHz, 0.6A Synchronous Step Down Regulator

General Description

The SY20213B is a high efficiency 3MHz synchronous step down DC/DC regulator IC capable of delivering up to 0.6A output current. It can operate in PFM or CCM mode during light load programed by MODE pin. It can operate over a wide input voltage range from 1.85V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Ordering Information

SY20213□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY20213BDTC	DFN1.45x1-6	--

Features

- 1.85~5.5V input voltage range
- 3MHz switching frequency
- 40uA low quiescent current
- Low $R_{DS(ON)}$ for internal switches (PFET/NFET): 350mΩ/250mΩ
- Fixed 100us soft-start time
- PFM/CCM operation mode during light load programed by MODE pin
- Hic-cup mode protection for hard short condition
- RoHS Compliant and Halogen Free
- Compact package: DFN1.45x1-6

Applications

- Portable Audio, Portable Media
- Cell phones
- Digital Cameras

Typical Applications

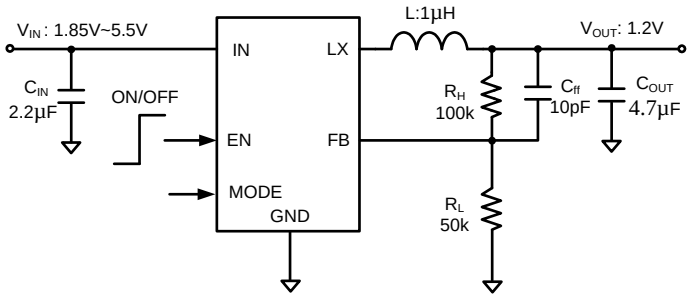


Figure 1.Schematic diagram

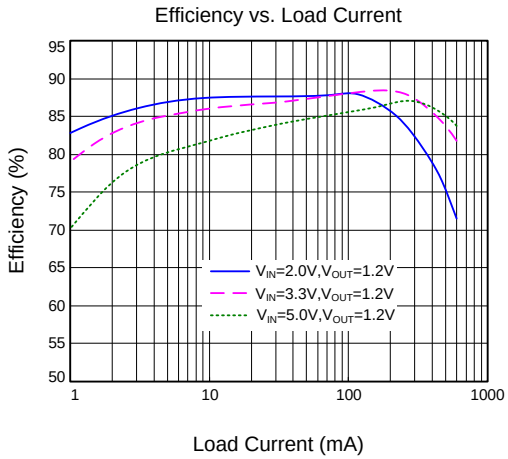
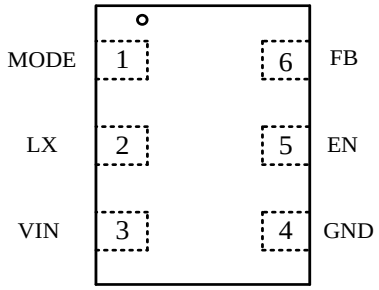


Figure 2. Efficiency vs. Load Current

Pinout (Top View)



(DFN1.45x1-6)

Top Mark: C*xyz* *for SY20213B* (device code: C, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
1	MODE	Mode control pin. MODE=high, selected Force CCM mode operation during light load. MODE=low, selected PFM mode operation during light load.
2	LX	Inductor pin. Connect this pin to the switching node of inductor.
3	VIN	Input pin. Decouple this pin to GND pin with at least 2.2uF ceramic cap.
4	GND	Ground pin.
5	EN	Enable control. Pull high to turn on. Do not leave it float.
6	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.4V*(1+R_H/R_L)$.

Absolute Maximum Ratings (Note 1)

VIN, LX---------- 6.0V
Enable, MODE, FB Voltage---------- V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25°C,
DFN1.45x1-6 ---------- 450mW
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 200°C/W
θ_{JC} ---------- 130°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 1.85V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.2V, L = 1uH, C_{OUT} = 4.7uF, T_A = 25°C, unless otherwise specified)

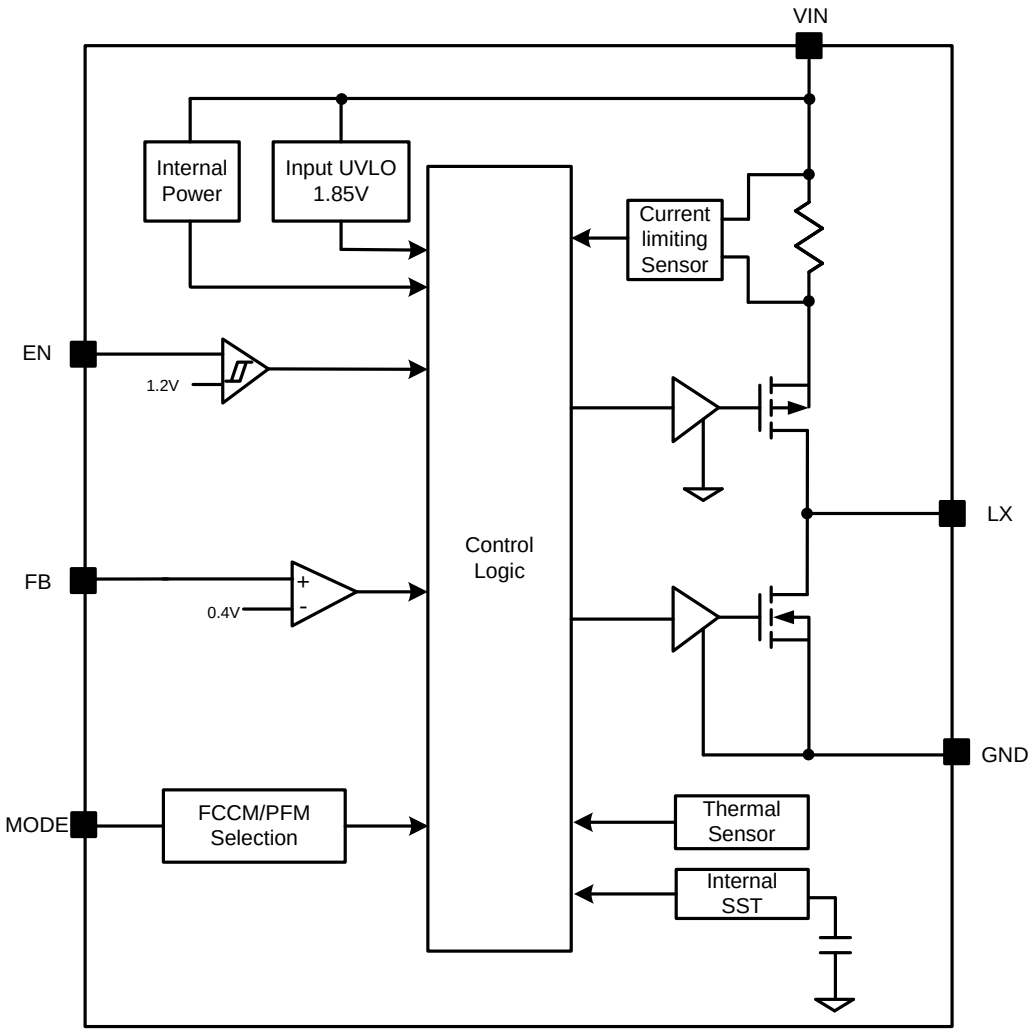
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		1.85		5.5	V
Quiescent Current	I_Q	I_{OUT}=0,V_{FB}=V_{REF} × 105%		40		μA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.392	0.4	0.408	V
Input UVLO threshold	V_{UVLO}				1.85	V
UVLO hysteresis	V_{HYS}			0.1		V
PFET RON	$R_{DS(ON),P}$			350		mΩ
NFET RON	$R_{DS(ON),N}$			250		mΩ
PFET Current Limit	I_{LIM}		1			A
EN rising threshold	V_{ENH}		1.2			V
EN falling threshold	V_{ENL}				0.4	V
Oscillator Frequency	F_{OSC}			3		MHz
Min ON Time				50		ns
Soft Start Time	T_{SS}			100		us
Short Circuit Protection Threshold	V_{SCP}			0.17		V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

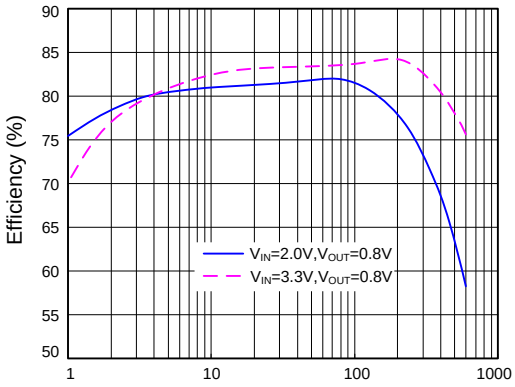
Note 3: The device is not guaranteed to function outside its operating conditions.

Block Diagram



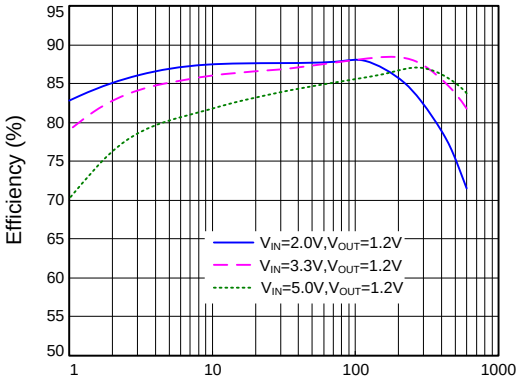
Typical Performance Characteristics

Efficiency vs. Load Current



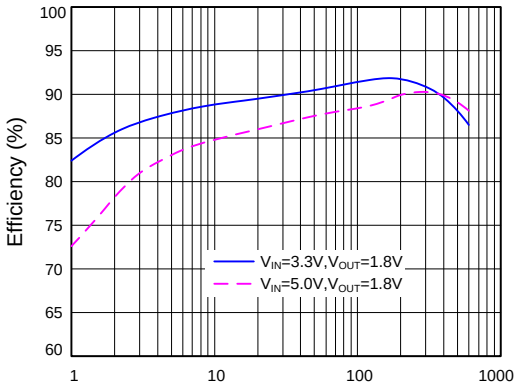
Load Current (mA)

Efficiency vs. Load Current



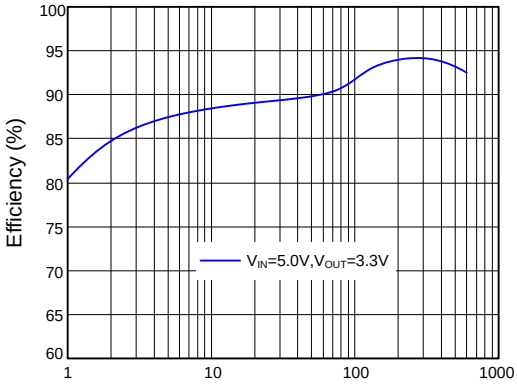
Load Current (mA)

Efficiency vs. Load Current



Load Current (mA)

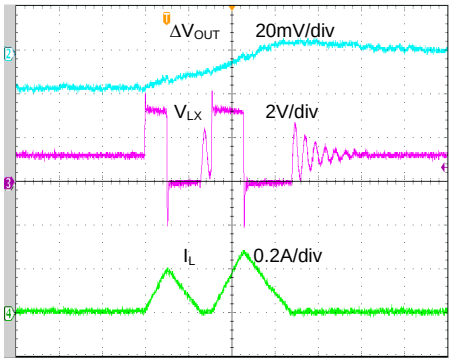
Efficiency vs. Load Current



Load Current (mA)

Output Ripple

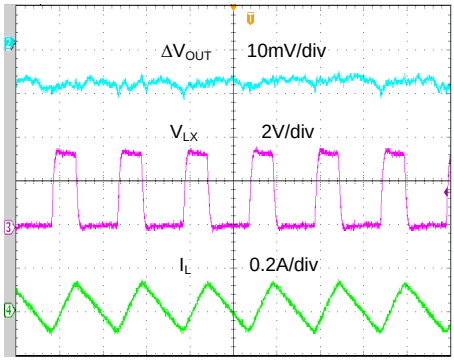
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A, PFM)



Time (200ns/div)

Output Ripple

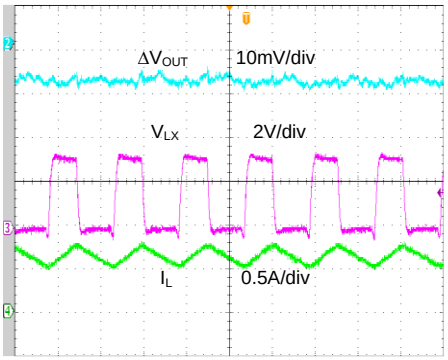
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A, FCCM)



Time (200ns/div)

Output Ripple

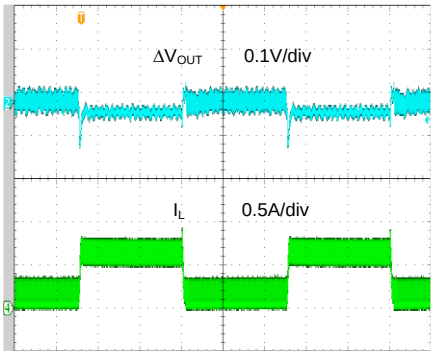
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=0.6A)



Time (200ns/div)

Load Transient

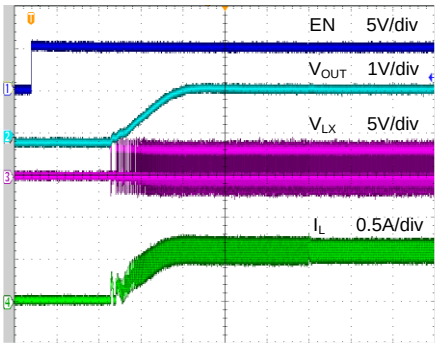
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=0.06~0.6A)



Time (200μs/div)

Startup from Enable

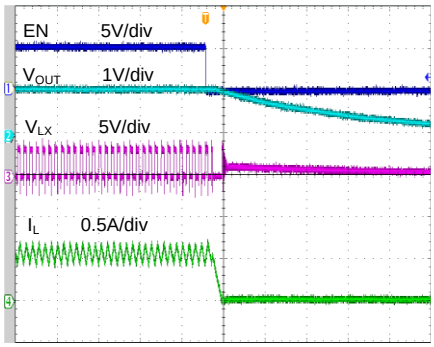
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=0.6A)



Time (40μs/div)

Shutdown from Enable

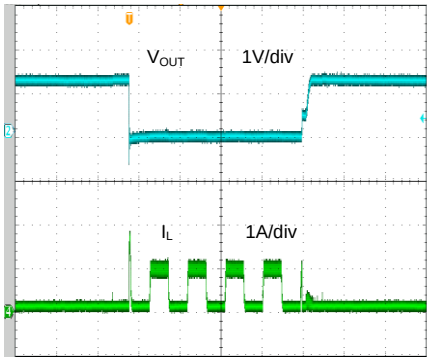
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=0.6A)



Time (2μs/div)

Short Circuit Protection

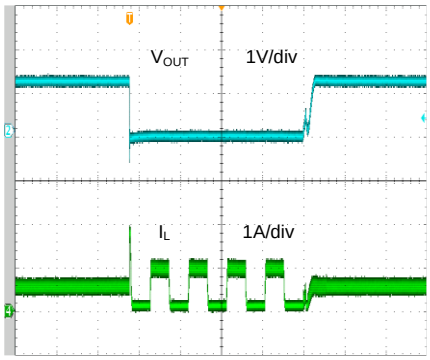
(V_{IN}=3.3V,V_{OUT}=1.2V,0A To Short)



Time (400μs/div)

Short Circuit Protection

(V_{IN}=3.3V,V_{OUT}=1.2V,0.6A To Short)



Time (400μs/div)

Operation

SY20213B is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

Applications Information

Because of the high integration in the SY20213B IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT} and output inductor L need to be selected for the targeted applications specifications.

Feedback resistor dividers R_H and R_L:

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If R_L=120kΩ is chosen, then RH can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.4V) \cdot R_L}{0.4V}$$

Input capacitor C_{IN}:

With the maximum load current at 0.6A, the maximum ripple current through input capacitor is about 0.6Arms. A typical X5R or better grade ceramic capacitor with 6V rating and greater than 2.2uF capacitance can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6V rating and greater than 4.7uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20213B regulator ICs are quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<150mΩ to achieve a good overall efficiency.

Layout Design:

The layout design of SY20213B regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN} and L.

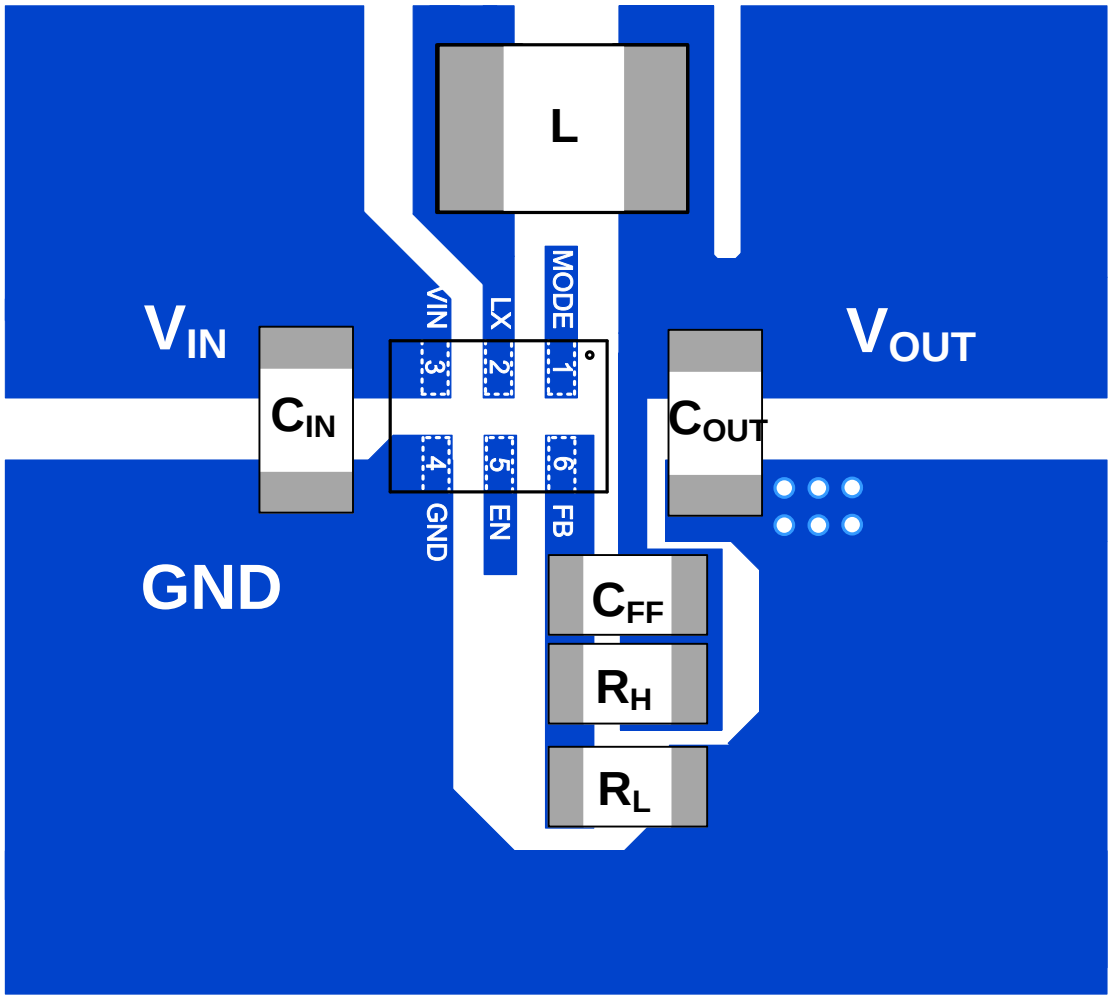
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

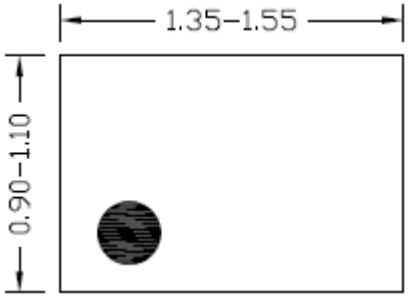
3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The trace connecting to the OUT pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

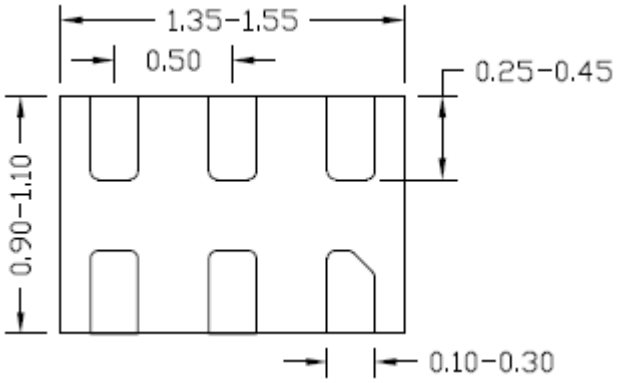
PCB Layout Suggestion



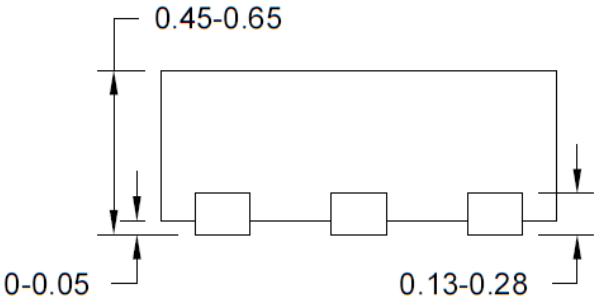
DFN1.45×1-6 Package Outline Drawing



Top View



Bottom View

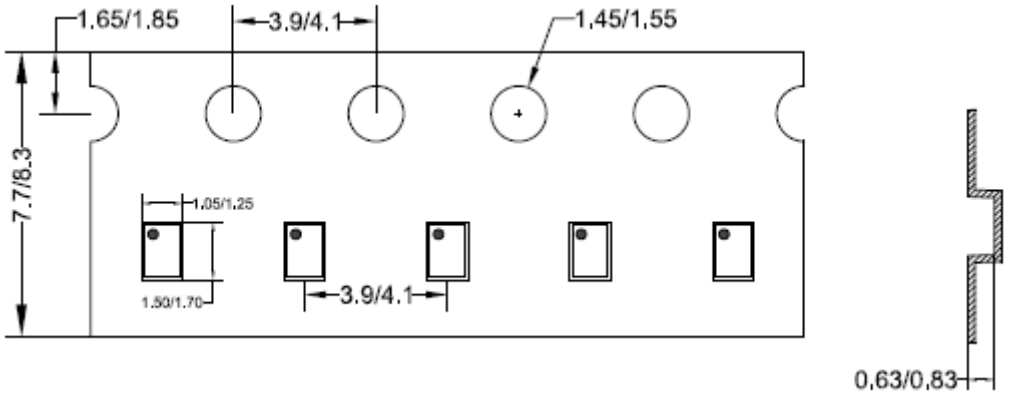


Side View

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

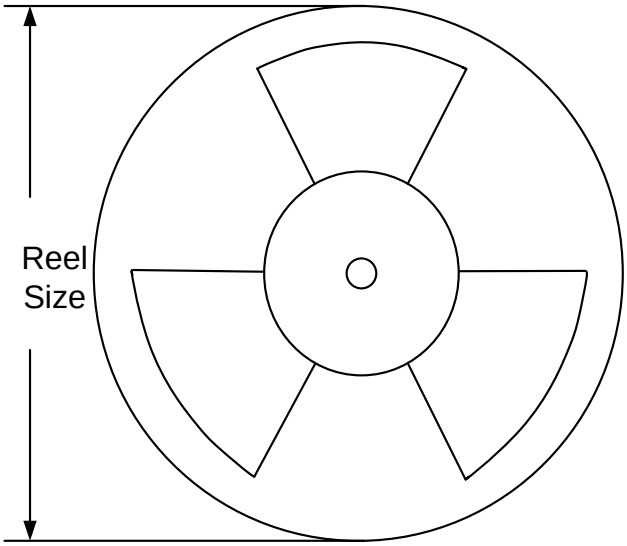
Taping & Reel Specification

1. Taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.45x1	8	4	7"	400	160	3000

3. Others: NA

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