SY21087

High Efficiency Fast Response, 2A, 23V Input Synchronous Step Down Regulator

General Description

SY21087 develops a high efficiency synchronous step-down DC/DC converter capable of delivering 2A output current. SY21087 operates over a wide input voltage range from 4.5V to 23V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

SY21087 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500kHz under continuous conduction mode to minimize the size of inductor and capacitor.

Ordering Information

SY21087 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21087FAC	SO8	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 150/110 mΩ
- 4.5-23V Input Voltage Range
- Instant PWM Architecture to Achieve Fast Transient Responses
- Programmable Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 500kHz
- 2A Output Current Capability
- 1.5% 0.6V Reference
- RoHS Compliant and Halogen Free
- Compact Package: SO8

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Applications

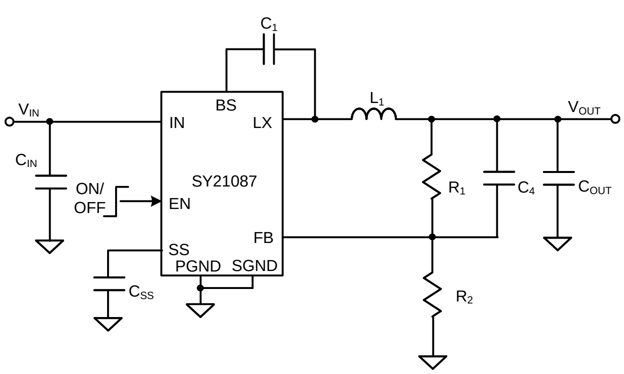


Figure 1. Schematic Diagram

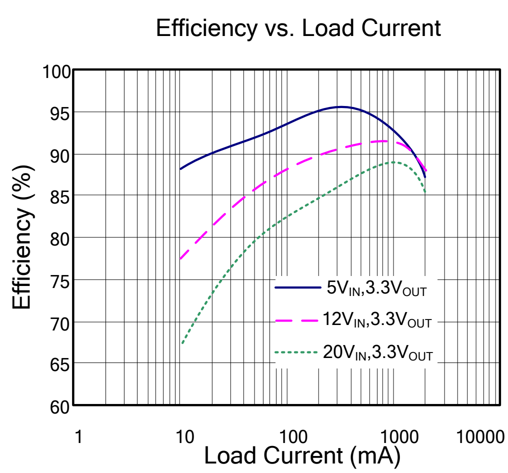
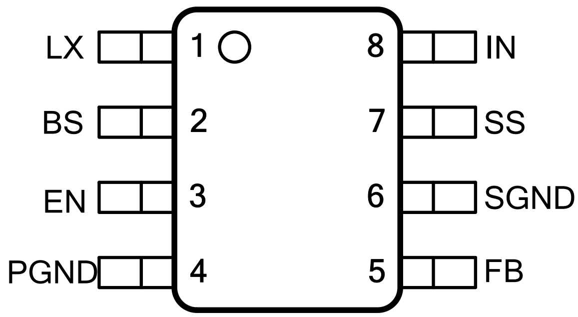


Figure 2. Efficiency Figure

Pinout (top view)



(SO8)

Top Mark: **AIU*xyz***, **(**Device code:AIU, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
BS	2	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with a 0.1uF ceramic capacitor.
IN	8	Input pin. Decouple this pin to PGND pin with at least a 1uF ceramic capacitor.
LX	1	Inductor pin. Connect this pin to the switching node of the inductor.
PGND	4	Power Ground pin.
FB	5	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.6*(1+R1/R2)
SGND	6	Signal Ground pin, should be connected to clean ground plane.
EN	3	Enable control. Pull high to turn on. Do not leave it floating.
SS	7	Soft-start programming pin. The default soft-start time is 800us when this pin is floated. For longer soft-start time, connect a capacitor from this pin to SGND to program the soft-start time. $t_{SS}(ms)=C_{SS}(nF)\times\frac{0.6V}{5uA}$

Block Diagram

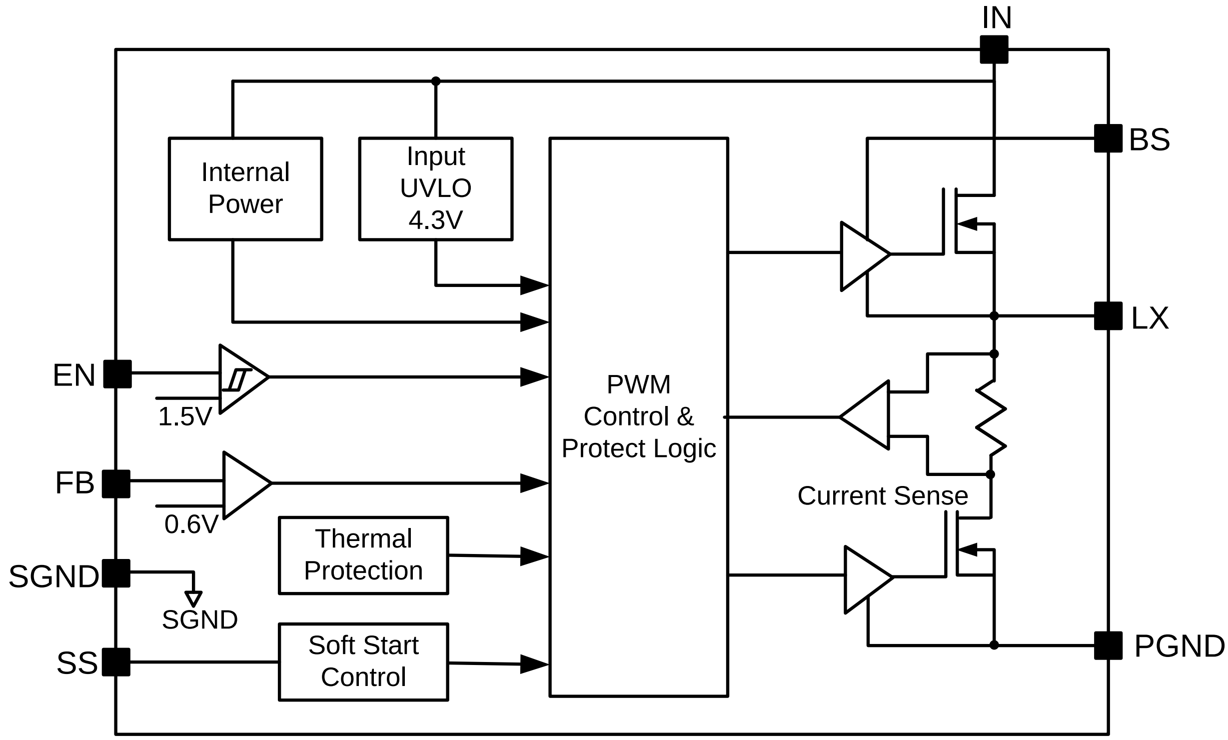


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage -- 25V
EN, LX-- VIN + 0.3V
FB, BS-LX -- 4V
Power Dissipation, P_D @ T_A = 25°C SO8 -- 1.1W
Package Thermal Resistance (Note 2)
θ_{JA} -- 88°C/W
θ_{JC} -- 45°C/W
Junction Temperature Range -- 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage -- 4.5V to 23V
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range -- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 5V, C_{OUT} = 10uF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		23	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		400		μA
Shutdown Current	I_{SHDN}	EN=0		10		μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
FB Input Current	I_{FB}	V_{FB}=4V	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			150		mΩ
Bottom FET RON	$R_{DS(ON)2}$			110		mΩ
Bottom FET Valley Current Limit	I_{LIM}		2			A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				4.5	V
UVLO Hysteresis	V_{HYS}			0.4		V
Oscillator Frequency	F_{SW}	V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=1A		0.5		MHz
Soft-start Time	t_{SS}	SS pin is floated		0.8		ms
		Connect C_{SS} between SS pin and SGND		$C_{SS}(nF)\times\frac{0.6V}{5uA}$		ms
Min ON Time				50		ns
Min OFF Time				160		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	$T_{SD,HYS}$			15		°C

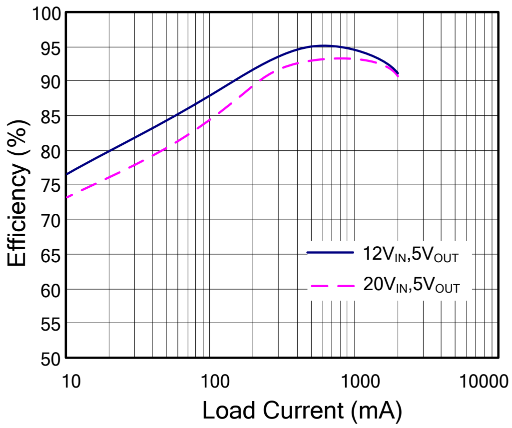
Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of SO8 package is the case position for θ_{JC} measurement.

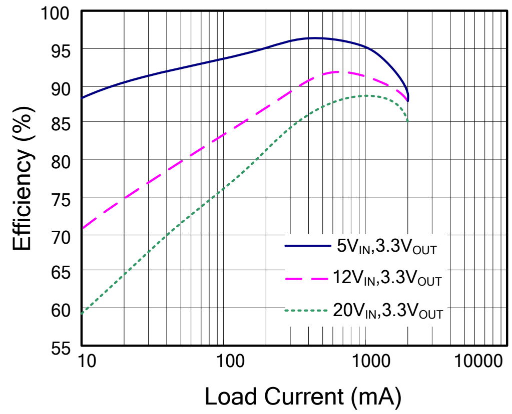
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

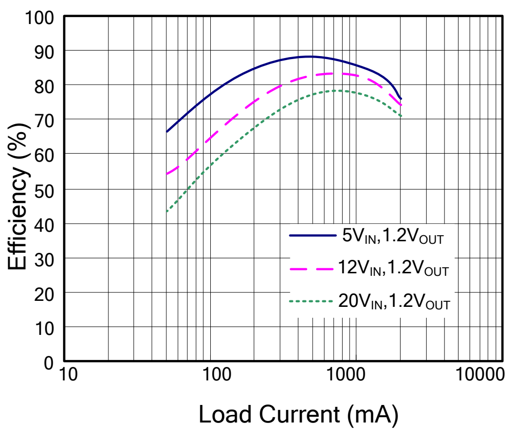
Efficiency vs. Load Current



Efficiency vs. Load Current

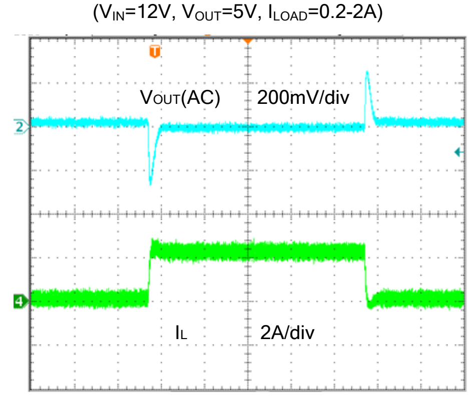


Efficiency vs. Load Current



Load Transient

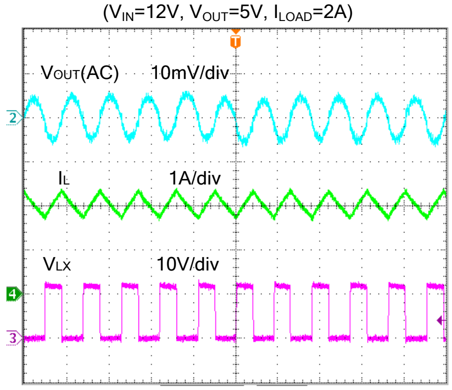
(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=0.2-2A)



Time (100us/div)

Output Ripple

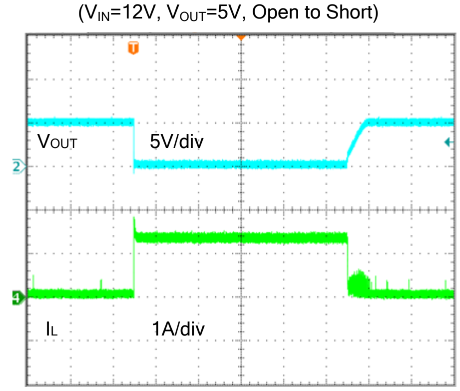
(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=2A)



Time (2us/div)

Short Circuit Protection

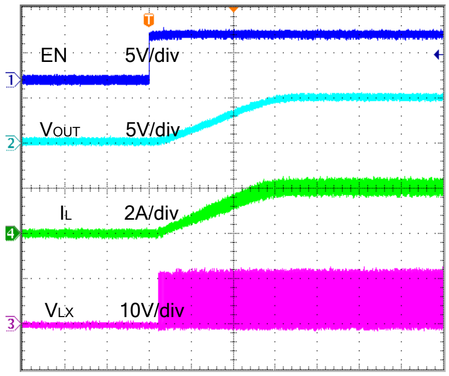
(V_{IN}=12V, V_{OUT}=5V, Open to Short)



Time (1ms/div)

Startup

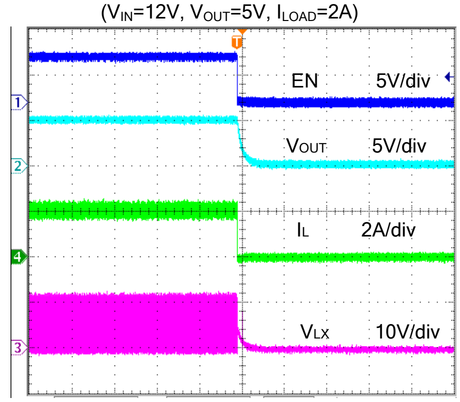
(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=2A)



Time (400us/div)

Shutdown

(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=2A)



Time (400us/div)

Operation

SY21087 is a synchronous buck regulator that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator IC can achieve high efficiency and high switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

SY21087 provides protection functions such as cycle by cycle current limiting, output short circuit protection and thermal shutdown protection.

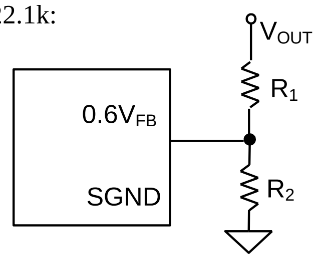
Applications Information

Because of the high integration in the SY21087 IC, the application circuit based on this regulator is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If Vout is 3.3V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input Capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} \cdot$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and PGND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/PGND pins. In this case, a 10uF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21087 regulator is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

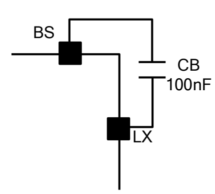
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

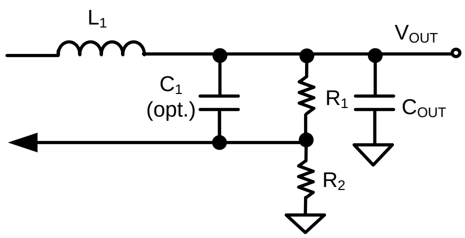
External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



Load Transient Considerations:

The SY21087 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic cap in parallel with R1 may further speed up the load transient responses. It is recommended for applications with large load transient step requirements.



Soft-start:

The default soft-start time is 800us when SS pin is floated. For longer soft-start time, connect a capacitor from this pin to SGND to program the soft-start time.

$$t_{SS}(ms)=C_{SS}(nF)\times\frac{0.6V}{5uA}$$

Layout Design:

The layout design of SY21087 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to PGND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and PGND. The loop area formed by C_{IN} and PGND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and PGND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

6) Put the node of R2, C_{SS} to SGND pin, ensure that the SGND pin is connected to clean ground plane.

PCB Layout Suggestion

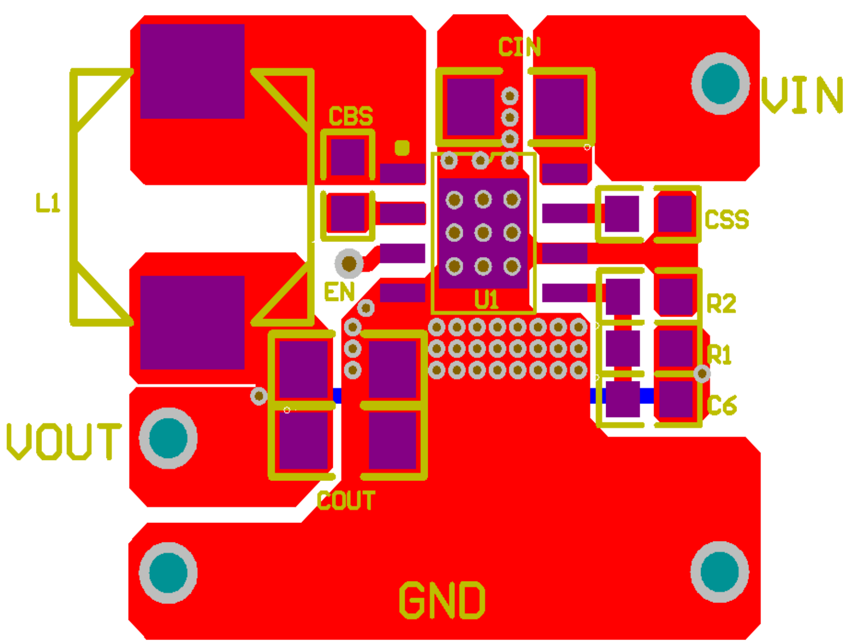
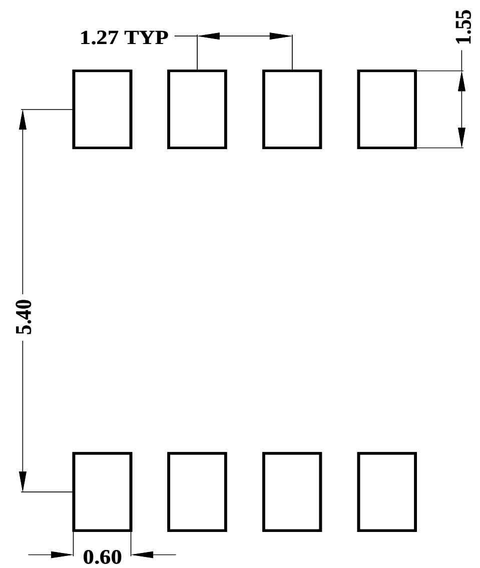
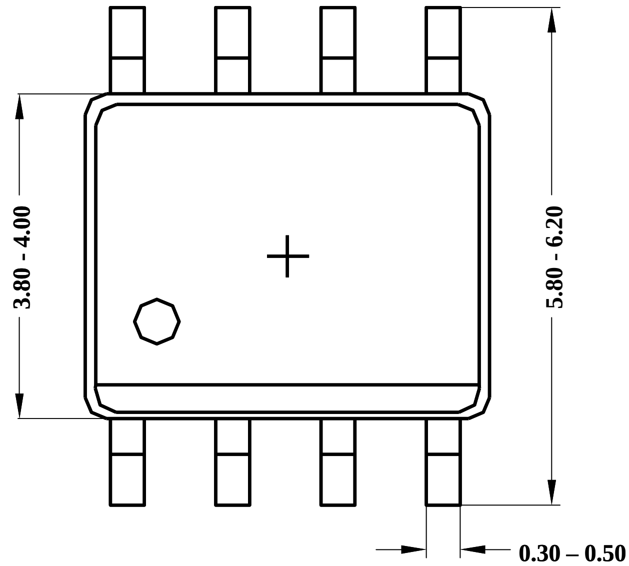


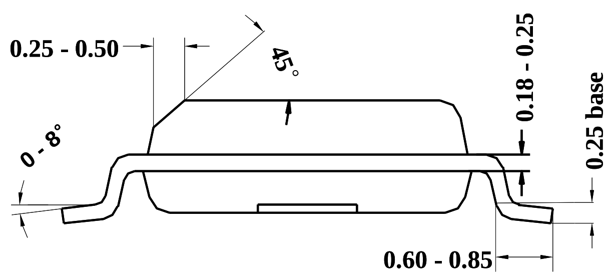
Figure4. PCB Layout Suggestion

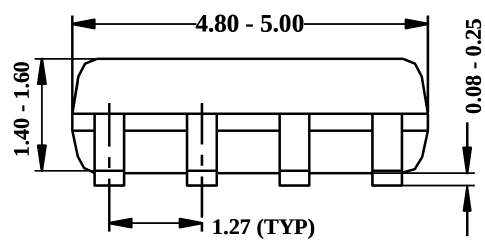
SO8 Package outline & PCB layout design



Recommended Pad Layout







Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

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