SY20466B

1.8V Minimum Input and 5. 5V Maximum Output 6A Peak Current Synchronous Boost with Output Disconnect

General Description

The SY20466B is a high efficiency synchronous Boost regulator that converts down to 1.8V input and up to 5.5V output voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch. It can disconnect the output from input during the shutdown mode.

Ordering Information

SY20466□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20466BQMC	QFN2×2-10	----

Features

- 1.8V Minimum Input Voltage
- Adjustable Output Voltage from 2.5V to 5. 5V
- 6A Peak Current Limit
- Input Under Voltage Lockout
- Load Disconnect During Shutdown
- Selectable Forced PWM Mode Operation
- Output Over Voltage Protection
- Low $R_{DS(ON)}$ (Main Switch/Synchronous Switch) at 5.0V output: 20/40mΩ
- Compact Package: QFN2×2-10

Applications

- All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment

Typical Applications

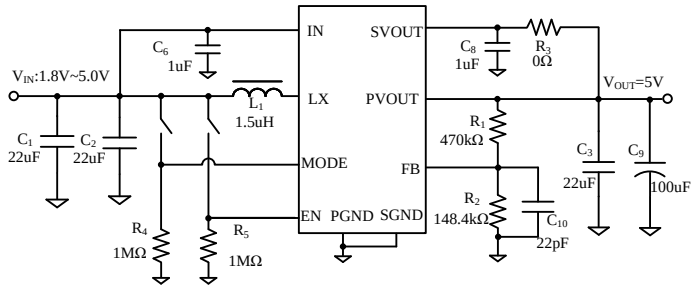


Figure 1. Schematic Diagram

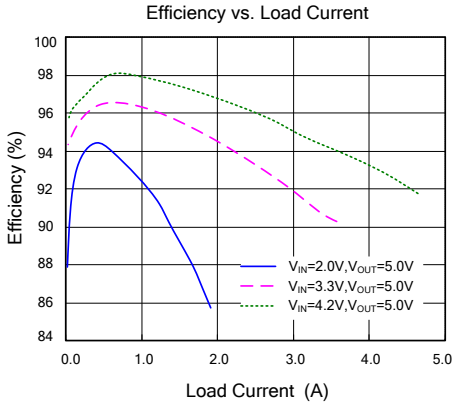
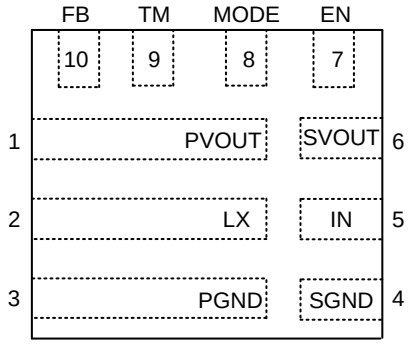


Figure 2. Efficiency Figure

Pinout (top view)



(QFN2×2-10)

Top mark: **XZ*xyz*** (Device code: XZ, ***x=year code, y=week code, z= lot number code***)

Name	QFN2×2-10	Description
PVOUT	1	Power output pin. Decouple this pin to the GND pin with at least a 22μF ceramic capacitor.
LX	2	Inductor node. Connect an inductor between the IN pin and the LX pin.
PGND	3	Power ground pin.
SGND	4	Signal ground pin.
IN	5	Signal input pin.
SVOUT	6	Signal output pin. Decouple this pin to the GND pin with at least a 1.0μF ceramic capacitor for noise immunity consideration.
EN	7	Enable pin. Internal integrated with a 1MΩ pull-down resistor.
MODE	8	Mode control pin. Pull this pin high to operate in fixed frequency mode and pull this pin low to allow variable frequency operation. Do not leave this pin floating.
TM	9	Test mode pin. Ties to ground or float.
FB	10	Feedback pin. Connect a resistor R_1 between OUT and FB, and a resistor R_2 between FB and GND to program the output voltage. $V_{OUT}=1.2V\times(R_1/R_2+1)$.

Absolute Maximum Ratings (Note 1)

EN---------- V_{OUT}+0.3V
Other Pins---------- 6V
Power Dissipation, P_D@ T_A=25°C QFN2×2-10----------2.5W
Package Thermal Resistance (Note 2)
θ_{JA} ----------50°C/W
θ_{JC} ----------10°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ---------- 1.8V to 5.25V
PVOUT, SVOUT---------- 2.5V to 5.5V
EN ---------- 0V to V_{OUT}+0.3V
All other pins ---------- 0-5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =2.4V, V_{OUT}=5V, I_{OUT}=500mA, T_A = 25°C unless otherwise specified)

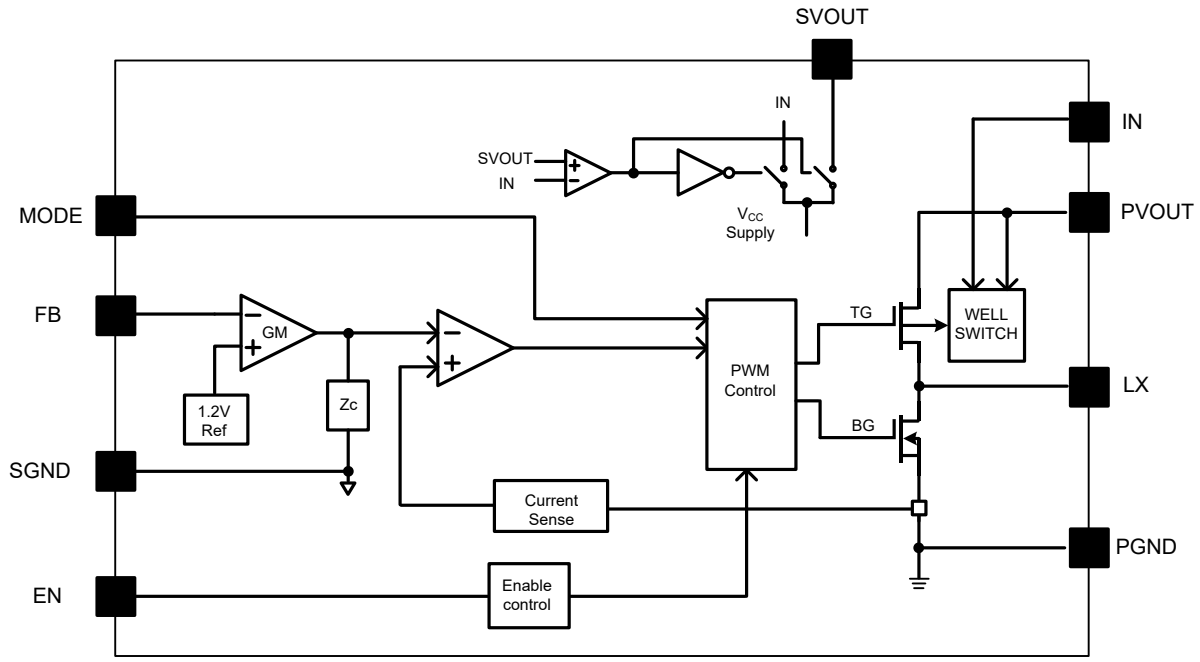
Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		1.8		5.25	V
Output Voltage Range		V_{OUT}		2.5		5.5	V
Quiescent Current	V_{IN}	I_Q	Io=0A,V_{EN}=V_{IN}=1.8V, V_{OUT}=5.0V		10		μA
	V_{OUT}				27		μA
Shutdown Current		I_{SHDN}	V_{EN}=0V, V_{IN}=2.4V		0.1	1	μA
Linear Charge Current		I_{CHARGE}	V_{OUT}≤1V		1.2		A
			1V<V_{OUT}<90%V_{IN}		1.0		
Soft-start Time		tss			1		ms
Input UVLO Threshold		V_{UVLO}				1.78	V
Input UVLO Hysteresis		V_{HYS}			0.1		V
EN Rising Threshold		V_{ENH}		1.2			V
EN Falling Threshold		V_{ENL}				0.4	V
MODE Rising Threshold		V_{MODE}			1.2		V
MODE Hysteresis		V_{MODE_HYS}			20		mV
Low Side Main FET R_{ON}		$R_{DS(ON)1}$	V_{OUT}=5.0V		20		mΩ
Synchronous FET R_{ON}		$R_{DS(ON)2}$	V_{OUT}=5.0V		40		mΩ
Main FET Current Limit		I_{LIM1}		6.0			A
Switching Frequency		fsw			500		kHz
Feedback Reference Voltage		V_{REF}		1.182	1.2	1.218	V
Output Over Voltage Protection		V_{OVP}			6		V
Minimum ON Time		t_{ON_MIN}			100		ns
Minimum OFF Time		t_{OFF_MIN}			100		ns
Max ON Time		t_{ON_MAX}			2		μs
Thermal Shutdown Temperature		T_{SD}			150		℃
Thermal Shutdown Hysteresis		T_{HYS}			20		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

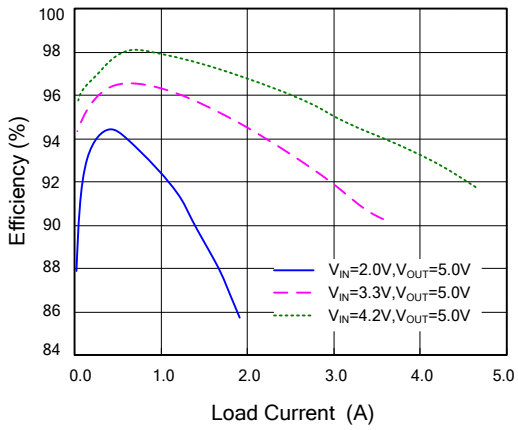
Note 3: The device is not guaranteed to function outside its operating conditions.

Block Diagram



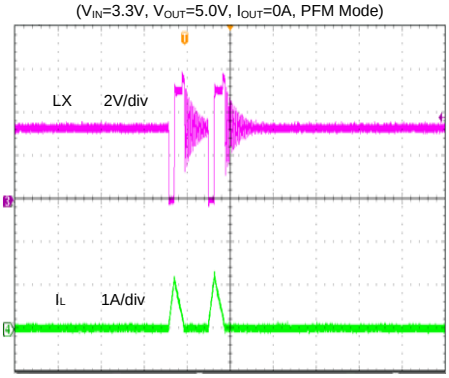
Typical Performance Characteristics

Efficiency vs. Load Current



Steady State

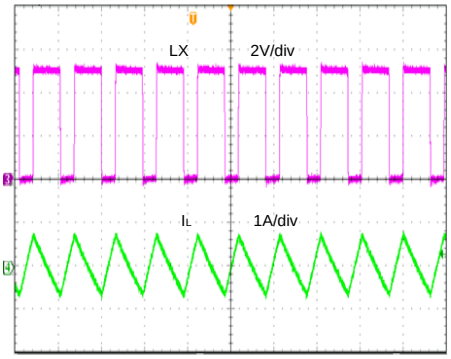
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{OUT}=0A, PFM Mode)



Time (4μs/div)

Steady State

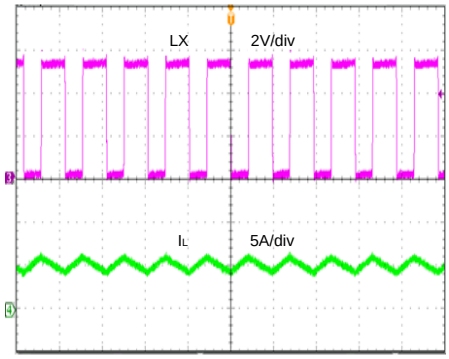
(V_{IN}=3.3V,V_{OUT}=5.0V, I_{OUT}=0A, Force PWM Mode)



Time (2μs/div)

Steady State

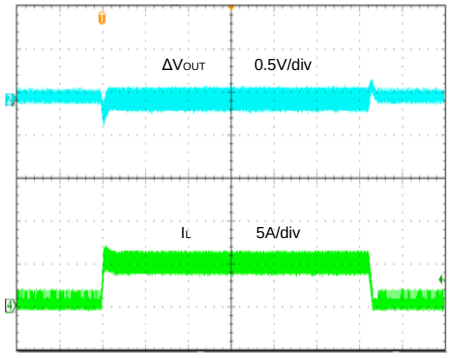
(V_{IN}=3.3V,V_{OUT}=5.0V, I_{OUT}=3.0A)



Time (2μs/div)

Load Transient

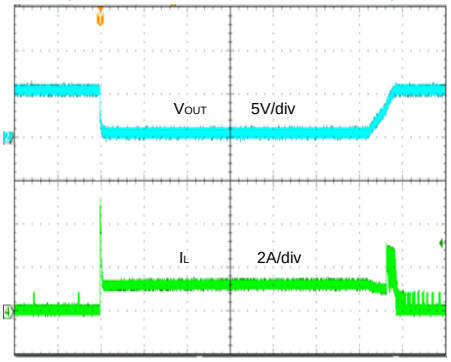
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{OUT}=0.3-3A)



Time (800μs/div)

Short Circuit

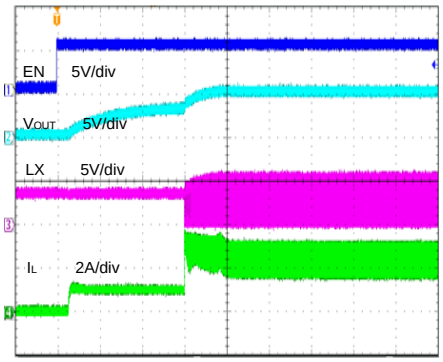
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{OUT}=0A to Short Circuit)



Time (800μs/div)

Startup from Enable

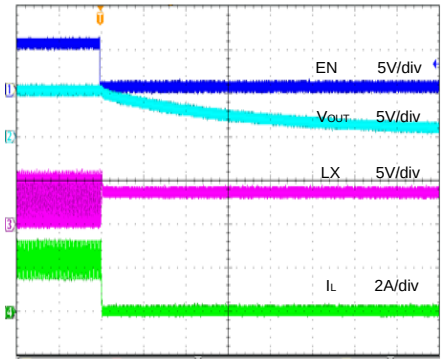
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{OUT}=1.4A)



Time (400μs/div)

Shutdown from Enable

(V_{IN}=3.3V, V_{OUT}=5.0V, I_{OUT}=1.4A)



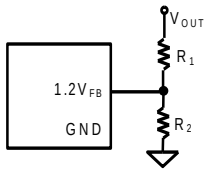
Time (100μs/div)

Applications Information

Because of the high integration for SY20466B, only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is recommended for both resistors. If V_{OUT} is 5.0V, R_1=470kΩ is chosen, using following equation, then R_2 can be calculated to be 148.4kΩ:



$$R_2 = \frac{1.2V}{V_{OUT} - 1.2V} R_1 \quad (1)$$

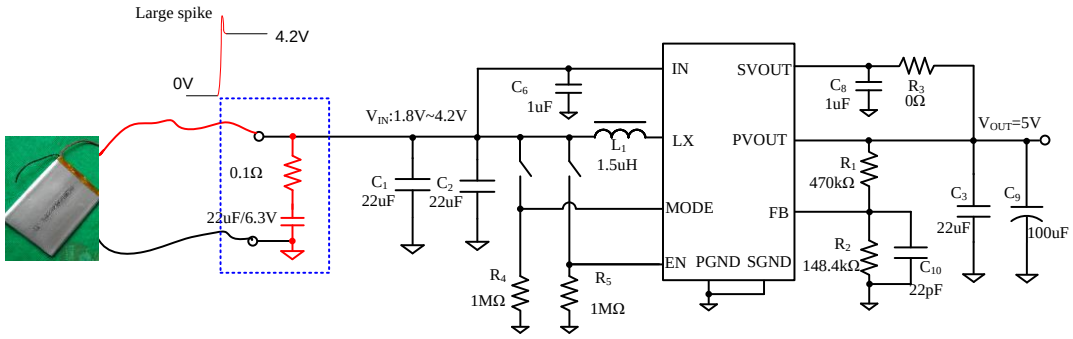
Input Capacitor C_{IN}:

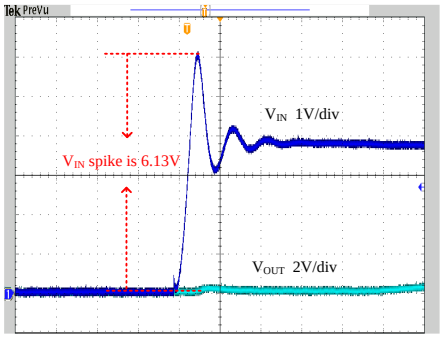
The input capacitor is selected to handle the input ripple current requirements. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and greater than 22uF capacitance.

Li-Ion Battery Hot Plug Consideration:

In the mass production stage, the Li-Ion Battery will always hot plug in between IC IN and GND pin. The hot plug may lead to large voltage spike and even lead to IC EOS fail. To avoid this potential risk, 1pcs 22uF ceramic cap serial with 0.1Ω resister is recommended to absorb the input voltage spike.

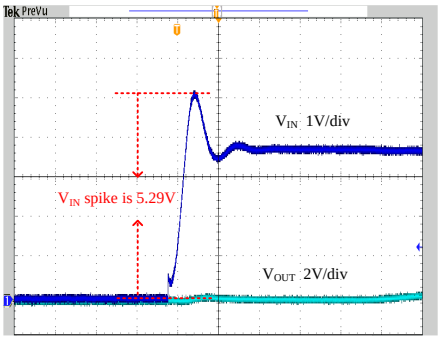
With the recommended input absorb solution, the voltage spike can be reduced from 6.13V to 5.29V.





Time (10us/div)

C_{IN}=22uF/6.3V*2



Time (10us/div)

C_{IN}=22uF/6.3V*2 // (22uF+0.1Ω)

Inductor L Selection:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = (\frac{V_{IN}}{V_{OUT}})^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT,MAX} \times 40\%} \quad (2)$$

where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current. The SY20466B regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

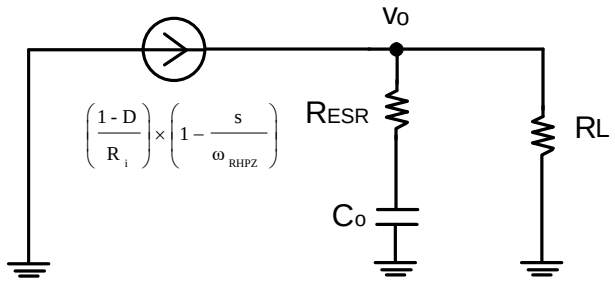
$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L} \quad (3)$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Inductor vs. Output Capacitor:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. Care should be taken to minimize the loop area formed by COUT, and OUT/GND pins. It's recommended to use a X5R or better grade ceramic capacitor with 10V rating and great than 22uF capacitance to decouple the high frequency current. And also a tantalum capacitor with 16V rating and great than 100uF capacitance is recommended for the stability consideration.

All continuous mode boost converters have a right half plane zero (RHPZ) due to the inductor being removed from the output during charging. In a converter with current mode control, inner current feedback loop allows the switch, inductor and modulator to be lumped together into a small signal variable current source, shown as fallow.



the power stage approximate transfer function is:

$$G_c(s) = \frac{(1-D) \times R_L}{R_i} \times \frac{\left(1 + \frac{s}{\omega_{ESR}}\right)\left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_p}} \quad (4)$$

Where

$$\omega_{ESR} = \frac{1}{R_{ESR} C_O} \quad (5)$$

$$\omega_P = \frac{1}{(R_{ESR} + R_L) \times C_O} \quad (6)$$

$$\omega_{RHPZ} = \frac{R_L}{L} \times \left(\frac{V_{IN}}{V_{OUT}} \right)^2 \quad (7)$$

As the equation 4 shows, Boost convert with current mode control transfer function is consist of one ESR zero, one right half plane zero and one pole. Right half plane zero brings 20dB/decade gain increase, 90 degrees phase drop. So the bandwidth of boost converter MUST be lower than f_{RHPZ}.

As shown in equation 7, right half plane zero is depending on R_L, L and duty cycle. Larger inductor lead to lower f_{RHPZ}, so bandwidth should be designed lower than f_{RHPZ}.

Some low profile application may prefer to use the ceramic capacitor solution and some low cost application may use the Electrolytic cap to reduce the BOM cost.
Below is selection table based on different inductance and output capacitor.

Inductance vs. Output Capacitor Selection Table

Inductance		Low profile capacitor application		Low cost capacitor application
Part Number	L(μH)	Part Number	C_{OUT} (μF)	C_{OUT} (μF)
SPM6530T-1R0M	1.0	C3216X5R1A226M	22μF/10V×3pcs	22μF/10V+100uF(E-cap)
SPM6530T-1R5M	1.5	C3216X5R1A226M	22μF/10V×4pcs	22μF/10V+100uF(E-cap)
SPM6530T-2R2M	2.2	C3216X5R1A226M	22μF/10V×5pcs	22μF/10V+200uF(E-cap)

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY20466B shutdown current drops to lower than 1uA, driving the EN pin high (> 1.2V) will turn on the IC again.

Layout Design Consideration:

For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, C_{OUT}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to PGND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly recommended.

2) C_{OUT} must be close with Pins PVOUT and PGND. The loop area formed by C_{OUT} and GND must be minimized.

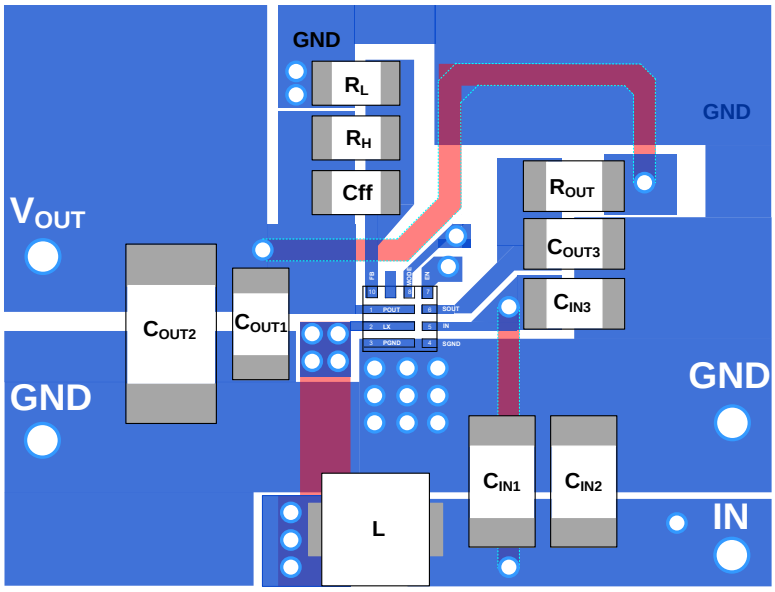
3) To minimize the output decouple loop area, LX trace is recommended to be routed on bottom or middle layer through via.

4) SVOUT is the power supply pin for the internal control circuit. Don't connect to PVOUT pin directly. A 4.7uF ceramic cap is strongly recommended to decouple SVOUT pin to SGND pin. Please use a jump wire to connect SVOUT pin to output capacitor side.

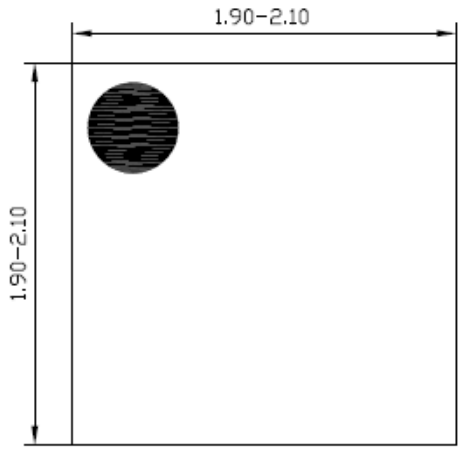
5) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

6) The components R_1 and R_2 and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

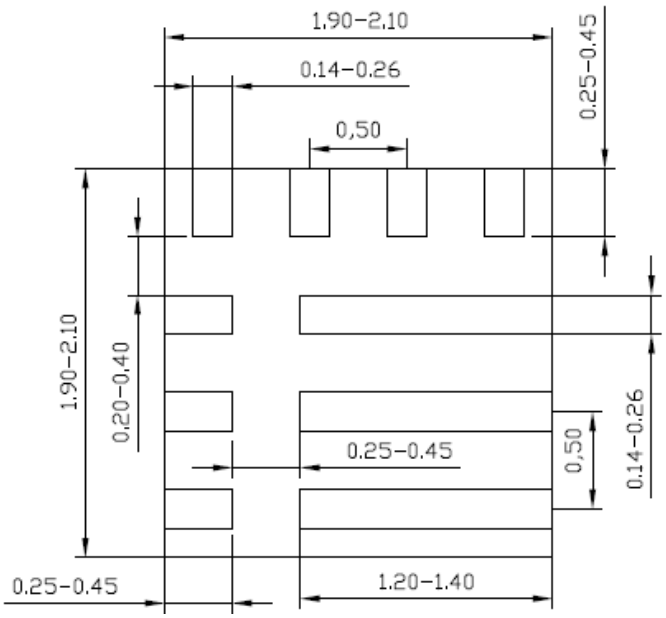
PCB Layout Suggestion



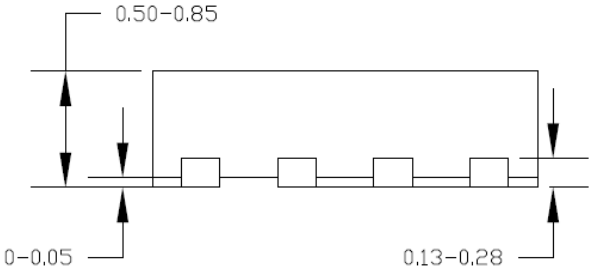
QFN2×2-10 Package Outline



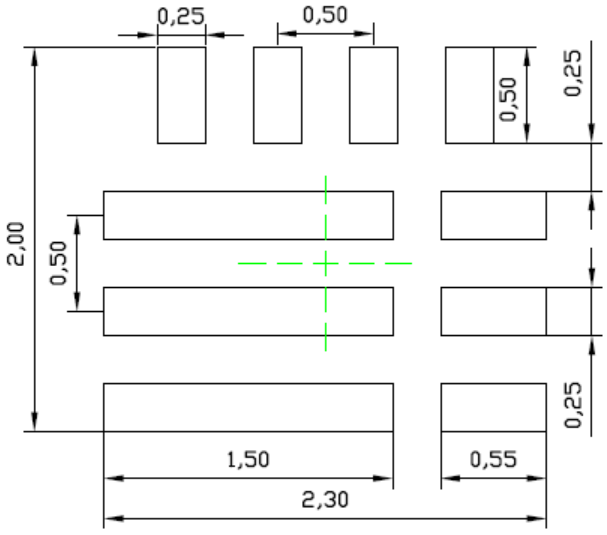
Top View



Bottom View



Side View



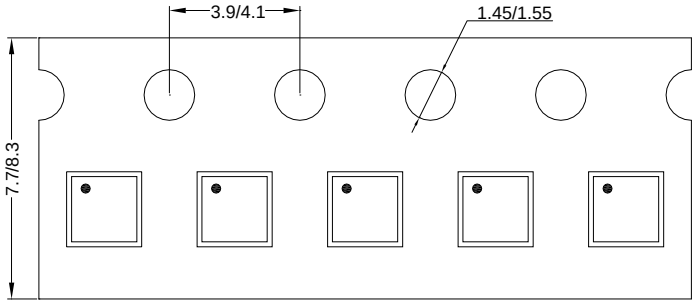
Recommended PCB Layout (Reference only)

Notes: All dimension in MM and exclude mold flash & metal burr

Taping & Reel Specification

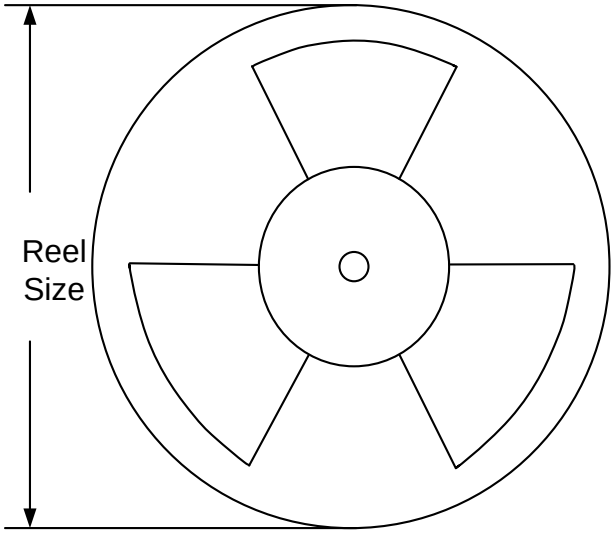
1. Taping orientation

QFN2×2



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2x2	8	4	7"	400	160	3000

3. Others: NA

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