SY21305

High Efficiency, 15A Synchronous Step Up Regulator with Accurate Output Current Limit

General Description

SY21305 develops a high efficiency synchronous Boost regulator with programmable output current limit. The device adopts adaptive constant off time and current mode control. The integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

SY21305 features cycle by cycle peak current limit, output short circuit protection and true shutdown. The device also provides enable control and power good indicator for system sequence control. Low output voltage ripple and small external inductor and capacitor size are achieved with programmable pseudo-constant frequency.

Ordering Information

SY21305□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21305RDC	QFN4x4-18	----

Features

- Input Range: 3-16V
- Programmable Pseudo-constant Frequency
- Low $R_{DS(ON)}$ Internal Switch
  Main FET: 16mΩ
  Rectified FET: 18mΩ
  Disconnection FET: 18mΩ
- True Shutdown Function
- Programmable Output Current Limit
- Internal Soft-start Limits The Inrush Current
- Input Voltage UVLO
- Over Temperature Protection
- Over Voltage Protection
- Output Short Circuit Protection
- Minimum ON Time: 100ns typical
- Minimum OFF Time: 120ns typical
- RoHS Compliant and Halogen Free
- Compact Package:QFN4x4-18

Applications

- Power Bank
- High Power AP

Typical Application

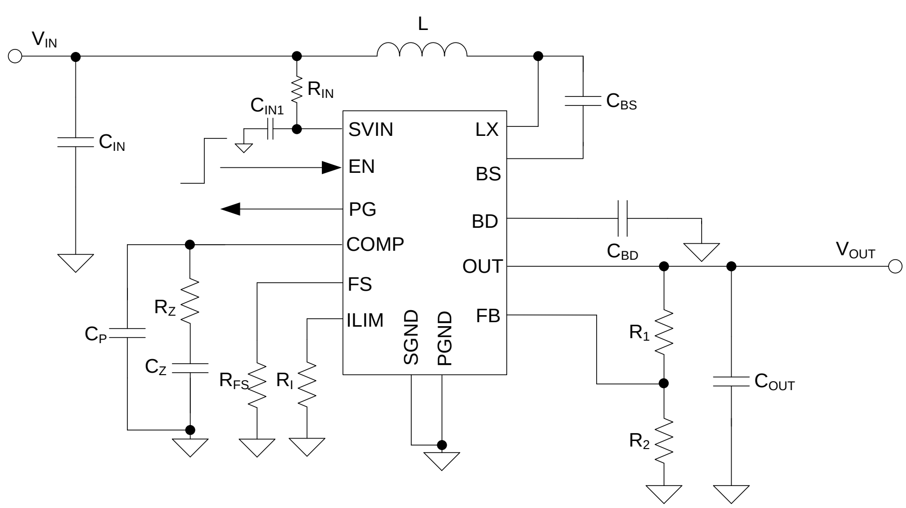
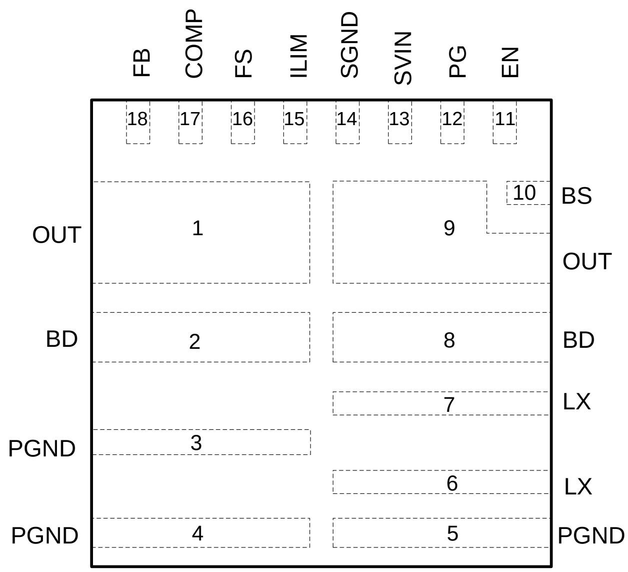


Figure1. Schematic Diagram

Pinout (top view)



(QFN4x4-18)

Top mark: **BDU*xyz*** (Device code: BDU, ***x=year code, y=week code, z= lot number code***)

Pin Name	QFN4x4-18	Pin Description
SVIN	13	IC power supply input pin. Decouple this pin to the SGND pin with a 1μF ceramic capacitor.
SGND	14	Signal ground pin.
PGND	3,4,5	Power ground pin.
LX	6,7	Inductor node. Connect an inductor from power input to the LX pin.
FB	18	Feedback pin. Connect to the center of resistor voltage divider to program the output voltage: $V_{OUT}=1V\times(R1/R2+1)$
EN	11	Enable control. Pull high to turn on the IC. Do not leave it floating.
ILIM	15	Output current limit program pin. Connect a resistor R_{LIM} from this pin to SGND to program output current limitation threshold. $I_{LIM}(A)=30(V)/R_{LIM}(k\Omega)$
OUT	1,9	The boost converter output pin.
BD	2,8	Connect to the Drain of internal Disconnect FET. Bypass at least 4.7uF ceramic cap to PGND.
BS	10	Boot-strap pin. Supply Rectified FET's gate driver. Decouple this pin to LX with a 0.1μF ceramic capacitor. Do not connect a resistor in series with the capacitor.
FS	16	Switching frequency setting pin. Connect a resistor from this pin to ground to program the switching frequency. $f_{SW}(kHz)=1.4\times10^6/R_{FS}(\Omega)^{0.645}$.
PG	12	Power good indicator. Open drain output, pull low when the output < 90% of regulation voltage, high impendence otherwise.
COMP	17	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.

Block Diagram

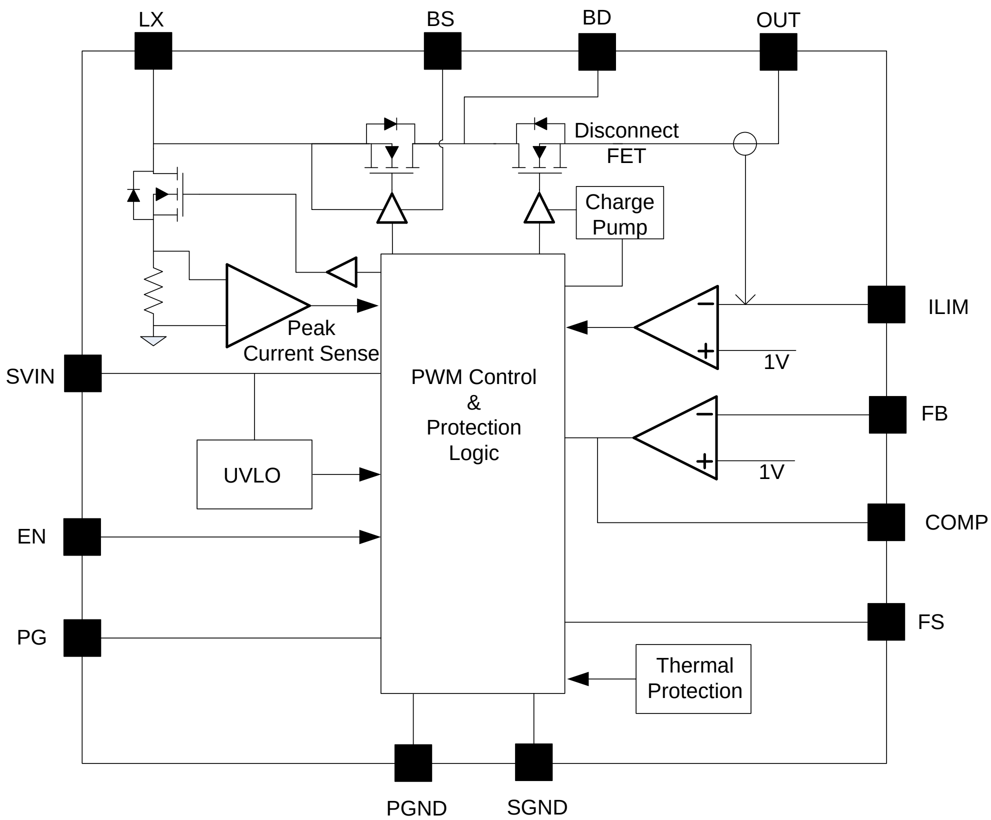


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

SVIN, LX, EN, ILIM, OUT, BD, BS, FS, PG, COMP -------------------- -0.3V to 18V
FB-------------------- 4V
BS-LX -------------------- 4V
Power Dissipation, P_D @ T_A = 25°C, QFN4x4-18--------------------3.4W
Package Thermal Resistance (Note 2)
θ_{JA} -------------------- 30°C/W
θ_{JC} -------------------- 3.2°C/W
Junction Temperature Range -------------------- -40°C to 125°C
Lead Temperature (Soldering, 10 sec.) -------------------- 260°C
Storage Temperature Range -------------------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

SVIN -------------------- 3V to 16V
Junction Temperature Range -------------------- - 40°C to 125°C
Ambient Temperature Range -------------------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =5V, V_{OUT}=12V, I_{OUT}=100mA, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3		16	V
Output Voltage Range	V_{OUT}		V_{IN}×1.1		18	V
Output OVP Threshold	V_{FB_OVP}	V_{FB} Rising	110%	115%	120%	V_{REF}
Quiescent Current	I_Q	V_{OUT}=13V			220	μA
Shutdown Current	I_{SHDN}	EN=0			5	μA
FB Leakage Current	I_{FB}		-50		50	nA
Main N-FET RON	$R_{DS(ON)\_M}$			16		mΩ
Rectified N-FET RON	$R_{DS(ON)\_R}$			18		mΩ
Disconnect N-FET RON	$R_{DS(ON)\_D}$			18		mΩ
Main N-FET Current Limit	$I_{LIM,PEAK}$		15		20	A
Switching Frequency	F_{SW}	R_{FS}=390kΩ		345		kHz
Switching Frequency Programmable Range	$F_{SW,RNG}$		250		1000	kHz
Feedback Reference Voltage	V_{REF}		0.985	1	1.015	V
IN UVLO Rising Threshold	$V_{IN,UVLO}$				2.85	V
UVLO Hysteresis	$V_{HYS,UVLO}$			0.2		V
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Output Current Limit Reference Voltage	V_{LIM}			1		V
Output Current Limit Programmable Range	$I_{LIM,OUT}$	V_{OUT}<=5V	1		5	A
		V_{OUT}>5V	1		4	A
Minimum ON Time	$t_{ON,MIN}$			100		ns
Minimum OFF Time	$t_{OFF,MIN}$			120		ns
Error Amplifier Trans-conductance	g_m			100		μS
Current Sense Gain	R_i			75		mΩ
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

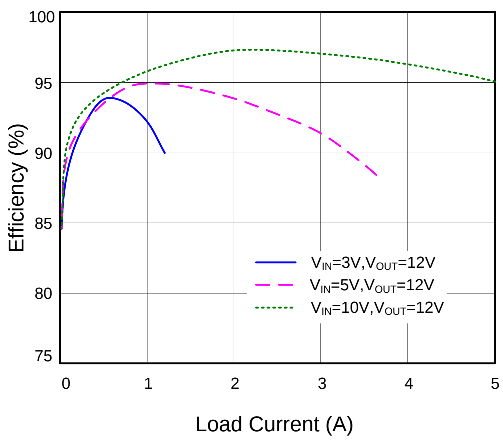
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

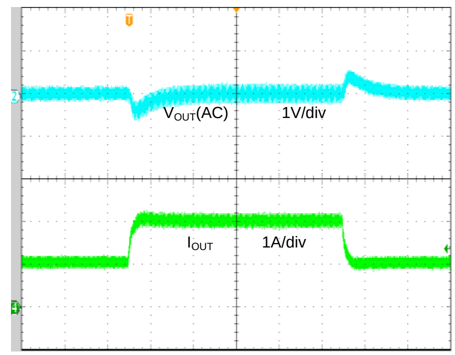
Typical Performance Characteristics

Efficiency vs. Load Current



Load Transient

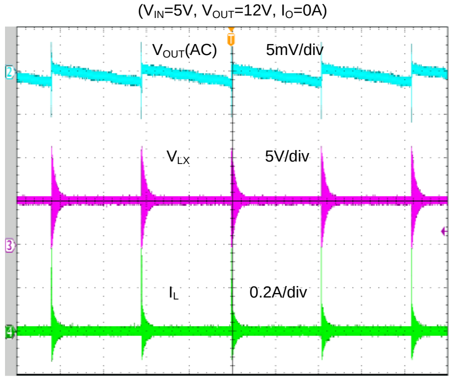
(V_{IN}=5V, V_{OUT}=12V, I_O=1 ~ 2A)



Time (200μs/div)

Output Ripple

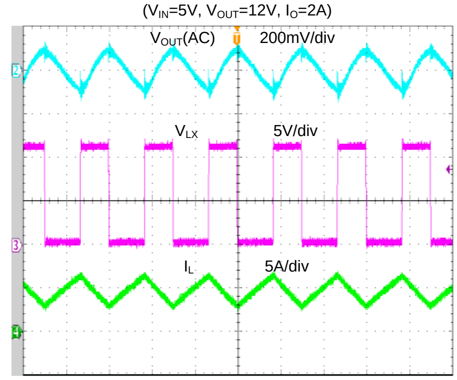
(V_{IN}=5V, V_{OUT}=12V, I_O=0A)



Time (40μs/div)

Output Ripple

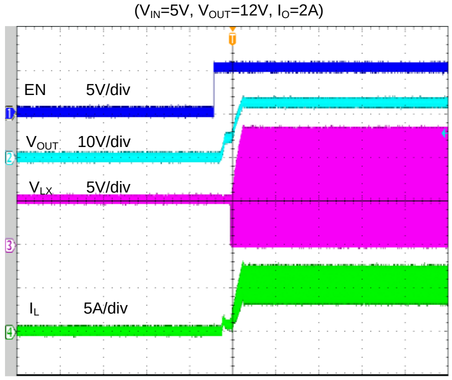
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (2μs/div)

Startup from Enable

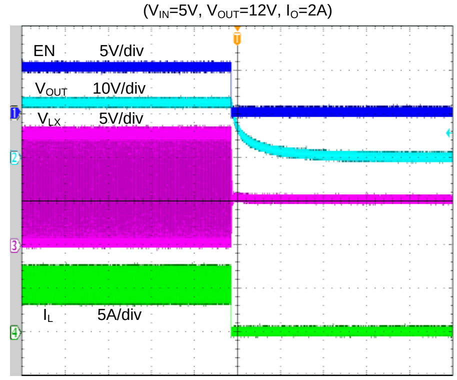
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (4ms/div)

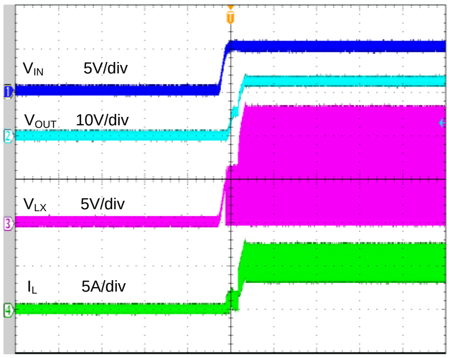
Shutdown from Enable

(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



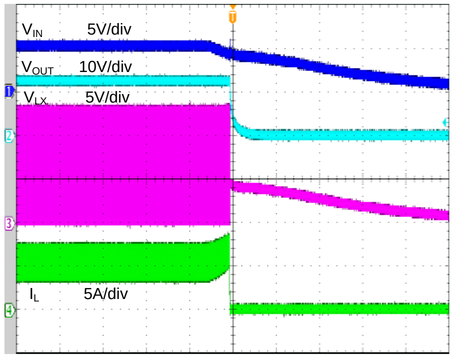
Time (400μs/div)

Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



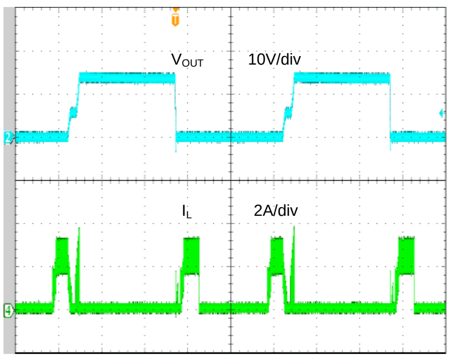
Time (4ms/div)

Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



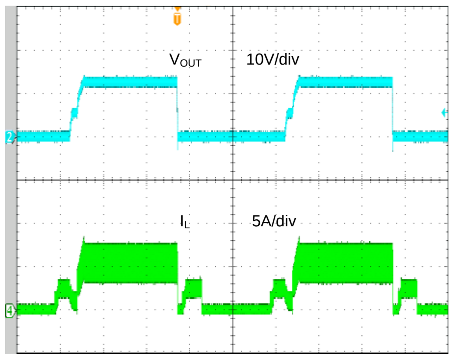
Time (2ms/div)

Short Circuit Protection
(V_{IN}=5V, V_{OUT}=12V, I_O=0A ~ short)



Time (4ms/div)

Short Circuit Protection
(V_{IN}=5V, V_{OUT}=12V, I_O=2A ~ short)



Time (4ms/div)

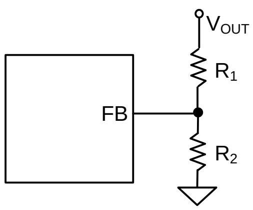
Applications Information

Because of the high integration in SY21305, the application circuit based on this regulator is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output current limit resistor R_{LIM}, switching frequency program resistor R_{FS}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback Resistor Divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10k and 1M is recommended for both resistors. If R_1=200k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{R_1}{V_{OUT} - 1}(\Omega)$$



Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}(A)$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the VIN and PGND pin. Care should be taken to minimize the loop area formed by C_{IN}, VIN, and PGND pin. In this case a 10uF low ESR ceramic capacitor is recommended.

The SVIN capacitor must be close to the SVIN and SGND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by C_{IN1}, and SVIN/SGND pins. In this case a 2uF low ESR ceramic is recommended.

Boost Output Capacitor C_{BD} and Disconnection FET Output Capacitor C_{OUT}

The Boost Output capacitor C_{BD} and disconnection FET Output capacitor C_{OUT} are selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into account when selecting these capacitors. For the best performance, it is recommended to use an X5R or a better grade ceramic capacitor with 25V rating and more than 22µF capacitors.

Boost Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT\_MAX} \times 40\%}(H)$$

Where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

SY21305 regulator IC is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,\,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good overall efficiency.

Switching Frequency

The switching frequency of SY21305 in CCM can be programmed by adjusting external resistor R_{FS} connected to FS pin:

$F_{SW}(kHz)=1.4\times10^6/R_{FS}(\Omega)^{0.645}$.

Under light load condition, SY21305 linearly fold back the frequency, thus minimize the output ripple.

Enable Operation

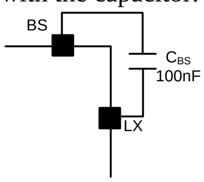
Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, Driving the EN pin high (>1.5V) will turn on the IC again.

Power Good Indication

PG is an open-drain output pin. This pin will pull to ground if output voltage is lower than 90% of regulation voltage or OVP is triggered. Otherwise this pin will go to a high impedance state.

External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal rectifier. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended. Do not connect a resistor in series with the capacitor.



Output Current Limit

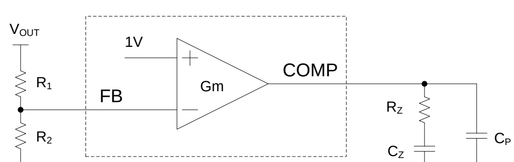
There are two feedback loops inside the regulator. When the voltage on ILIM pin meets 1V threshold, the current feedback loop will take over and regulate the output DC current to the target value.

$I_{LIM}(A)=30(V)/R_{LIM}(k\Omega)$.

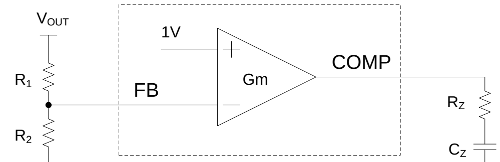
Loop Compensation

The SY21305 incorporates constant off time current mode control scheme. The current mode control scheme has two feedback loops. The inner loop, current loop, does not require any external compensation component. The outer loop, voltage loop, is compensated with external components.

In most applications, a Type 2 or Type 2a compensation network shown below can be used to stabilize the voltage loop. The Type 2 is the most widely used and works fine for power stages lagging down to -90˚ and where the boost brought by the output capacitor ESR must be canceled. Type 2a is used where the output capacitor ESR effect can be neglected.



Type 2



Type 2a

Follow the steps below to calculate the value of external components for voltage loop compensation.

1. Select the crossover frequency fc of the closed loop. It is recommend that the crossover frequency is chosen to be the minimum value of 1/5 of right half plane zero (f_{RHPZ}) and 1/10 of switching frequency for the tradeoff of stability and transient response of the system. The system has faster response at higher crossover frequency.

$$f_{RHPZ} = \frac{(1-D_{MAX})^2 \times V_{OUT}}{2\pi \times L \times I_{OUT}}$$

2. Select a Rz value of the R-C series combination connected to the COMP pin.

$$R_Z = \frac{V_{OUT}}{g_m \times G_{fc} \times V_{REF}}$$

Where g_m is the error amplifier trans-conductance, which is typically 100uS; G_{fc} is gain of the power stage at crossover frequency.

$$G_{fc} = \frac{(1-D_{MAX})}{2\pi \times fc \times C_{OUT} \times R_i}$$

Where R_i is the current sense gain, which is typically 75mΩ.

3. Select a Cz value of the R-C series combination connected to the COMP pin. The compensation zero decides phase margin at the crossover frequency. Place a compensation zero at or before the dominant pole of R_L and C_O. R_L is the load resistance, which equals to V_{OUT}/I_{OUT}.

$$C_Z = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_Z}$$

4. A high frequency pole is recommended to attenuate the high frequency noise. Place this pole to cancel the ESR zero of C_{OUT}

$$C_P = \frac{R_{ESR} \times C_O}{R_Z}$$

Layout Design

The layout design of SY21305 regulator is highly simplified. To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, C_{BD}, C_{OUT}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to PGND pin to achieve a better thermal performance and noise immunity. If the board space allowed, a designated ground plane layer is highly recommended.

2) C_{IN} must be close to SVIN and SGND pins. The loop area formed by C_{BD}, LX and PGND pins must be minimized.

3) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

4) The components R_1 and R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the SVIN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor across the EN and SGND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

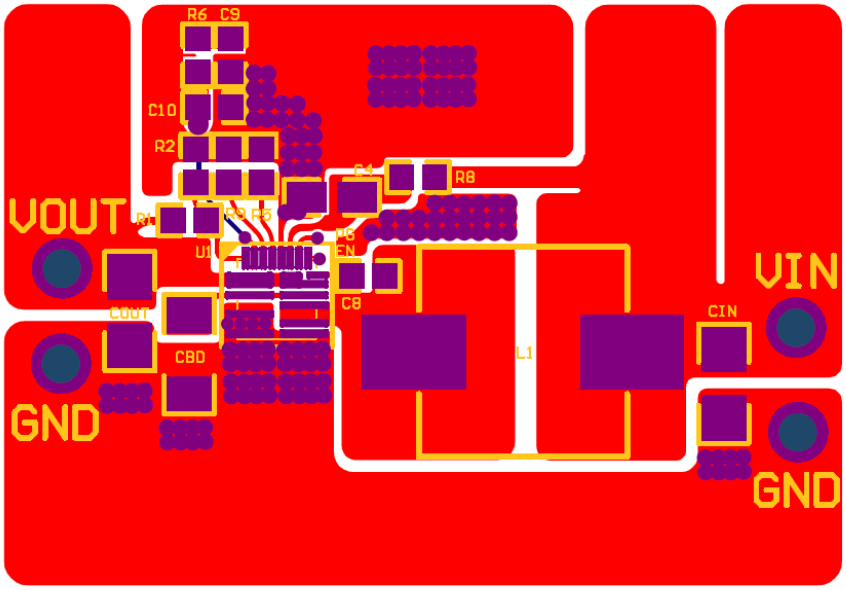
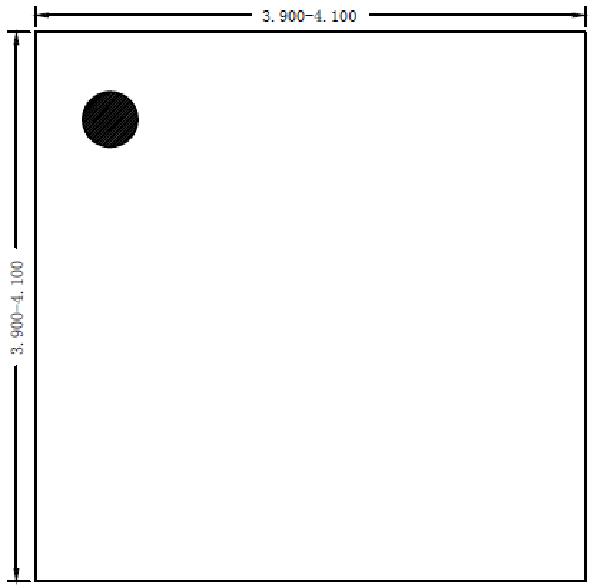
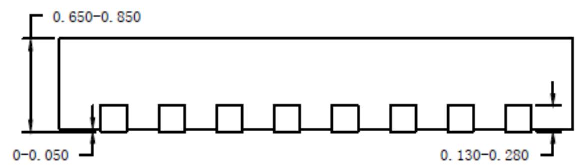


Figure3. PCB Layout Suggestion

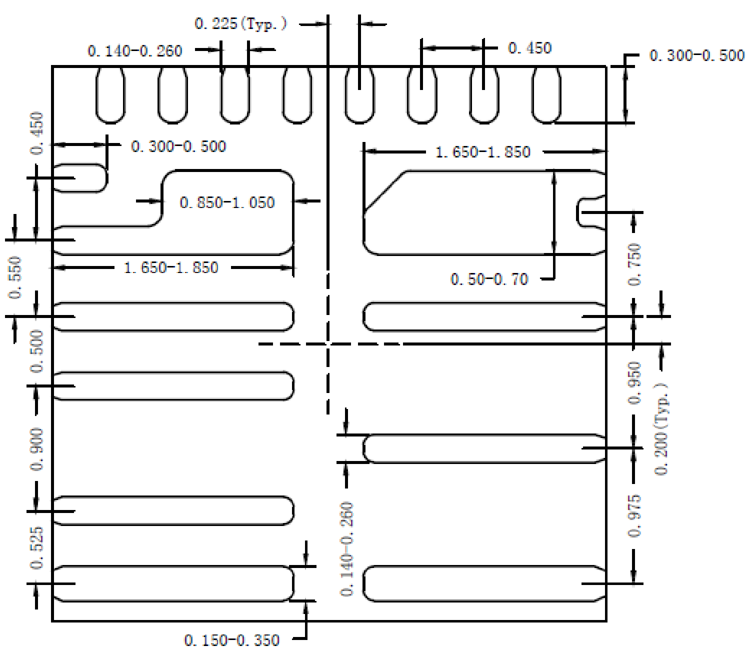
QFN4x4-18 Package Outline Drawing



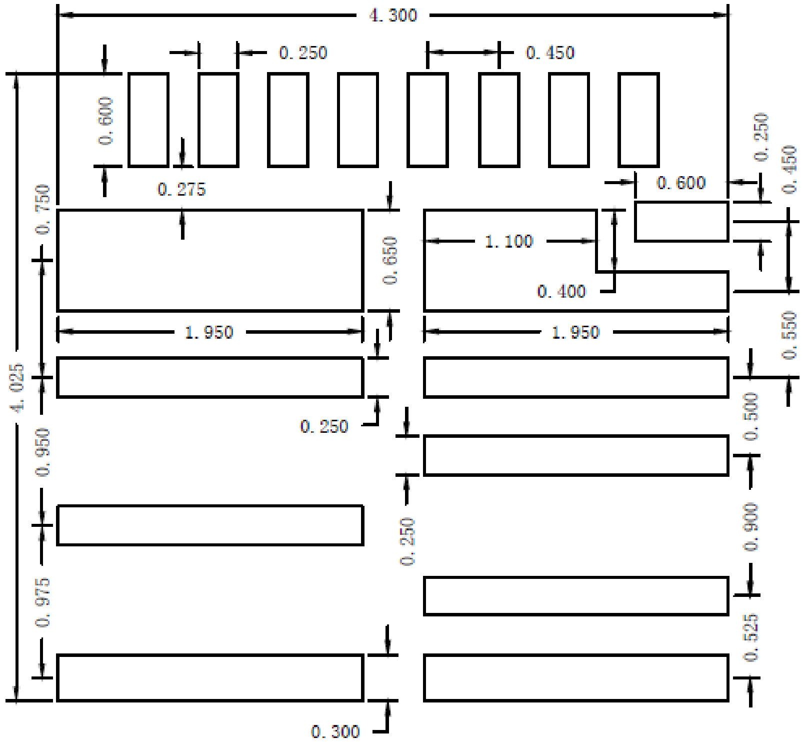
Top View



Side View



Bottom View



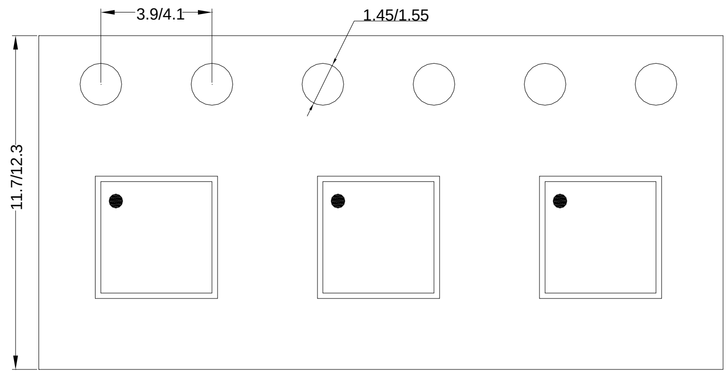
Recommended PCB layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

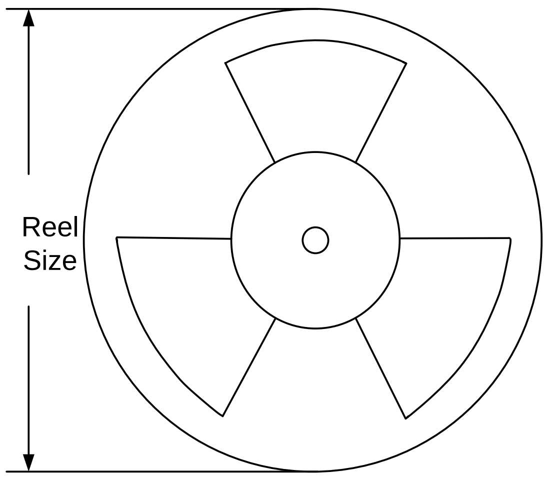
1. Taping orientation

QFN4x4



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4x4	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 13, 2025	Revision 1.0	Add the following description to the BS pin description (Page2) and the External Bootstrap Capacitor application information (page 8): ---- Do not connect a resistor in series with the capacitor.

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