

General Description

SY205218 is a low-capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With a typical capacitance of 4pF, SY205218 is designed to protect against over-voltage and over-current transient events. It complies with IEC61000-4-2 (ESD) ($\pm 30\text{kV}$ air, $\pm 30\text{kV}$ contact discharge), IEC61000-4-5 (surge) (4A, 8/20 μs), etc.

Each SY205218 device can protect one data line. SY205218 is available in small DFN1.0x0.6-2 and DFN0.6x0.3-2 packages.

Features

- Protects One Data, Control, or Power Line
- Low Capacitance: 4pF (Typical)
- Low Leakage Current: 0.01 μA @ V_{RWM} (Typical)
- Low Clamping Voltage
- Transient Protection for High-speed Data Lines
 - IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (Air) $\pm 30\text{kV}$ (Contact)
 - IEC 61000-4-5 (Surge) 4A (8/20 μs)
- For Operating Voltage of 12V and Below
- Package Optimized for High-Speed Lines
- Ultra Small Packages: DFN1.0x0.6-2/DFN0.6x0.3-2
- Each I/O pin can withstand over 1000 ESD strikes for $\pm 8\text{kV}$ contact discharge.

Applications

- Portable Electronics
- Desktops, Servers, and Notebooks
- Cellular Phones
- Digital Camera Ports

Mechanical Characteristics

- DFN1.0x0.6-2 and DFN0.6x0.3-2 Packages
- Flammability Rating: UL 94V-0
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

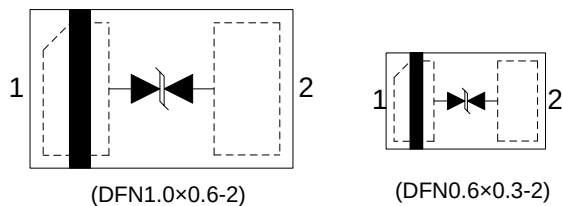
Circuit Diagram



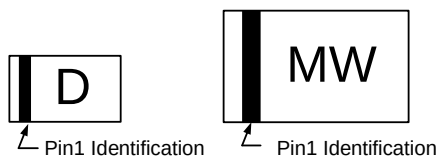
Ordering Information

Part Number	Package Type	Top Mark
SY205218DXC	DFN0.6×0.3-2 RoHS Compliant and Halogen Free	D
SY205218DWC	DFN1.0×0.6-2 RoHS Compliant and Halogen Free	MW

Pinout (Top View)



Marking Codes



Note 1: “D”, “M” is device code, fixed.

Note 2: “W” is date code

Absolute Maximum Rating				
Parameter	Symbol	Min	Max	Unit
Peak Pulse Current (8/20μs)	I_{PP}		4	A
Peak Pulse Power (8/20μs)	P_{PK}		90	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	-30	30	kV
Operating Temperature	T_{OPT}	-40	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics $T_A = 25^\circ\text{C}$						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	V_{RWM}				12.5	V
Reverse Leakage Current @ V_{RWM}	I_R	$V_{RWM} = 12\text{V}, T_A = 25^\circ\text{C}$		0.01	0.1	μA
Reverse Breakdown Voltage @ I_T	V_{BR}	$I_T = 1\text{mA}$	13.0		17	V
Clamping Voltage @ I_{PP}	$V_C (1)$	$I_{PP} = 4\text{A}, t_p = 8/20\mu\text{s}$			23	V
Clamping Voltage @ I_{PP}	$V_C (1)$	$I_{PP} = 16\text{A}, t_p = 10/100\text{ns}$		22		V
Dynamic Resistance	$R_{DYN} (1,2)$	$t_p = 10/100\text{ns}$		0.5		Ω
Parasitic Capacitance	$C_{ESD} (1)$	$V_R = 0\text{V}, f = 1\text{MHz}$		4	8	pF

Note 1: Guaranteed by design and not subject to production test.

Note 2: R_{DYN} calculated based on $I_{PP}=8\text{A}$ to $I_{PP}=16\text{A}$, $t_p = 10/100\text{ns}$.

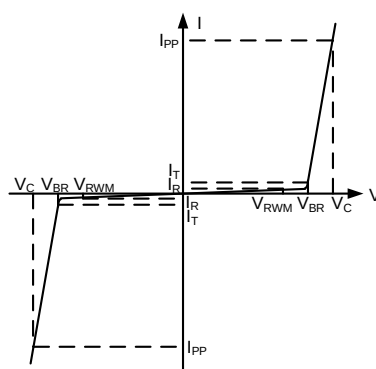
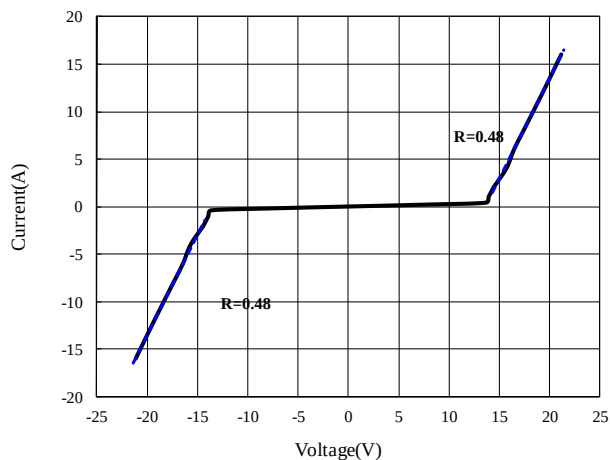


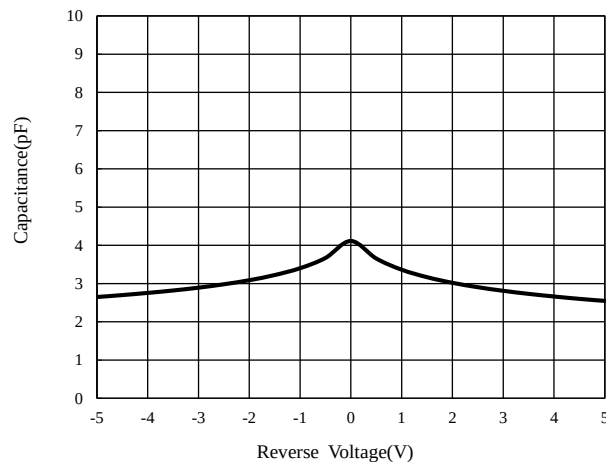
Figure 1. Bi-directional TVS

Typical Characteristics

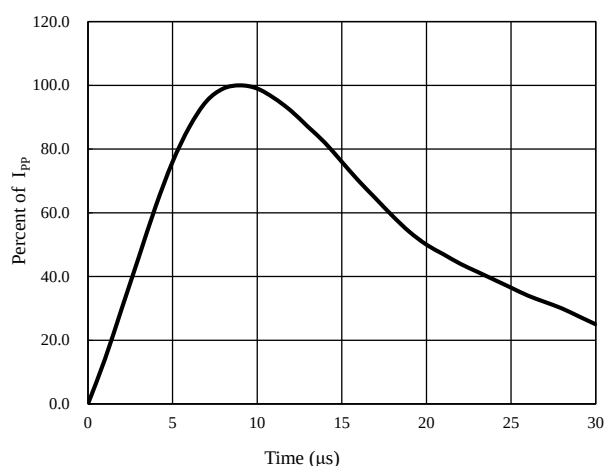
TLP Testing of I/O_1 to I/O_2



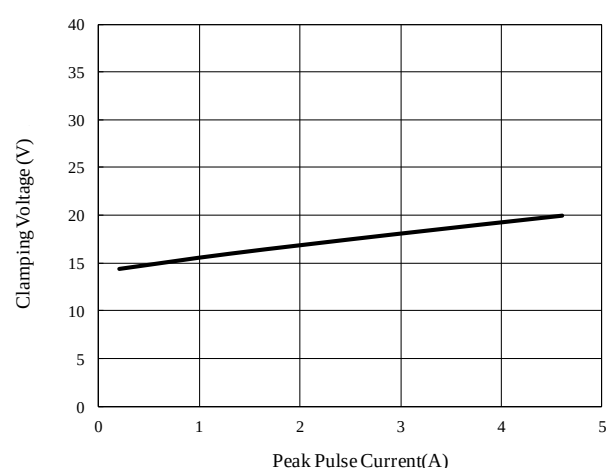
Capacitance vs. Reverse Voltage



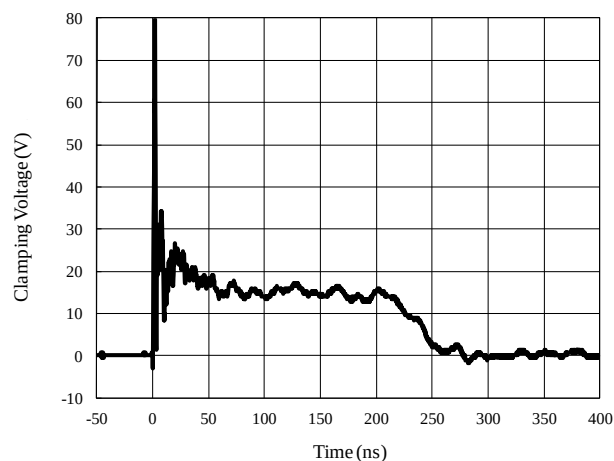
8/20 μ s Current Pulse Waveform



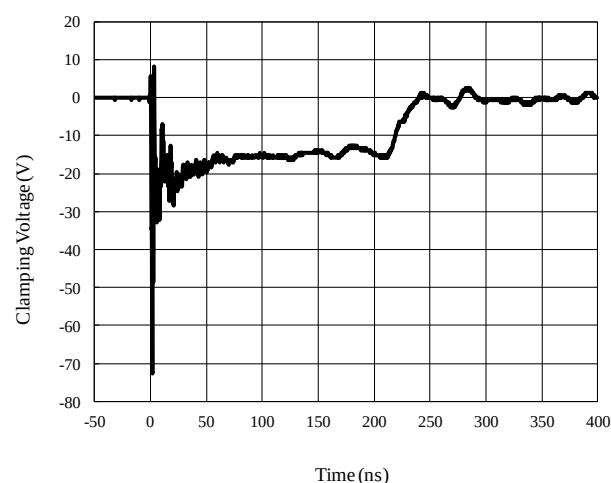
Clamping Voltage vs. Peak Pulse Current



ESD Clamping of I/O_1 to I/O_2 (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O_1 to I/O_2 (-8kV Contact per IEC 61000-4-2)



Application Information

The SY205218 protects one bidirectional low speed data line against over-voltage and over-current transient events by clamping it to an acceptable reference.

The SY205218 pin connections are shown in Figure 2. The protected line is connected at Pin1 while Pin2 is connected to GND, which should connect to a ground plane on the board. All path lengths connected to pins of SY205218 should be as short as possible to minimize the parasitic inductance.

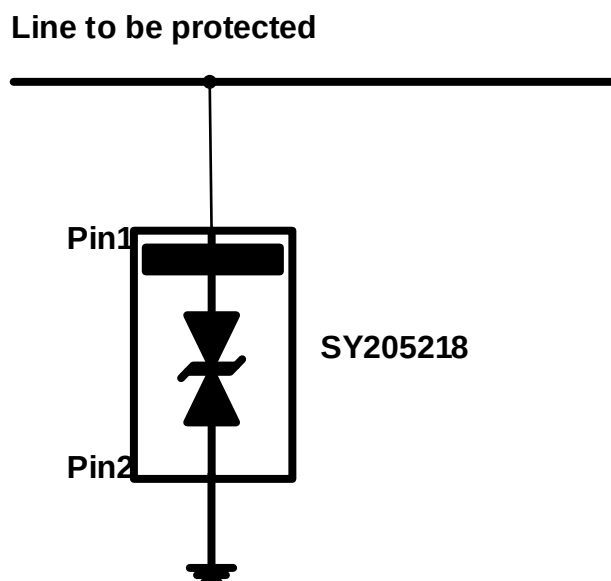


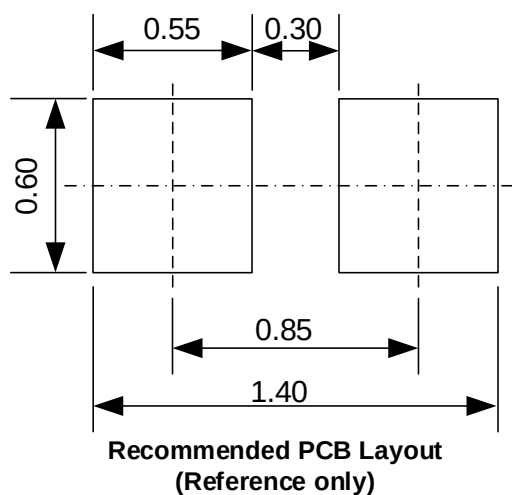
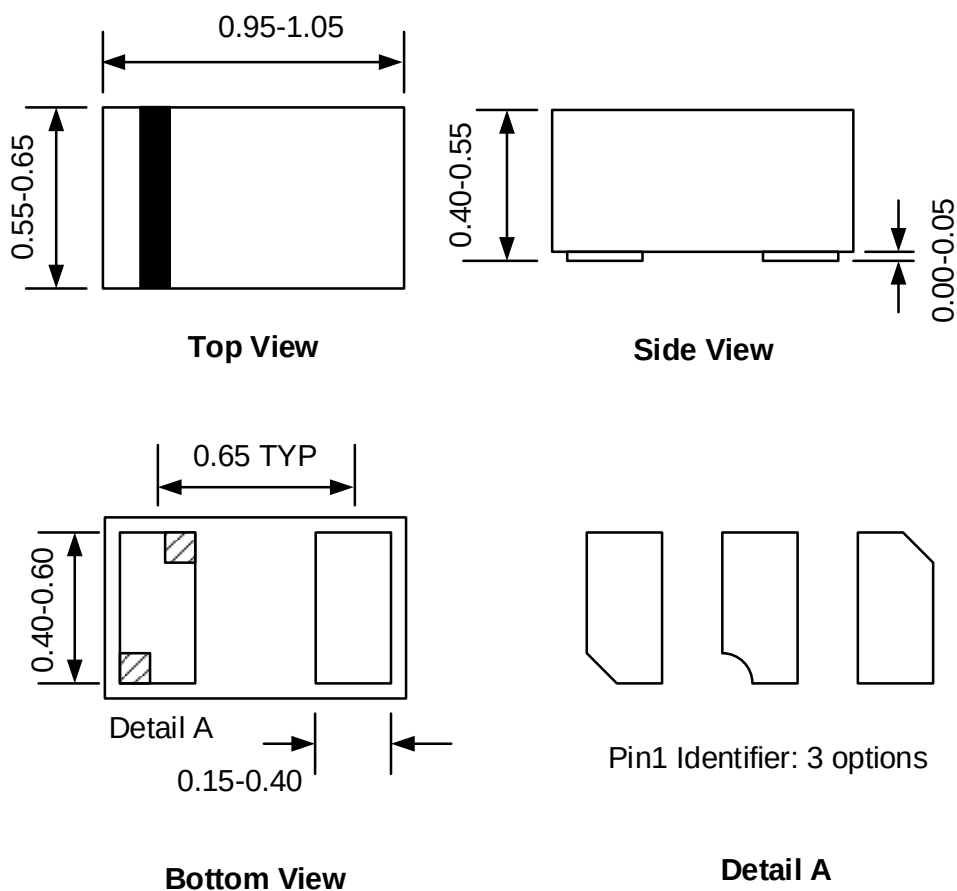
Figure 2. ESD/Surge Protection Circuit

PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following circuit board guidelines are recommended:

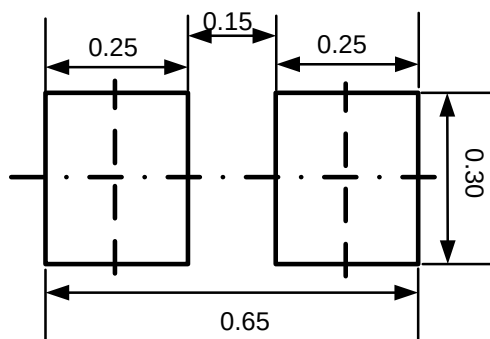
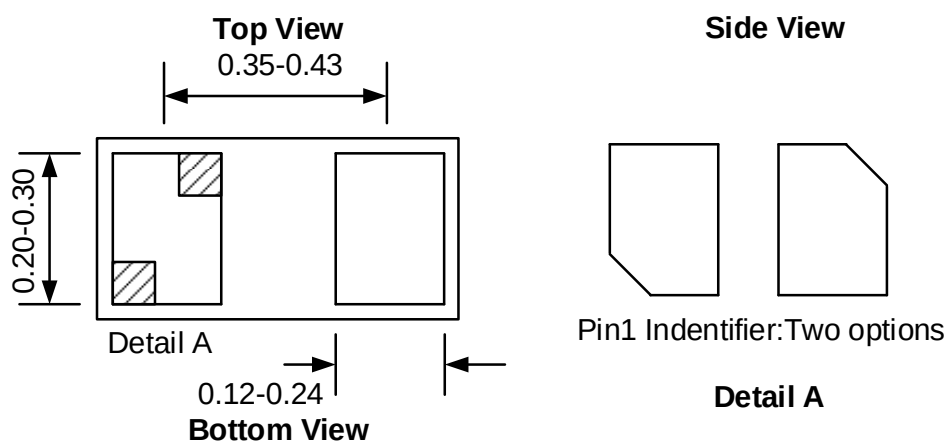
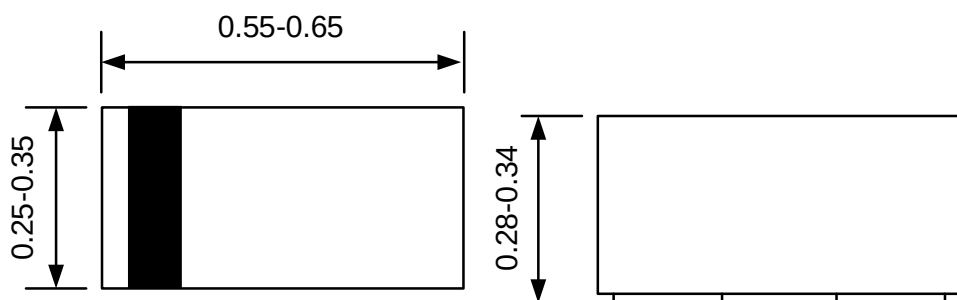
- Place SY205218 as close to the connector or terminal ports as possible.
- Use a large via to connect the SY205218 pin to the ground.
- Avoid running signals near board edges.
- The SY205218 should be placed near the protected line.
- The distance between the SY205218 ground pin and the GND reference path should be as short as possible.

DFN1.0x0.6-2 Package Outline



Note: All dimensions are in millimeters and exclude mold flash and metal burr.

DFN0.6x0.3-2 Package Outline

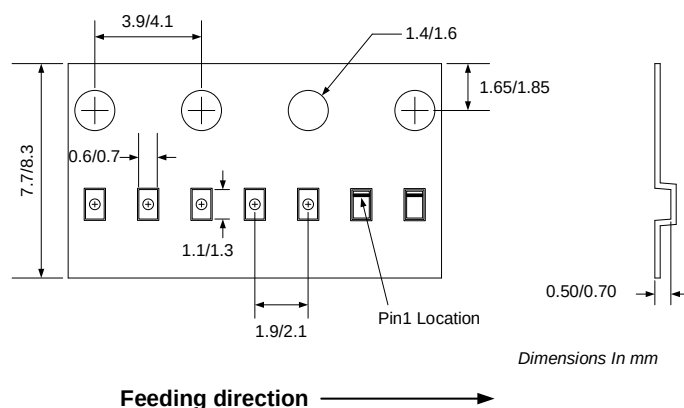


Recommended PCB Layout
(Reference only)

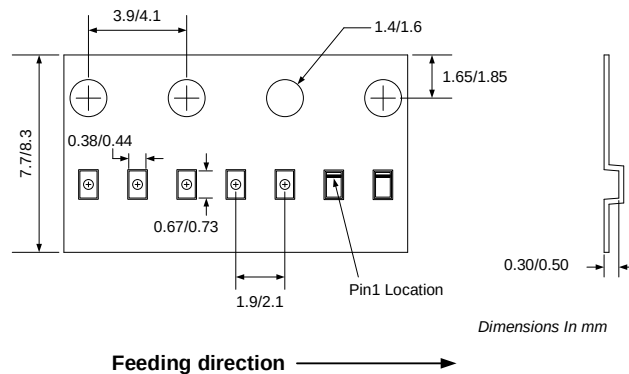
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Specification

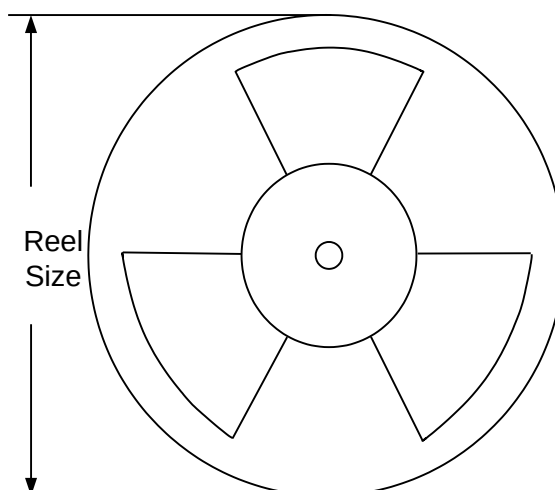
DFN1.0×0.6-2 Taping Orientation



DFN0.6×0.3-2 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel(pcs)
DFN1.0×0.6-2	8	2	7"	10000
DFN0.6×0.3-2	8	2	7"	10000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	09/11/2019	Initial Release	
1.0	09/11/2020	Production Release	

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