SY20257N

High Efficiency 5.5V, 6A, 2.4MHz I²C Programmable, Synchronous Step Down Regulator

General Description

SY20257N is a high efficiency 2.4MHz synchronous step down DC/DC regulator capable of delivering up to 6A output currents. It can operate over a wide input voltage range from 2.6V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The output voltage can be programmed from 0.6V to 1.3875V through I²C interface.

SY20257N is in a space saving, low profile CSP1.56*1.96-20 package.

Ordering Information

SY20257 □(□,□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY20257NPKC	CSP1.56*1.96-20	6A

Features

- Input Voltage Range: 2.6V to 5.5V
- 2.4 MHz Switching Frequency Minimizes the External Components
- Typical 65μA Quiescent Current
- Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 28mΩ/17mΩ
- Programmable Output Voltage: 0.6V to 1.3875V in 12.5mV Steps
- 6A Continuous Output Current Capability.
- Capable for 0.33μH or 0.25μH Inductor and 22μF Ceramic Capacitor.
- Hic-cup Mode Protection for Hard Short Condition
- RoHS Compliant and Halogen Free
- Compact package: CSP1.56*1.96-20

Applications

- Smart-phone
- Web-tablet

Typical Applications

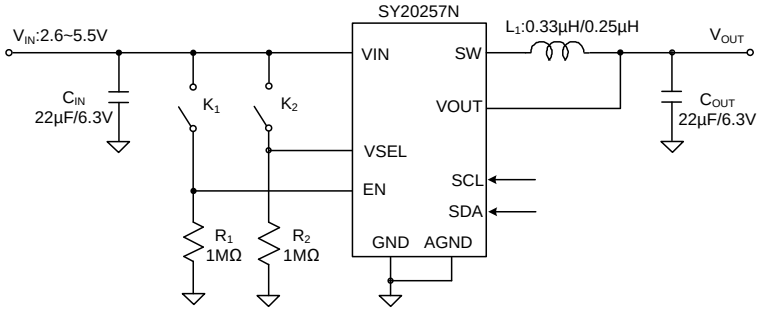


Figure 1. Schematic Diagram

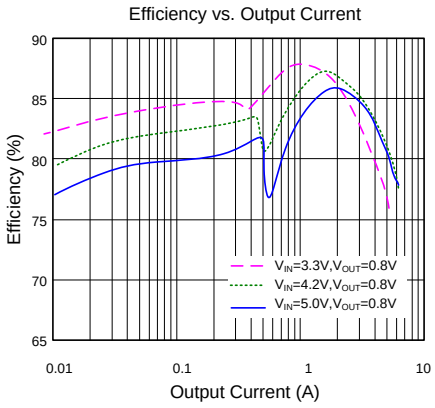
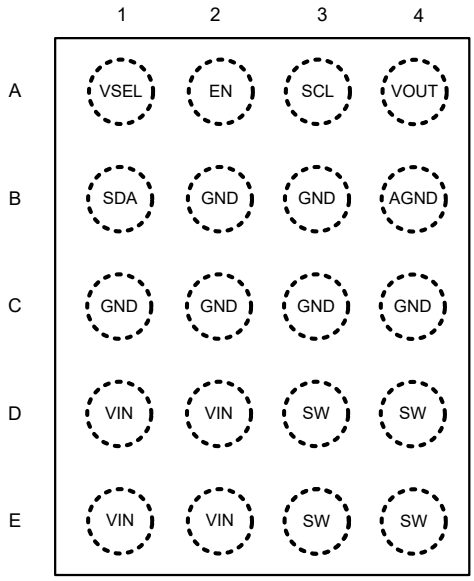


Figure2. Efficiency

Pinout (top view)



Part Number	Package type	Top Mark①
SY20257NPKC	CSP1.56*1.96-20	Yp***xyz***

Note①： ***x=year code, y=week code, z= lot number code.***

Pin	Pin Name	Pin Description
D1,D2,E1,E2	VIN	Power input pin. These pins must be decoupled to ground with at least a 22μF ceramic capacitor. The input capacitor should be placed as close as possible between VIN and GND pins.
D3,D4,E3,E4	SW	Switching node pin. Connect these pins to the switching node of the inductor.
B2,B3,C1,C2,C3,C4	GND	Power ground pins.
A1	VSEL	Voltage select pin. When this pin is low, V_{OUT} will be set by the VSEL0 register. When this pin is high, V_{OUT} will be set by the VSEL1 register.
A2	EN	Enable control pin. Active high. Do not leave it floating. If EN pin is low, the DC/DC converter will be turned off, and all I^2C registers will be reset to default values.
B1	SDA	I^2C interface Bi-directional Data line.
B4	AGND	Analog ground pin.
A3	SCL	I^2C interface clock line.
A4	VOUT	Sense pin for output. Connect it to the output capacitor side.

Block Diagram

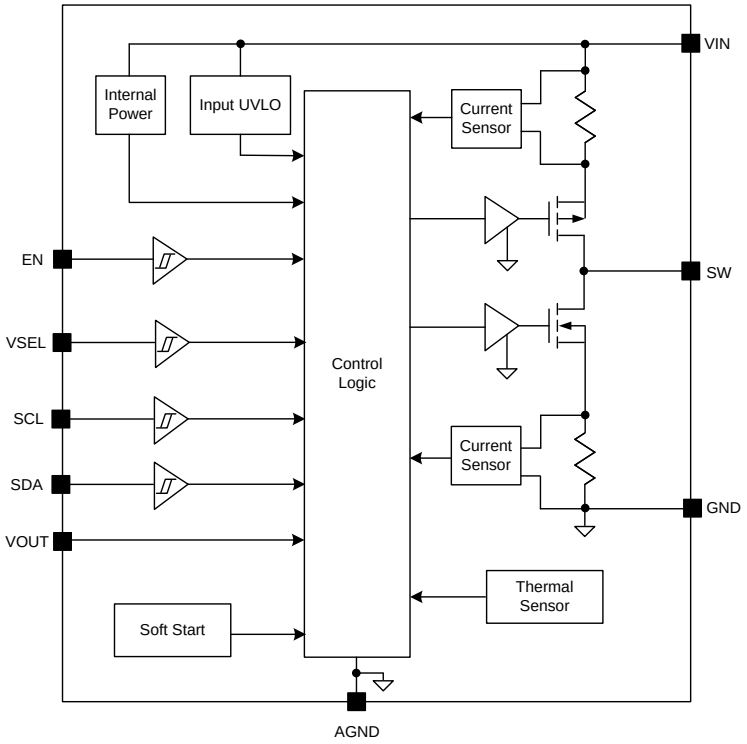


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

VIN ---------- 6.0V
All Other Pins ---------- V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25°C CSP1.56*1.96-20 ---------- 2.6W
Package Thermal Resistance (Note 2)
θ_{JA} ----------38°C/W
θ_{JC} ---------- 8°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.6V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 0.8V, L = 0.33µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.6		5.5	V
Input UVLO Threshold	V_{UVLO}			2.45	2.58	V
Input UVLO Hysteresis	V_{HYS}			0.15		V
Quiescent Current	I_Q	$V_{FB}=V_{REF}\times105\%$		65		µA
Shutdown Current	$I_{SHDN,H/W}$	V_{EN}=0V		0.1	1	µA
	$I_{SHDN,S/W}$	$V_{EN}=V_{IN}$, Buck_Enx=0		41		µA
Output Voltage Set-point	V_{SET}	Forced PWM, V_{OUT}=VSEL0,default value	-1.5		+1.5	%
SW Node Discharge Resistance	R_{DIS}			150		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			28		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			17		mΩ
EN,VSEL,SDA,SCL						
Input Voltage High	V_{IH}		1.1			V
Input Voltage Low	V_{IL}				0.4	V
Min ON Time	$t_{ON,MIN}$			40		ns
Soft-start Time	t_{SS}			0.3		ms
Switching Frequency	F_{SW}	CCM		2.4		MHz
Top FET Current Limit	$I_{LMT,TOP}$		7.5			A
Bottom FET Current Limit	$I_{LMT,BOT}$		6			A
Input Over Voltage Threshold	V_{OVP}	Rising Threshold		6.15		V
		Falling Threshold	5.5	5.85		V
Input OVP Delay	$t_{OVP,DLY}$			20		µs
Thermal Shutdown Temperature	T_{SD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYS}			15		˚C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY20257NPKC is measured in the natural convection at T_A = 25°C on a 2OZ two-layer Silergy evaluation board. Paddle of CSP1.56*1.96-20 package is the case position for SY20257NPKC θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Enabling Function

The EN pin controls SY20257N start up. EN pin low to high transition starts the power up sequencer. If EN pin is low, the DC/DC converter will be turned off, and all registers will be reset to default values.
SY20257N allows software to enable/disable the regulator when EN is HIGH, via the BUCK_EN bits. BUCK_EN0 and BUCK_EN1 are both initialized HIGH in the registers.

Hardware and Software Enable Control Table

Pins		Bits		
EN	VSEL	BUCK_EN0	BUCK_EN1	OUTPUT
0	x	x	x	OFF
1	0	0	x	OFF
1	0	1	x	ON
1	1	x	0	OFF
1	1	x	1	ON

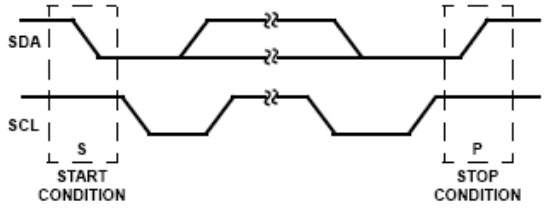
Input Over Voltage Protection Function

When the V_{IN} exceeds over voltage protection threshold, SY20257N will stop switching to protect the circuitry. An internal 20us blanking time filter helps to prevent the circuit from shutting down due to noise spikes.

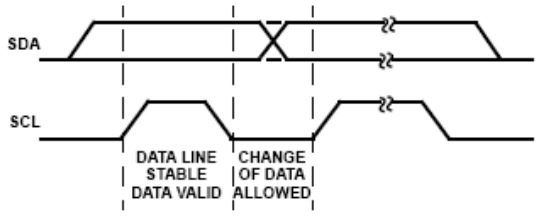
I²C Interface

SY20257N features an I²C interface that allow the HOST processor to control the output voltage achieve the DVS function. The I²C interface supports clock speeds of up to 3.4MHz and uses standard I²C commands. SY20257N always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation. I²C address of the SY20257N is set at the factory to 0xC0h.

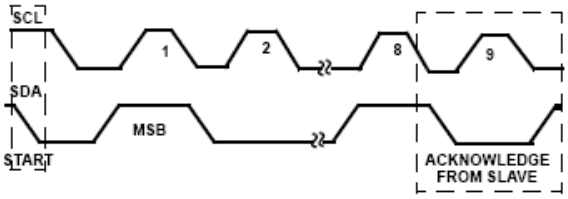
START and STOP Conditions:
SY20257N is controlled via an I²C compatible interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.



Data Validity:
The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

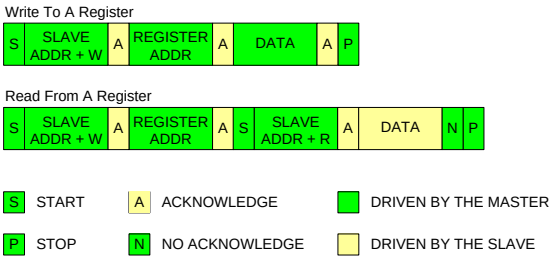


Acknowledge:
Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.



Data Transactions:
All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address (1100000x for the SY20257N, this address can be changed if necessary) followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA

line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and SY20257N acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the SY20257N which register the master will write or read. Once the SY20257N receives a register address byte it responds with an acknowledge.



Register Settings:

1. VSEL0 (0x00)

Register Name				VSEL0
Address				0x00
Field	**Bit**	**R/W**	**Default**	**Description**
BUCK_EN0	7	R/W	1	Software buck enable. When EN pin is low, the regulator is off. When EN pin is high, BUCK_EN bit takes precedent.
MODE0	6	R/W	0	0=Allow auto-PFM mode during light load. 1=Forced PWM mode
NSEL0	5:0	R/W	010000 (V_{OUT}=0.8V)	000000 = 0.60V 000001 = 0.6125V …… 010000 = 0.8 V …… 111111=1.3875V

2. VSEL1 (0x01)

Register Name				VSEL1
Address				0x01
Field	**Bit**	**R/W**	**Default**	**Description**
BUCK_EN1	7	R/W	1	Software buck enable. When EN pin is low, the regulator is off. When EN pin is high, BUCK_EN bit takes precedent.
MODE1	6	R/W	0	0=Allow auto-PFM mode during light load. 1=Forced PWM mode
NSEL1	5:0	R/W	010000 (V_{OUT}=0.8V)	000000 = 0.60V 000001 = 0.6125V …… 010000 = 0.8V …… 111111=1.3875V

3. Control Register (0x02)

Register Name				Control Register
Address				0x02
Field	**Bit**	**R/W**	**Default**	**Description**
Output Discharge	7	R/W	1	0 = discharge resistor is disabled. 1 = discharge resistor is enabled.
Slew Rate	6:4	R/W	011=12.5mV/1.2us	Set the slew rate for positive voltage transitions. 000 = 12.5mV/0.15us 001 = 12.5mV/0.3us 010 = 12.5mV/0.6us 011 = 12.5mV/1.2us 100 = 12.5mV/2.4us 101 = 12.5mV/4.8us 110 = 12.5mV/9.6us 111 = 12.5mV/19.2us
Reserved	3:0	R/W	0000	Always reads back 0.

4. ID1 Register (0x03)

Register Name				ID1 Register
Address				0x03
Field	**Bit**	**R/W**	**Default**	**Description**
VENDOR	7:5	R	100	IC vendor code.
Reserved	4	R	0	Always reads back 0.
DIE_ID	3:0	R	0001	

5. ID2 Register (0x04)

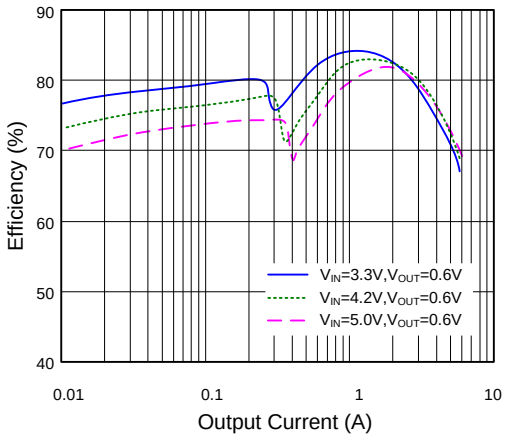
Register Name				ID2 Register
Address				0x04
Field	**Bit**	**R/W**	**Default**	**Description**
Reserved	7:4	R	0000	Always reads back 0.
DIE_REV	3:0	R	1100	

6. PGOOD Register (0x05)

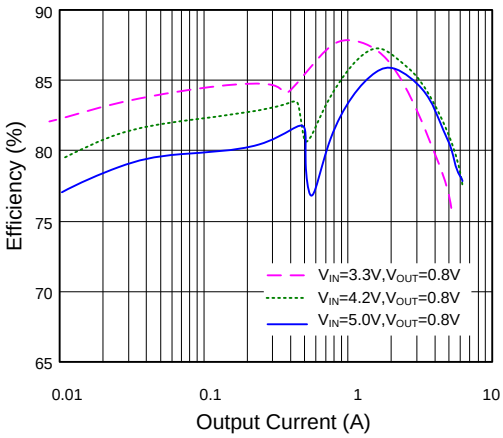
Register Name				PGOOD Register
Address				0x05
Field	**Bit**	**R/W**	**Default**	**Description**
PGOOD	7	R	0	1: Buck is enabled and soft-start is completed.
Reserved	6:0	R	000 0000	Always reads back 0.

Typical Performance Characteristics

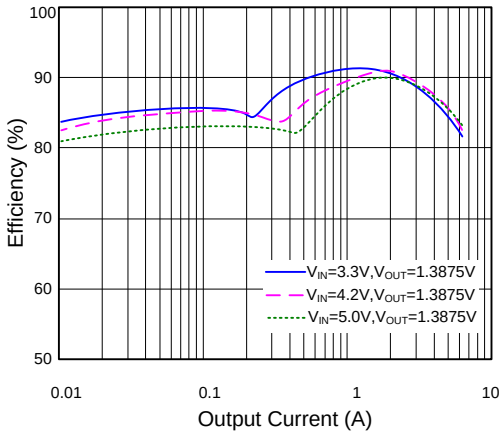
Efficiency vs. Output Current



Efficiency vs. Output Current

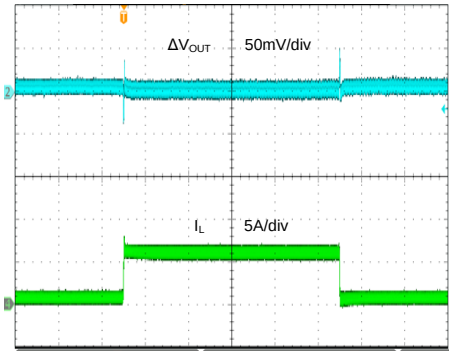


Efficiency vs. Output Current



Load Transient

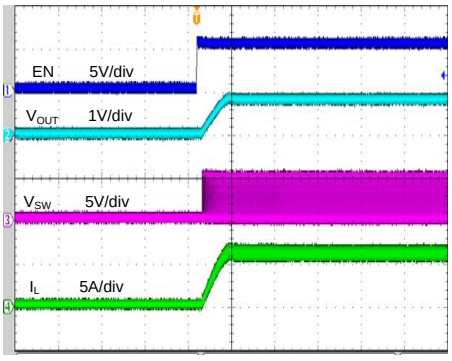
(V_{IN}=5.0V, V_{OUT}=0.8V, I_{OUT}=0.6 ~ 6.0A)



Time (400μs/div)

Startup from Enable

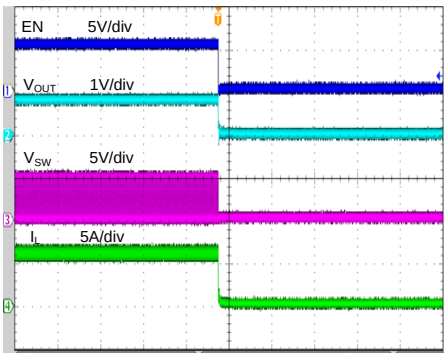
(V_{IN}=5.0V, V_{OUT}=0.8V, I_{OUT}=6.0A)



Time (400μs/div)

Shutdown from Enable

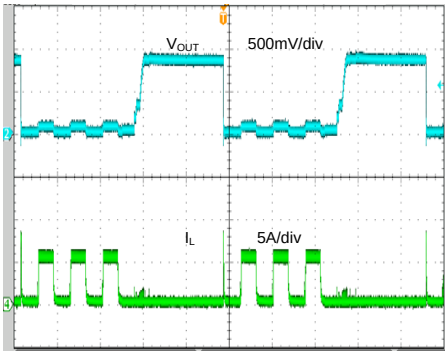
(V_{IN}=5.0V, V_{OUT}=0.8V, I_{OUT}=6.0A)



Time (400μs/div)

Short Circuit Protection

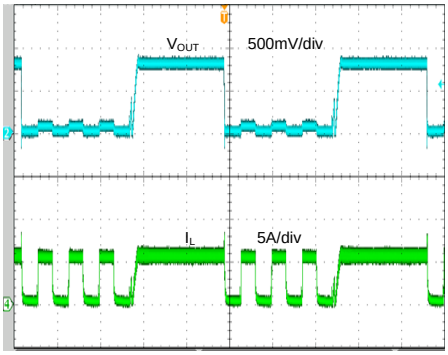
(V_{IN}=5.0V, V_{OUT}=0.8V, I_{OUT}=0A ~ short)



Time (2ms/div)

Short Circuit Protection

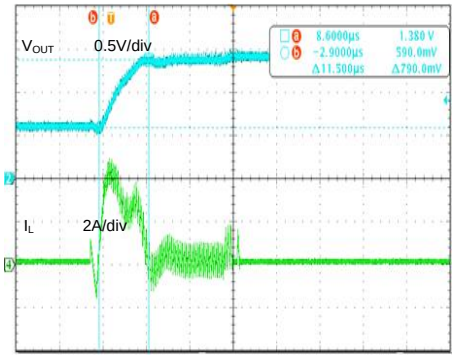
(V_{IN}=5.0V, V_{OUT}=0.8V, I_{OUT}=6A ~ short)



Time (2ms/div)

Dynamic Voltage Switch

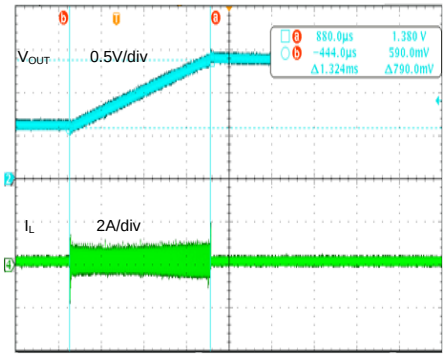
(V_{IN}=5.0V,0A Load,V_{OUT}=0.6~1.3875V,Slew Rate=10mV/0.15μs)



Time (10μs/div)

Dynamic Voltage Switch

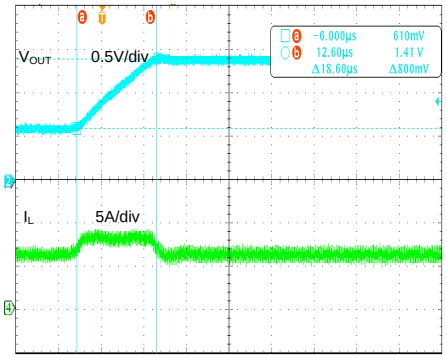
(V_{IN}=5.0V,0A Load,V_{OUT}=0.6~1.3875V,Slew Rate=10mV/19.2μs)



Time (400μs/div)

Dynamic Voltage Switch

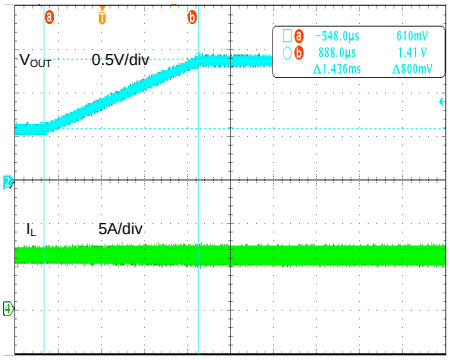
(V_{IN}=5.0V,6A Load,V_{OUT}=0.6~1.3875V,Slew Rate=10mV/0.15μs)



Time (10μs/div)

Dynamic Voltage Switch

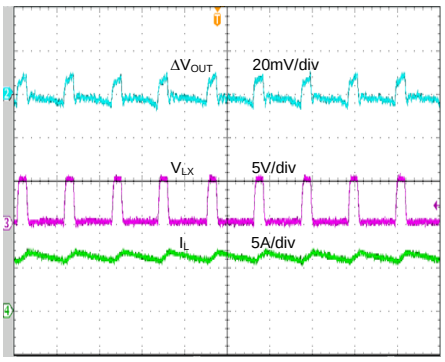
(V_{IN}=5.0V,6A Load,V_{OUT}=0.6~1.3875V,Slew Rate=10mV/19.2μs)



Time (400μs/div)

Output Ripple

(V_{IN}=5.0V, V_{OUT}=0.8V, I_{OUT}=6.0A)



Time (400ns/div)

Operation

SY20257N is a high efficiency 2.4MHz synchronous step down DC/DC regulator capable of delivering up to 6A output currents. It can operate over a wide input voltage range from 2.6V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss. The output voltage can be programmed from 0.6V to 1.3875V through I^2C interface.

Applications Information

Because of the high integration in SY20257N, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L need to be selected for the targeted applications.

Input Capacitor C_{IN}

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1\text{-}D)}\ (A)$$

This formula has a maximum at $V_{IN}=2\times V_{OUT}$ condition, where $I_{CIN\_RMS}=I_{OUT}/2$.

With the maximum load current at 6A, a typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 22uF capacitance can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the VIN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and VIN/GND pins.

Output Capacitor C_{OUT}

Both steady state ripple and transient requirements must be taken into account when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and more than one 22µF capacitor.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN\_MAX})}{F_{SW} \times I_{OUT\_MAX} \times 40\%}\ (H)$$

Where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

SY20257N is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{OUT,\,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<15mΩ to achieve a good overall efficiency.

Layout Design:

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, L, C_{OUT}.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) The decoupling capacitor of VIN and GND must be placed close enough to the pins. The loop area formed by the capacitors and GND must be minimized.

3) The PCB copper area associated with SW pin must be minimized to improve the noise immunity.

4) The feedback trace connecting C_{OUT} to the VOUT pin must NOT be adjacent to the SW node on the PCB layout to minimize the noise coupling to VOUT pin.

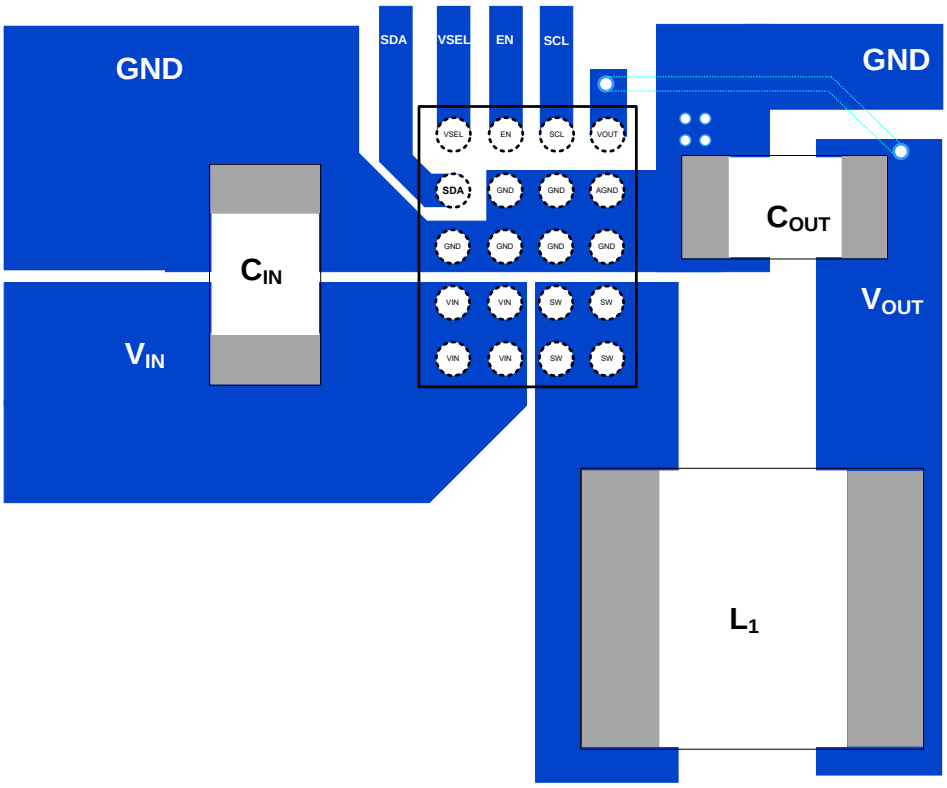
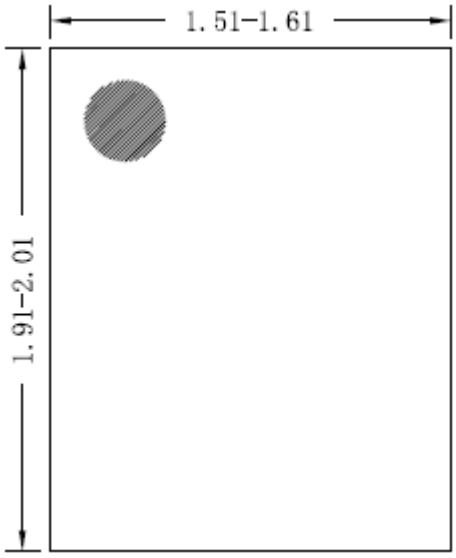
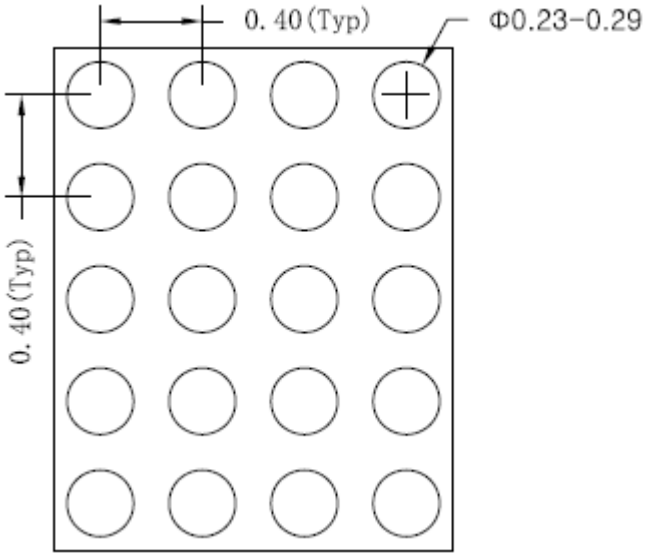


Figure4. PCB Layout Suggestion

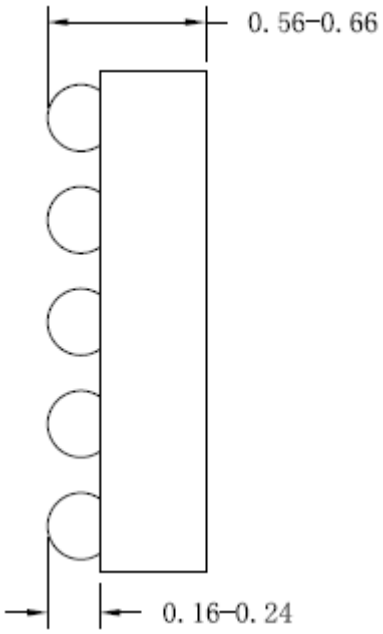
CSP1.56×1.96-20 Outline Drawing



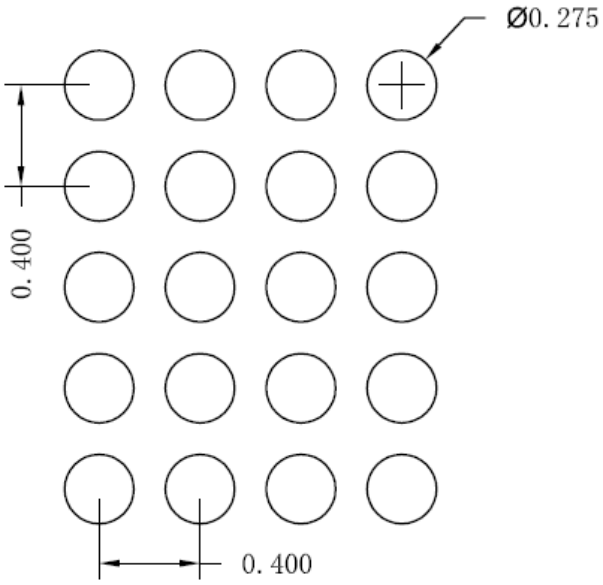
Top View



Bottom View



Side View

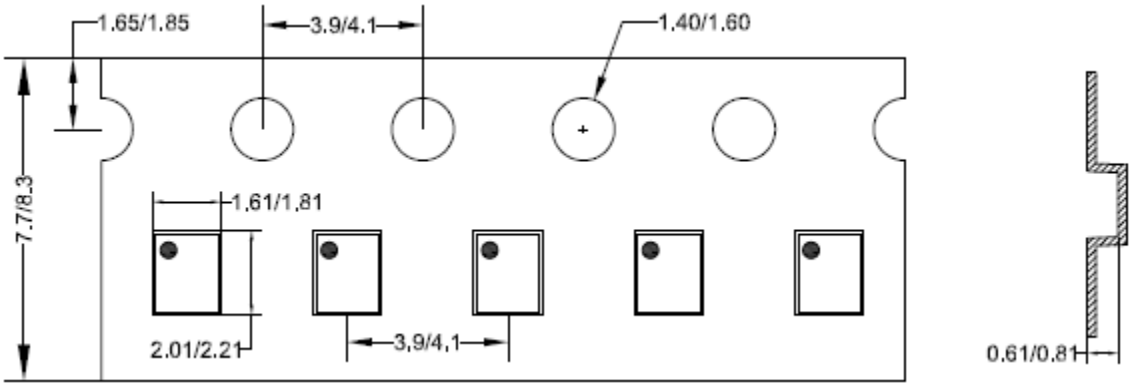


Recommended PCB Layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

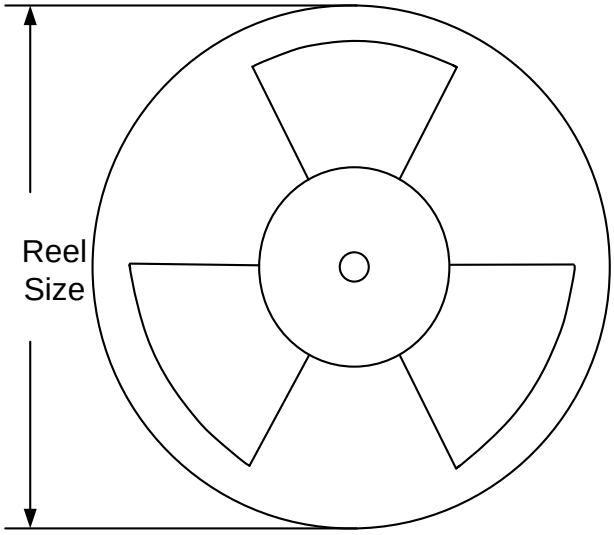
Taping & Reel Specification

1. CSP1.56×1.96



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
CSP1.56×1.96	8	4	7"	400	400	3000

3. Others: NA

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com