

General Description

SY20815 integrates an ultra-low $R_{DS(ON)}$ switch with accurate over-voltage protection. It supports up to 7V input surge voltage. Linear mode will be activated to maintain the output voltage at target clamp voltage when the input voltage exceeds the target clamp voltage. Thermal protection remains active in linear mode. The Power FET will be disabled when the thermal shutdown temperature is reached. When the temperature falls below 135°C, SY20815 restarts.

Ordering Information

SY20815 □(□□)□
 □ Temperature Code
 □ Package Code
 □ Optional Spec Code

Ordering Number	Package Type	Note
SY20815PRC	CSP0.79x0.79-4	

Features

- 7V input surge voltage capability
- Low $R_{DS(ON)}$: 96mΩ
- 1A continuous load current capability
- Precise clamping output voltage: 4.875V(±2.5%)
- Independent ON/OFF control input
- Ultra compact CSP0.79x0.79-4ball 0.3mm thick package
- RoHS Compliant and Halogen Free

Applications

- Smart Phone, Tablet PCs
- MID, E-Book
- Storage, DSLR, and Portable Devices

Typical Applications

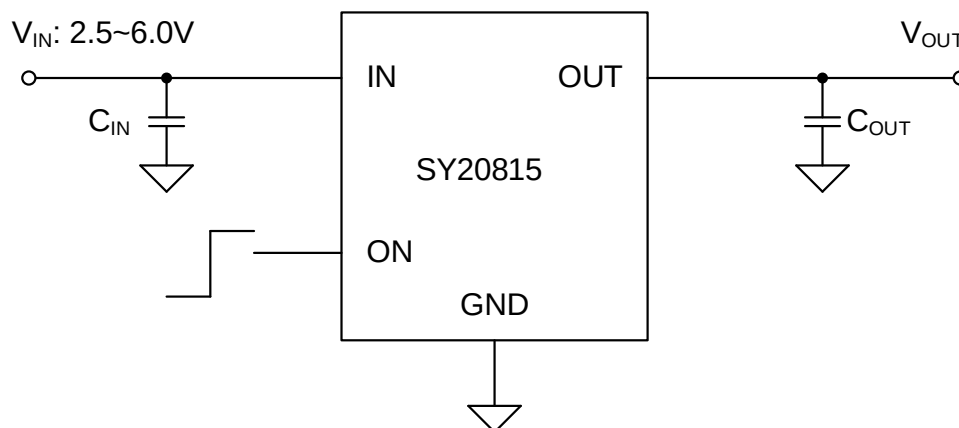
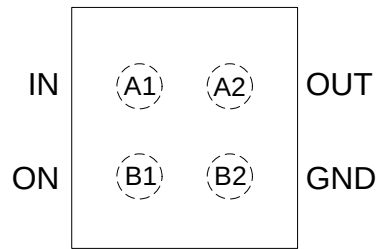


Figure 1. Schematic Diagram

Pinout (top view)



(CSP0.79x0.79-4)

Top Mark: **Jaxyz**, (Device code: Ja; x=*year code*, y=*week code*, z= *lot number code*)

Pin Name	Pin Number	Pin Description
IN	A1	Input pin. Decouple this pin to GND with at least 4.7uF ceramic cap.
OUT	A2	Output pins. Decouple this pin to GND with at least 4.7uF ceramic cap.
GND	B2	Ground pin.
ON	B1	ON/OFF control. Active high. Do not leave it floating.

Absolute Maximum Ratings (Note 1)

All pins----- 7.0V
Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$ -----0.66W
Package Thermal Resistance (Note 2)
 θ_{JA} ----- 188°C/W
 θ_{JC} ----- 2°C/W
Junction Temperature Range ----- 150°C
Lead Temperature (Soldering, 10 sec.) ----- 260°C
Storage Temperature Range ----- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN, OUT ----- 2.5V to 6V
Junction Temperature Range ----- -40°C to 125°C
Ambient Temperature Range ----- -40°C to 85°C



Electrical Characteristics

($V_{IN} = 4.2V$, $T_A = 25^{\circ}C$ unless otherwise specified)

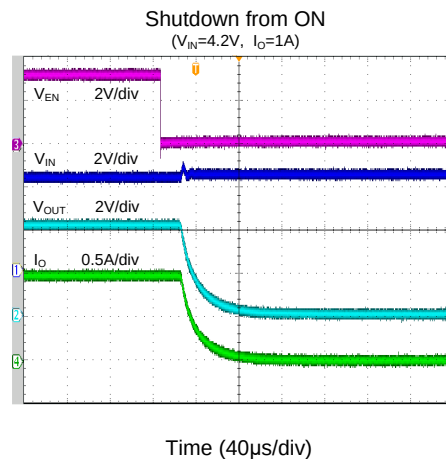
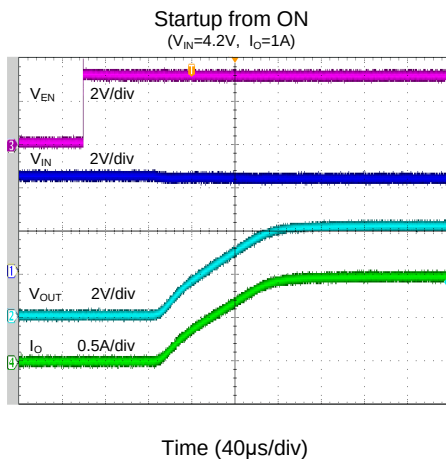
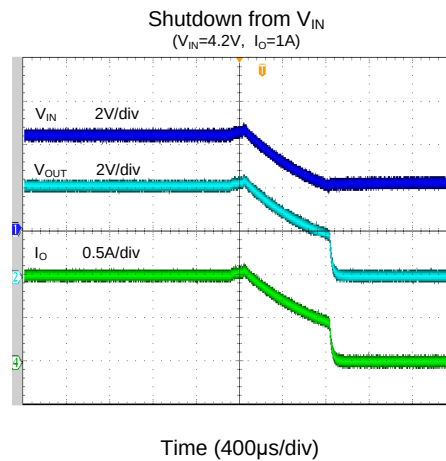
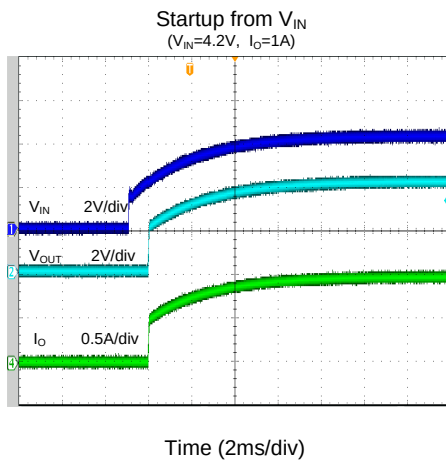
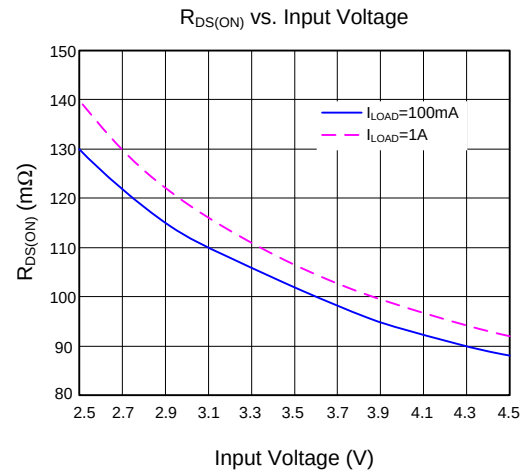
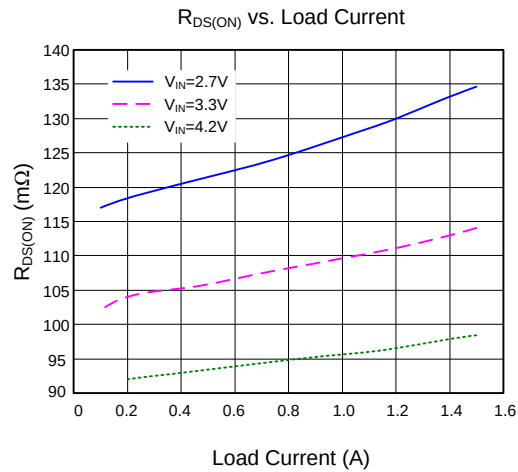
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		6	V
Input UVLO Threshold	V_{UVLO}				2.45	V
UVLO hysteresis	V_{HYS}			0.1		V
Shutdown Current	I_{SHDN}	ON=Low			1	μA
Quiescent Current	I_Q	$I_{OUT}=0$		10		μA
FET R_{ON}	$R_{DS(ON)}$	$V_{IN}=4.2V$		96		$m\Omega$
		$V_{IN}=3.3V$		112		$m\Omega$
		$V_{IN}=2.7V$		140		$m\Omega$
Clamping Output Voltage	V_{CLP}		4.750	4.875	5.000	V
ON Input Logic High	V_{IH}		1.0			V
ON Input Logic Low	V_{IL}				0.4	V
Thermal shutdown temperature	T_{SD}			150		$^{\circ}C$
Thermal shutdown hysteresis	T_{HYS}			15		$^{\circ}C$

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

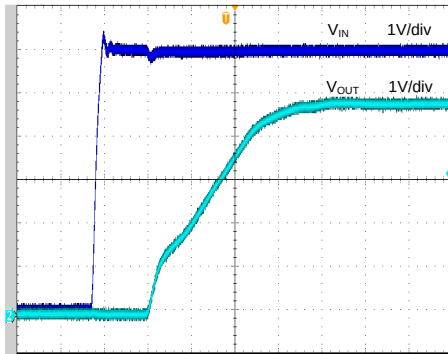
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^{\circ}C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

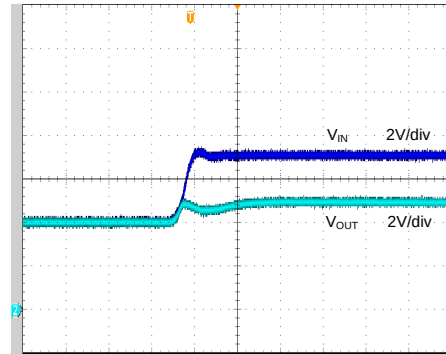


V_{IN} Overshoot Response
($V_{IN}=0V$ to $6V$ at $10\mu s$, $I_O=Null$)



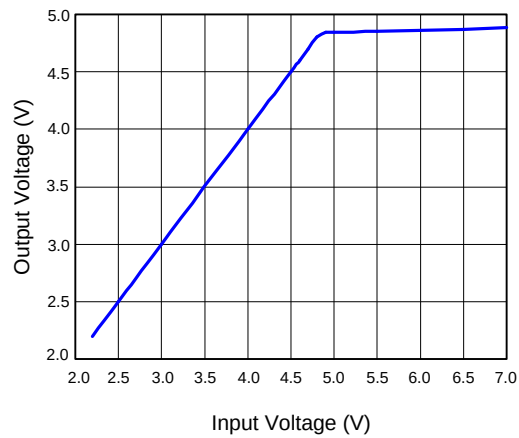
Time ($40\mu s/div$)

V_{IN} Overshoot Response
($V_{IN}=3.7V$ to $7V$ at $4.3\mu s$, $I_O=Null$)



Time ($10\mu s/div$)

Output Voltage Clamp vs. Input Voltage



Applications Information

Input Capacitor

To reduce device inrush current, a 4.7 μ F ceramic capacitor, C_{IN} , is recommended. A higher value of C_{IN} can be used to reduce the voltage drop experienced as the switch is turned on into large capacitive load.

Output Capacitor

A 4.7 μ F ceramic output cap is recommended to prevent parasitic board inductance from forcing V_{OUT} below GND when switching off.

Output Discharge

SY20815 integrates a 10 Ω pull down resistor for quick output discharge. The resistor is activated when the switch is turned off.

PCB Layout Guide

For best performance of the SY20815, the following guidelines must be strictly followed:

1. Keep all power trace as short and wide as possible. And it is desirable to use 2-layer or 4-layer board for thermal performance and better capability of current flow. These power pins include VIN and OUT.
2. Place input capacitor and output capacitor close to the IC for better transient performance.

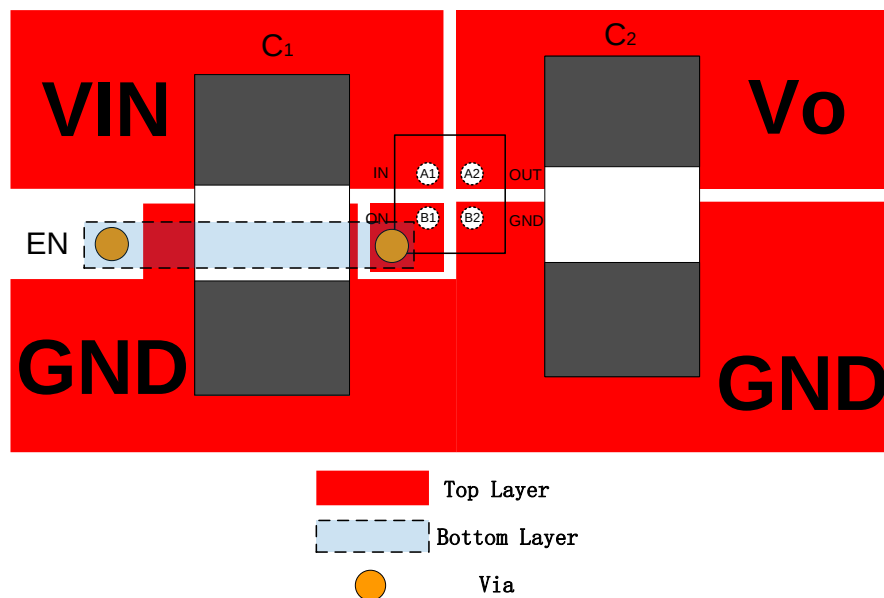
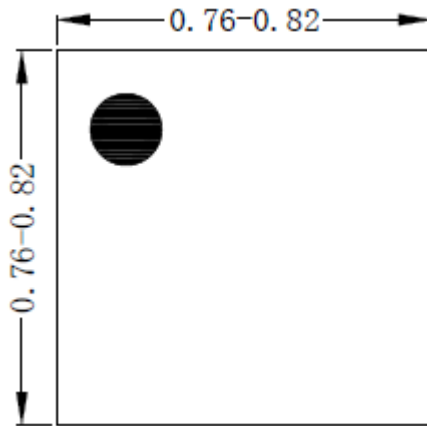
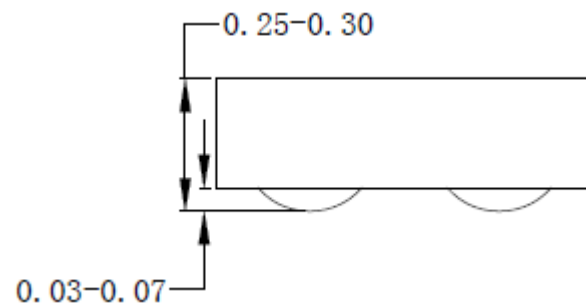


Figure 2. PCB Layout Suggestion

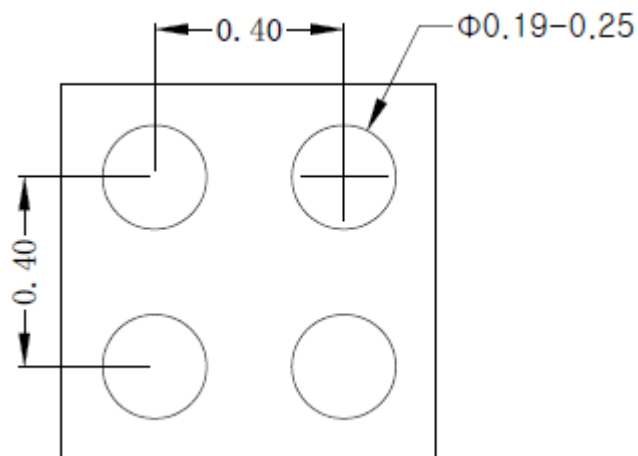
CSP0.79x0.79-4 Package Outline Drawing



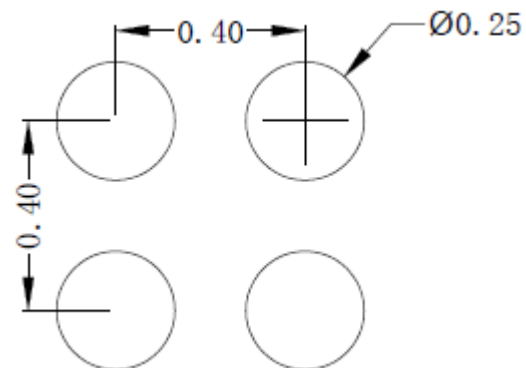
Top view



Side view



Bottom view

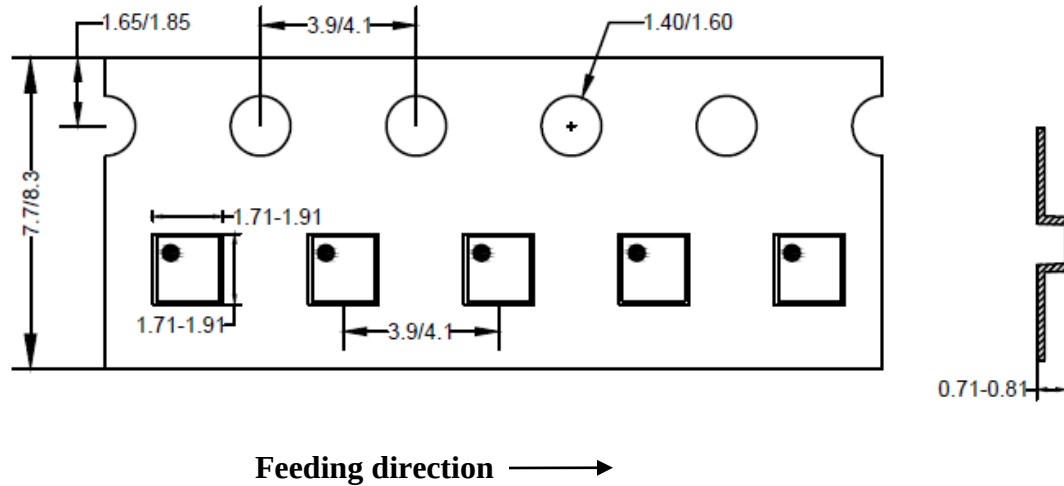


**Recommended PCB layout
(Reference only)**

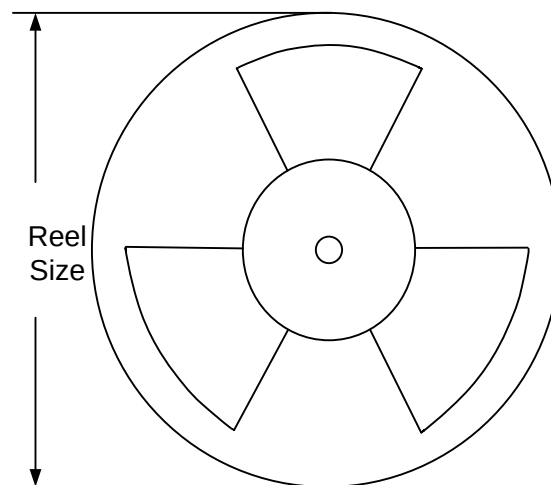
Notes: All dimension in millimeter and exclude mold flash & metal burr

Taping & Reel Specification

1. CSP0.79x0.79 taping orientation



2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP0.79x0.79	8	4	7"	400	160	10000

3. Others: NA



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