SY20804/SY20804A

1.2A Load Switch with D Flip Flop Control

General Description

The SY20804/SY20804A is a compact, low $R_{DS(ON)}$ load switch designed to deliver a continuous current of up to 1.2A. It functions across an input voltage range of 4.5V to 18V.

The SY20804/SY20804A includes a DFF (D Flip Flop) input, allowing the user to control the load switch on and off states. When the DFF pin is pulled low for a duration exceeding the programmable blanking time, t_{BLK} (set by C_T), the device will switch its output state. If the duration of the low level on the DFF pin is less than t_{BLK}, the device will maintain its previous output state.

The SY20804/A is available in a compact SO8 package.

Features

- Wide Input Voltage Range: 4.5 to 18V
- Up to 1.2A Continuous Load Current Capability
- Low $R_{DS(ON)}$: 110mΩ at V_{IN}=12V
- Programmable Blanking Time for DFF Control
- Start-Up Sequence:
  - SY20804: Default ON when EN high
  - SY20804A: Default OFF when EN high
- Low Shutdown Current
- Controlled Turn-On Slew Rate to Avoid Inrush Currents
- Over Temperature Shutdown with Auto Recovery
- RoHS Compliant and Halogen Free
- Compact Package: SO8

Applications

- Industrial Control
- Set-top Boxes

Typical Application

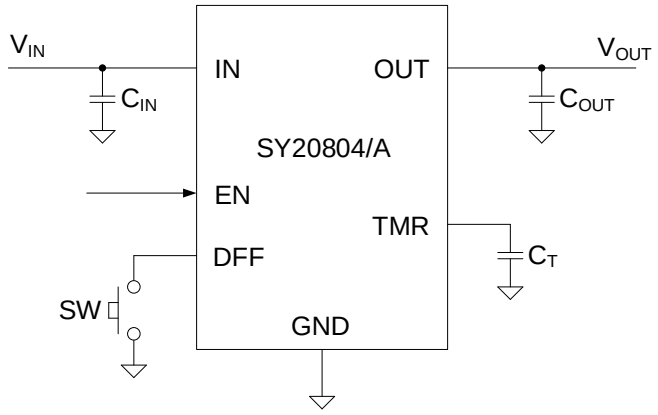


Figure 1. Schematic Diagram

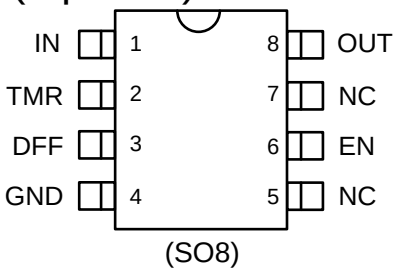
Ordering Information

SY20804 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Part Number	Package type	Top Mark①
SY20804FAC	SO8	**AUG*xyz***
SY20804AFAC	SO8	**AYW*xyz***

x=year code, y=week code, z= lot number code.

Pinout (top view)



(SO8)

Pin Name	Pin Number	Pin Description
IN	1	Input voltage. Connect a 1μF ceramic capacitor from IN to GND as close to the device as possible.
TMR	2	DFF input signal blanking time control. Connect a capacitor from this pin to GND to set the blanking time. $t_{BLK}(ms)=C_T(nF)\times1.0(V)/1(\mu A)$
DFF	3	Internal edge-trigged D flip-flop clock input. A 500kΩ pull-high resister is connected to this pin.
GND	4	GND pin.
EN	6	Enable control pin. Pull high to turn on.
OUT	8	Output pin. Decouple this pin to the ground with at least a 4.7μF ceramic capacitor.
NC	5, 7	No connection.

Block Diagram

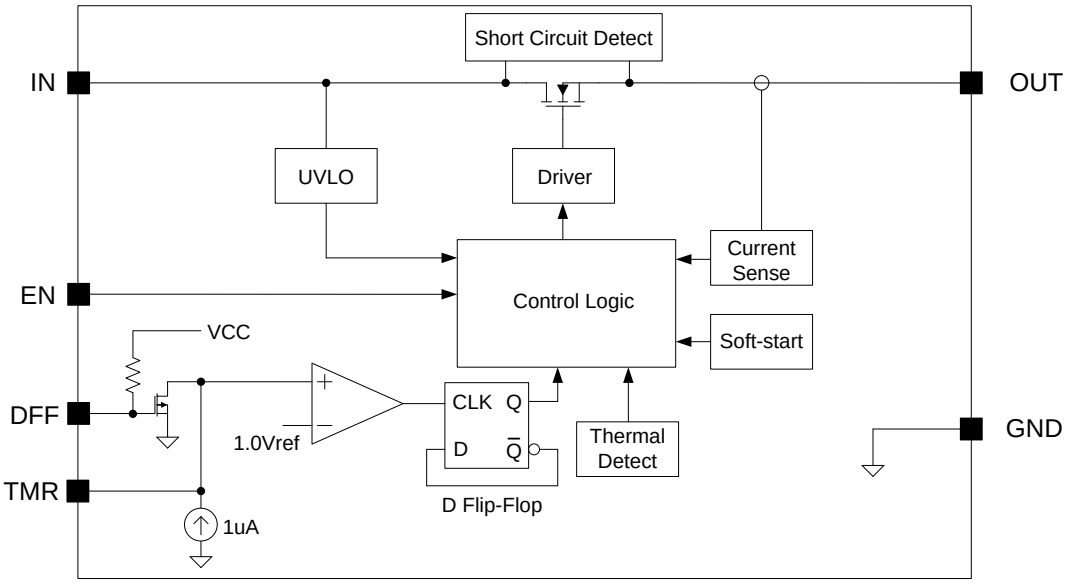


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
All Pins		20	V
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	88	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	45	
P_D Power Dissipation T_A = 25°C	1.1	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	4.5	18	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} =12V, C_{OUT}=1μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		18	V
Shutdown Input Current	I_{SHDN}	Output grounded, Switch off			2	μA
Quiescent Supply Current	I_Q	Open load, switch on		60	80	μA
FET RON	$R_{DS(ON)}$	V_{IN}=12V		110		mΩ
Current Limit	I_{LIM}			2		A
EN Rising Threshold	$I_{EN(H)}$		1.5			V
EN Falling Threshold	$I_{EN(L)}$				0.4	V
IN UVLO Threshold	$V_{IN,UVLO}$				4.5	V
IN UVLO Hysteresis	$V_{IN,HYS}$			0.2		V
Soft-start Time	t_{SS}			2		ms
DFF Low Level Blanking Time	t_{BLK}	C_T=100nF		100		ms
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

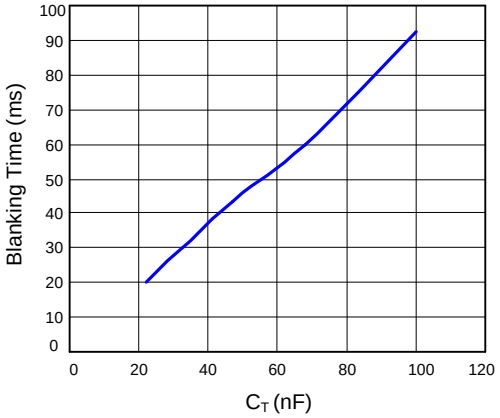
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured with natural convection at T_A = 25°C on a low effective single-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

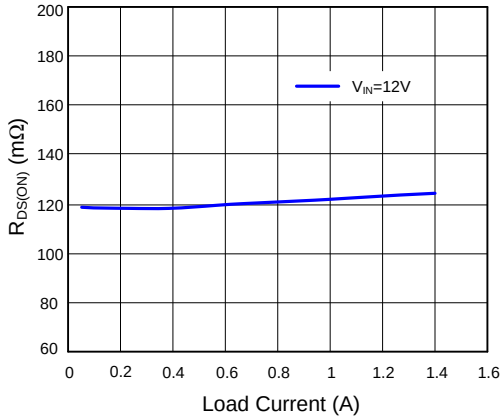
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

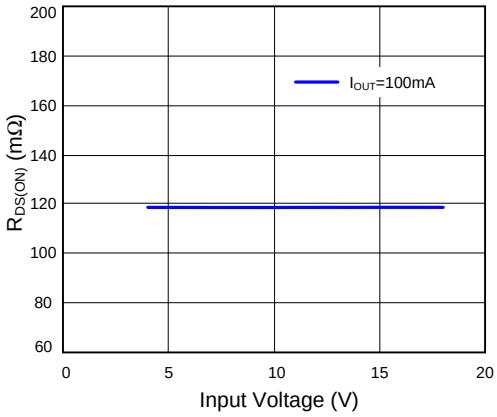
Blanking Time



$R_{DS(ON)}$ vs. Load Current

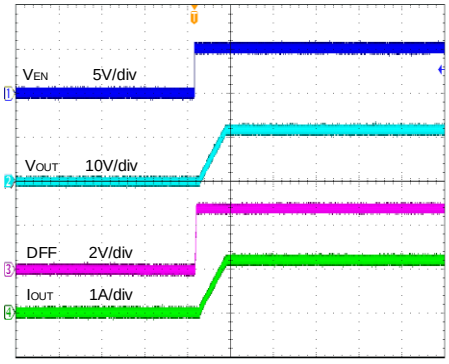


$R_{DS(ON)}$ vs. Input Voltage



Startup from Enable (SY20804)

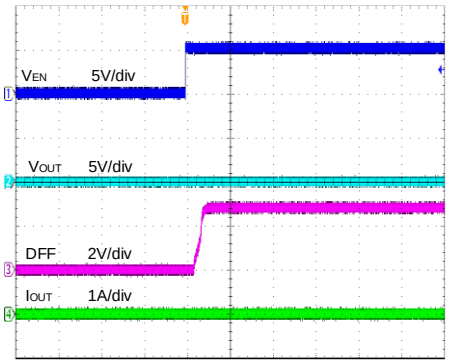
(V_{IN}=12V, I_{OUT}=1.2A)



Time (4ms/div)

Startup from Enable (SY20804A)

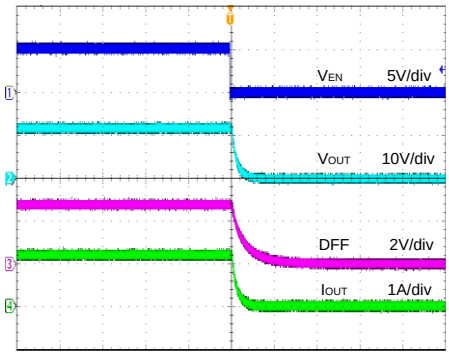
(V_{IN}=12V, I_{OUT}=1.2A)



Time (400μs/div)

Shutdown from Enable

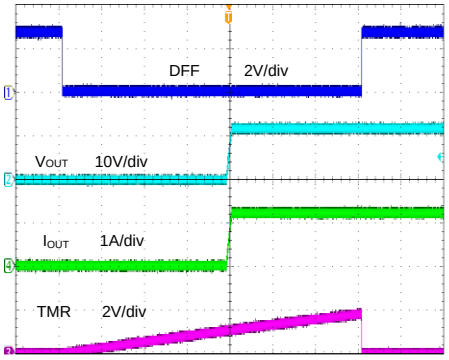
(V_{IN}=12V, I_{OUT}=1.2A)



Time (400μs/div)

Switch ON from DFF

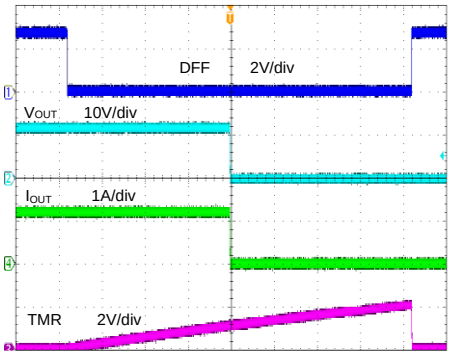
(V_{IN}=12V,C_T=100nF,I_{OUT}=1.2A)



Time (20ms/div)

Switch OFF from DFF

(V_{IN}=12V, C_T=100nF,I_{OUT}=1.2A)



Time (20ms/div)

Control Logic Description

SY20804:

1. When the supply power is on, and EN is set to High, the voltage at the DFF pin will rise to VCC, causing the SY20804 to turn on.
2. If the DFF pin is pulled low and remains there for less than t_{BLK}, the SY20804 will not change; its output stays in the original state.
3. If the DFF pin is held low for a duration exceeding t_{BLK}, the SY20804's output will switch to the opposite state.

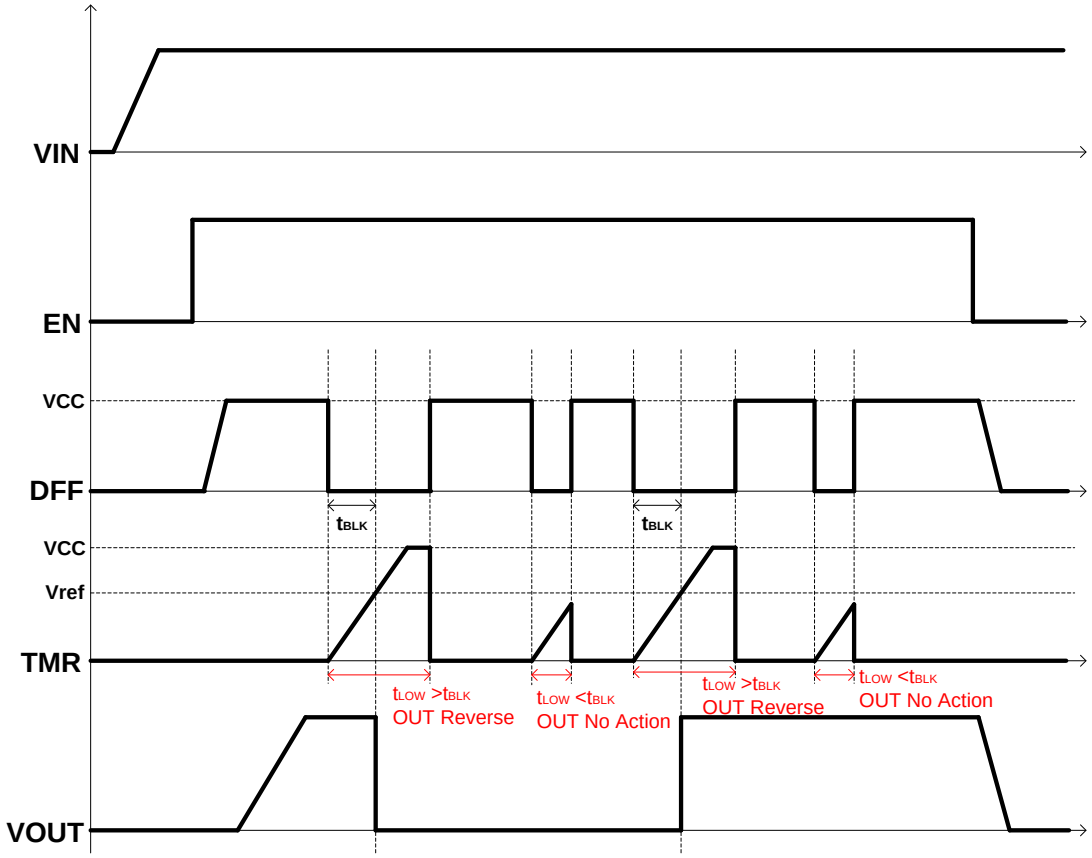


Figure 3. Control Logic of SY20804

SY20804A:

1. When the supply power is on and EN is set to High, the voltage at the DFF pin will rise to VCC, but SY20804A will remain off.
2. If the DFF pin is pulled low and remains there for less than t_{BLK}, the SY20804A will not change; its output stays in the original state.
3. If the DFF pin is held low for a duration exceeding t_{BLK}, the SY20804A's output will switch to the opposite state.

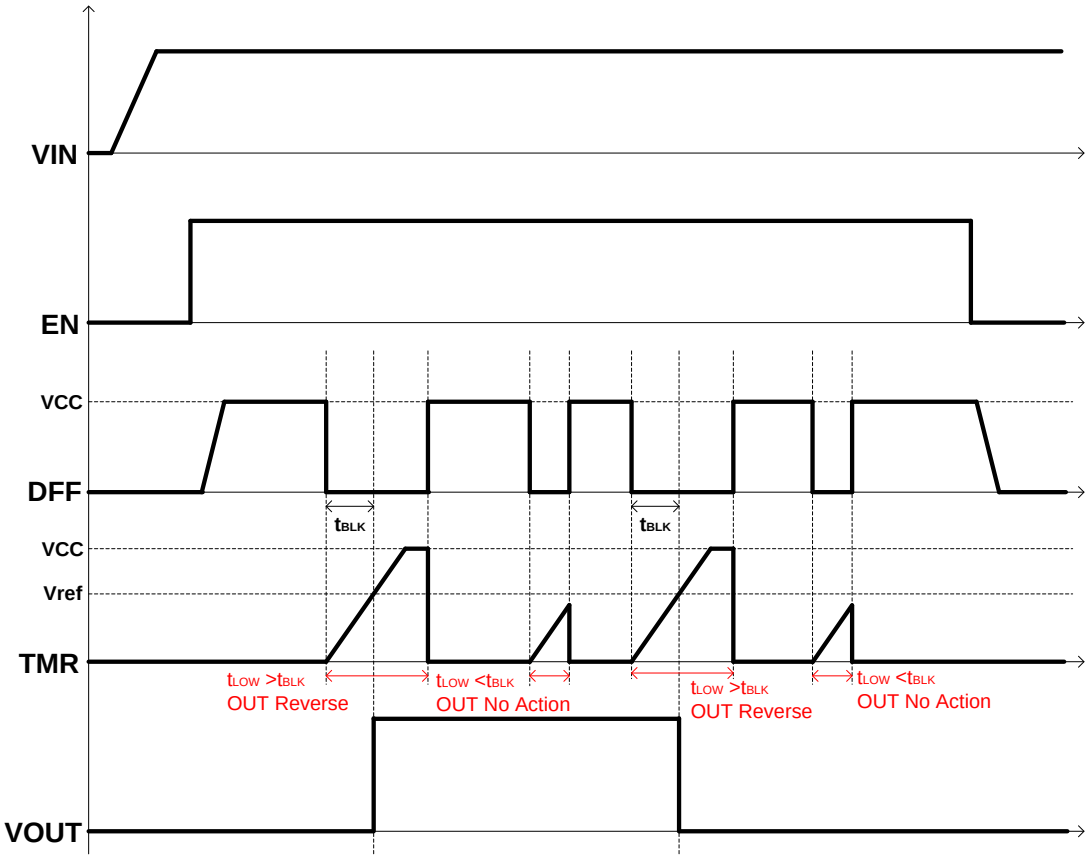


Figure 4. Control Logic of SY20804A

Application Information

Overcurrent and Overtemperature Protection:

Upon detecting an overcurrent condition, the gate of the switch is controlled to maintain a constant output current. In the event of an output short circuit, if the overcurrent condition continues for an extended period, the junction temperature could rise above 150°C, triggering the over-temperature protection to shut down the device. The switch will return to normal operation once the junction temperature falls below 130°C.

Timer Capacitor C_T:

The timer capacitor (C_T) is selected to program the blanking time (t_{BLK}) for the DFF low level. If t_{BLK} is 100ms, C_T can be calculated as 100nF using the following equation:

$$C_T = \frac{t_{BLK} \times 10^{-6} A}{1V}(F)$$

Input Capacitor:

A 4.7μF ceramic capacitor, CIN, is recommended to reduce device inrush current. A higher value of C_{IN} can be used to reduce the voltage drop experienced as the switch is turned on with a large capacitive load. In some applications, using a larger electrolytic capacitor in parallel with the above ceramic capacitor can help with reducing the voltage drop when the switch turns on with large capacitive loads. To minimize noise intererence, place C_{IN} as close as possible to the IN and GND pins.

Output Capacitor:

A 4.7μF ceramic output capacitor is recommended to prevent parasitic board inductance from forcing V_{OUT} below GND when switching off.

PCB Layout Guidelines:

For best performance of the SY20804/A, the following guidelines must be followed:

1. Keep all power traces as short and wide as possible to achieve the best thermal and noise performance.
2. Place a large copper pour under and around the device to lower both resistance and inductance and improve DC and transient performance.
3. The input decoupling ceramic capacitor should be placed as close as possible to the IN and GND pins and connected directly to the pins without vias.
4. The output decoupling ceramic capacitor should be placed as close as possible to the OUT and GND pins and connected directly to these pins without vias.

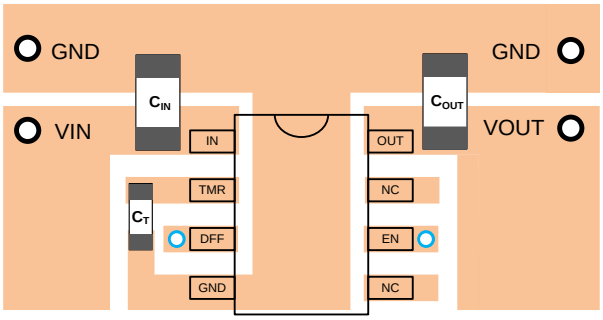


Figure 5. PCB Layout Suggestion

Application Schematic

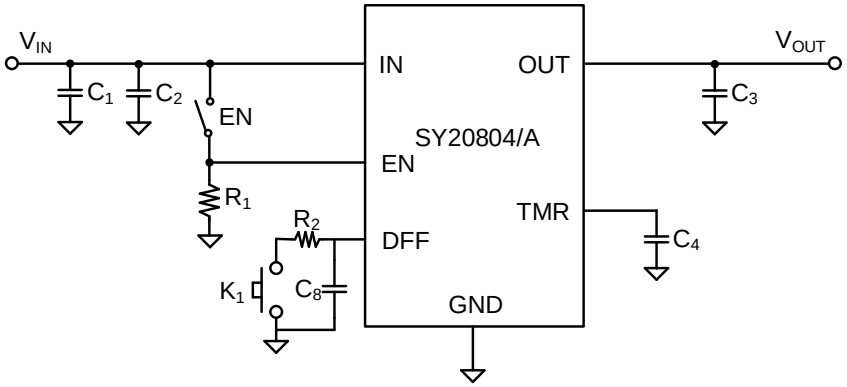
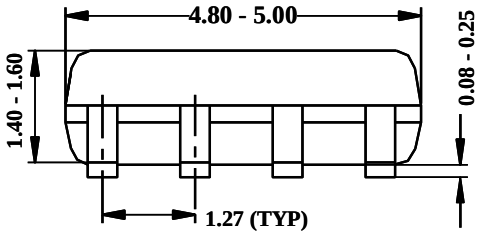


Figure 6. Application Schematic

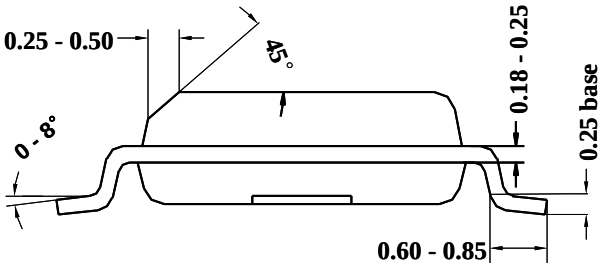
BOM List

Designator	Description	Part Number	Manufacturer
C1	47μF/50V/Electrolytic Capacitor		
C2、C3	4.7μF/25V/1206	C3216X5R1E475M	TDK
C4	100nF/50V/0603	C1608X5R1H104K	TDK
C8	NC		
R1	1MΩ/1%/0603	RC0603FR-071ML	YAGEO
R2	10kΩ/1%/0603	RC0603FR-0710KL	YAGEO

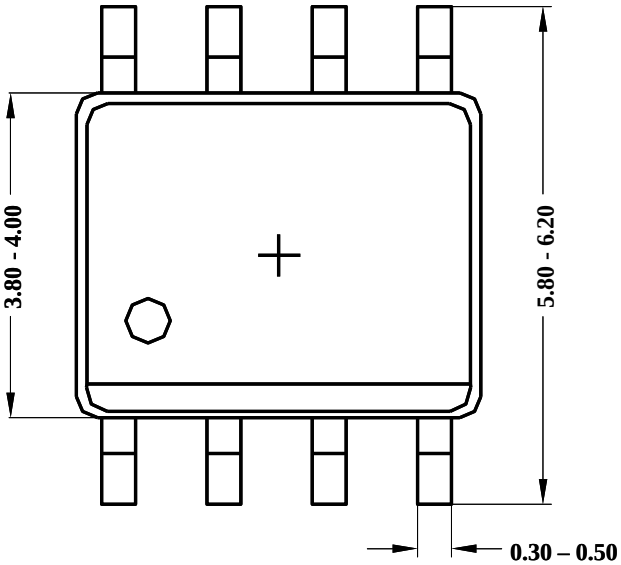
SO8 Package Outline



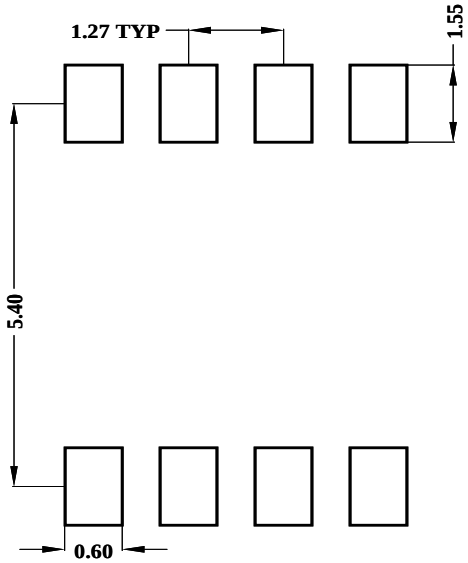
Front View



Side View



Top View

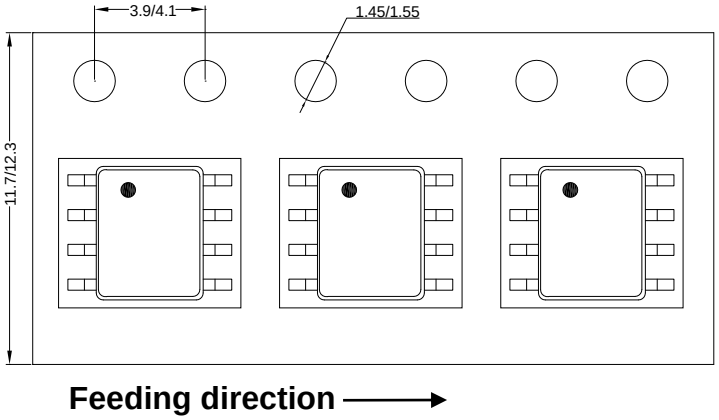


Recommended PCB Layout

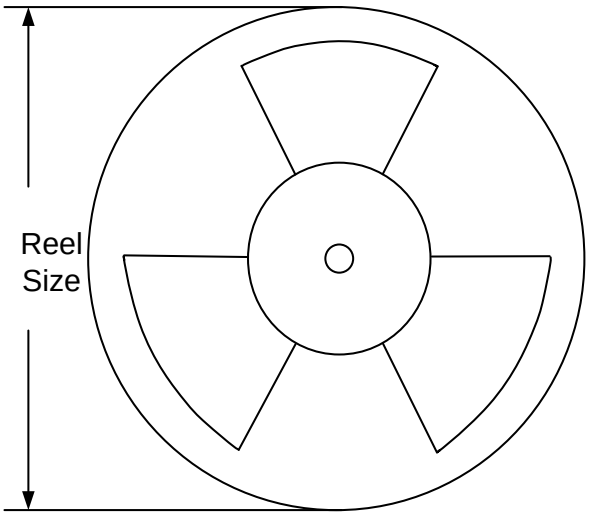
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Specification

Tape dimensions and pin 1 orientation



Reel dimensions



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Reel width (mm)	Trailer length (mm)	Leader length (mm)	Qty per reel
SOP8	12	8	13"	12.4	400	400	2500

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.15, 2024	Revision 1.0	Language improvements for clarity.
Mar.11, 2015	Revision 0.9	Initial Release

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