SY22655

Single Stage Flyback and PFC Controller with CV Control

General Description

SY22655 is a single stage Flyback and PFC controller targeting at Constant Voltage (CV) applications. Primary side control is applied to reduce the feedback circuit cost. It drives the Flyback converter in the Quasi-Resonant mode for high efficiency and achieves high power factor by constant on time control scheme. Adaptive PWM/PFM control is adopted for highest average efficiency.

Ordering Information

SY22655□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY22655ABC	SOT23-6	----

Features

- Primary Side CV Control Eliminates the Opto-coupler
- Valley Turn-on of the Primary MOSFET to Achieve Low Switching Loss
- Internal High Current MOSFET Driver: 0.1A Sourcing and 0.5A Sinking
- Power Factor >0.90 with Single-stage Conversion
- Maximum Switching Frequency Limitation 100 kHz
- RoHS Compliant and Halogen Free
- Compact Package: SOT23-6

Applications

- AC/DC Adapters
- Battery Chargers
- LED Lighting

Typical Applications

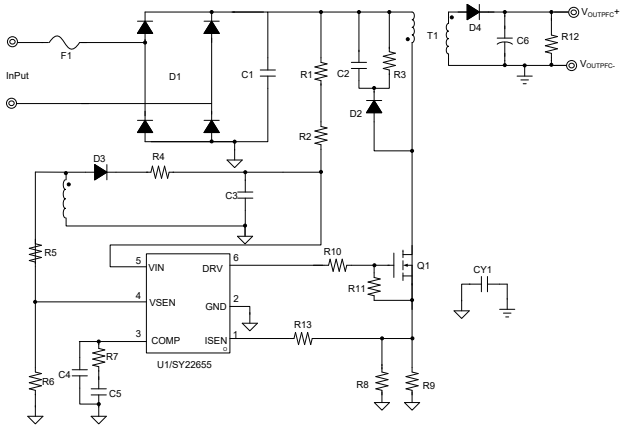


Figure 1. Schematic Diagram

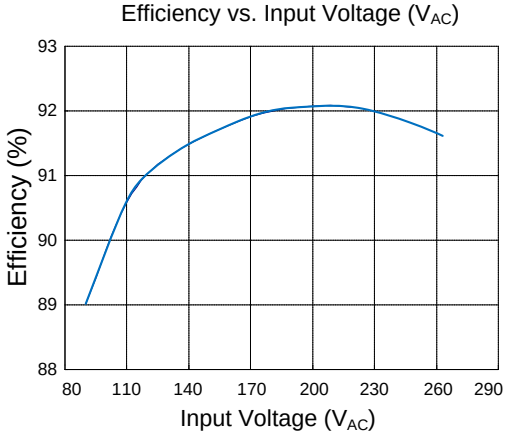
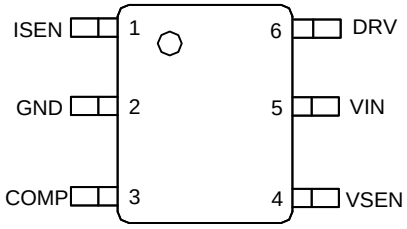


Fig. 2 Efficiency vs Input Voltage

Pinout (top view)



(SOT23-6)

Top Mark: Mt *xyz* (device code: Mt, ***x=year code, y=week code, z= lot number code***)**

Pin	Name	Description
1	ISEN	Current limit PIN.
2	GND	Ground pin.
3	COMP	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
4	VSEN	Output voltage and inductor current zero detection PIN. This pin receives the auxiliary winding voltage by a resistor divider.
5	VIN	Power supply pin.
6	DRV	Gate driver pin. Connect this pin to the gate of primary MOSFET with a resistor.

Absolute Maximum Ratings (Note 1)

VIN, DRV ---------- -0.3V to 36V
Supply current I_{VIN} ----------20mA
VSEN ---------- -0.3V to V_{IN}+0.3V
ISEN, COMP ---------- 3.6V
Power Dissipation, @ T_A = 25°C SOT23-6 ---------- 0.6W
Package Thermal Resistance (Note 2)
SOT23-6,θ_{JA}---------- 170°C/W
SOT23-6,θ_{JC} ---------- 130°C/W
Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN, DRV---------- 9V~22V
Junction Temperature Range ---------- -40°C to 150°C
Ambient Temperature Range ---------- -40°C to 120°C

Block Diagram

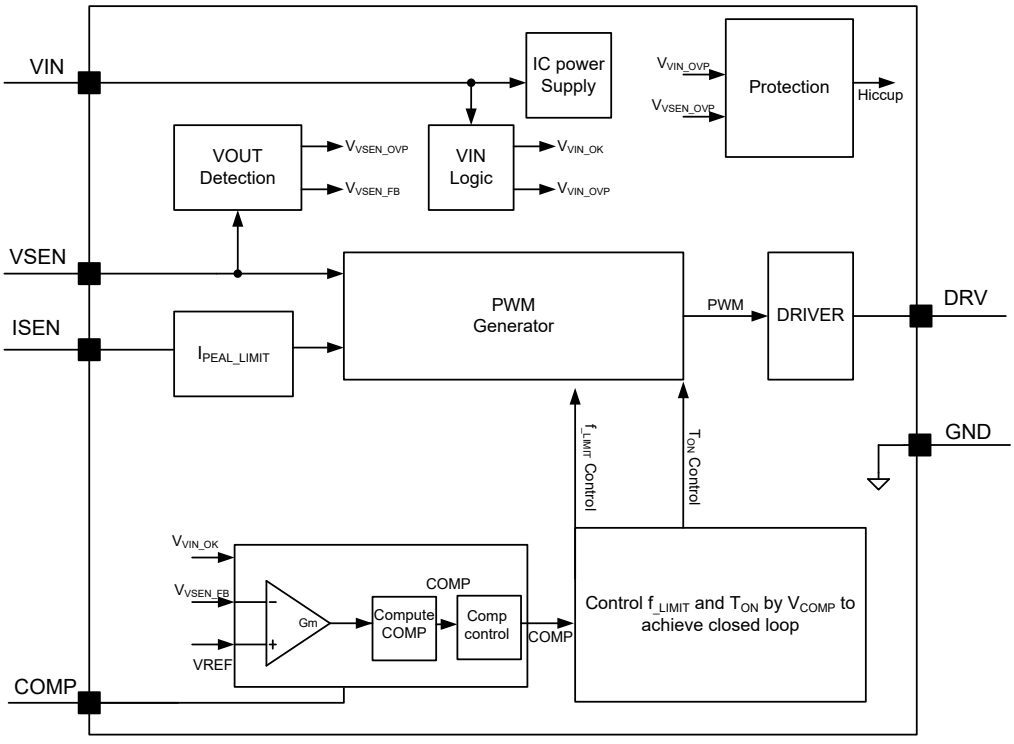


Fig3. Block Diagram

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
Input Voltage Range	V_{VIN}		9		22	V
VIN Turn-on Threshold	V_{VIN_ON}		18.5	21.5	23.5	V
VIN Turn-off Threshold	V_{VIN_OFF}		6.5	7.5	8.5	V
VIN OVP Voltage	V_{VIN_OVP}		22	24.5	27	V
Start up Current	I_{ST}	$V_{VIN}<V_{VIN\_OFF}$		1.5		μA
Operating Current	I_{VIN}		0.25	0.45	0.65	mA
Shunt Current in OVP Mode	I_{VIN_OVP}	$V_{VIN}>V_{VIN\_OVP}$		7.5		mA
Quick Start up Section						
Internal Pre-charge Current Source	I_{PRE_CHARGE}	$V_{FB}< V_{FB\_LOW}$		12		μA
Error Amplifier Section						
Current Limit Voltage	V_{ISEN_LIMIT}	$V_{FB}<0.2V$		0.4		V
		$0.2V<V_{FB}<1V$	0.9	1.0	1.1	V
Maximum Current Voltage	V_{ISEN_EX}		1.2	1.5	1.8	V
V_{FB} at Fast Start up	V_{FB_LOW}		1.04	1.10	1.16	V
Internal Reference Voltage	V_{REFV}		1.225	1.250	1.275	V
Threshold Value of Max V_{FB}	V_{FB_HIGH}		1.33	1.40	1.45	V
OVP Voltage Threshold	V_{VSEN_OVP}			V_{FB_HIGH} +0.1		V
Blanking Time for OFF Time	T_{OFF_MIN1}	V_{ISEN_HOLD}=0.15V		1.7		μs
	T_{OFF_MIN2}	V_{ISEN_HOLD}=0.40V		2.6		μs
Gate Driver Voltage	V_{Gate}			12		V
Typical Source Current	I_{SOURCE}			100		mA
Typical Sink Current	I_{SINK}			500		mA
Max ON Time	T_{ON_MAX}	V_{comp}=2.5V		10		μs
Min ON Time	T_{ON_MIN}			0.45		μs
Maximum Switching Frequency	F_{MAX}		75	100	125	kHz
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			155		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.

Operation

SY22655 is a constant voltage Flyback controller with primary side control and PFC function that targets at LED lighting applications.

The Device provides primary side control to eliminate the opto-couplers or the secondary feedback circuits, which would cut down the cost of the system.

High power factor is achieved by constant on operation mode, with which the control scheme and the circuit structure are both simple.

Start up process is optimized inside SY22655, and quick start up (less than 500ms) is achieved without any additional circuit

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at voltage valley; The start up current of SY22655 is rather small (2 μA typically) to reduce the standby power loss further. The maximum switching frequency is clamped to 100kHz to reduce switching losses and improve EMI performance; Specific design is adopted to ensure good performance when transition.

Adaptive PWM/PFM control is adopted for highest average efficiency.

SY22655 provides reliable protections such as Short Circuit Protection (SCP), Open LED Protection (OLP), Over Temperature Protection (OTP), transformer shorted protection and power diode shorted protection, etc.

SY22655 is available with SOT23-6 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises up to V_{VIN_ON}, the internal blocks start to work. V_{VIN} will be pulled down by internal consumption of IC until the auxiliary winding of Buck transformer could supply enough energy to maintain V_{VIN} above V_{VIN_OFF}.

The whole start up procedure is divided into two sections shown in Fig.4. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

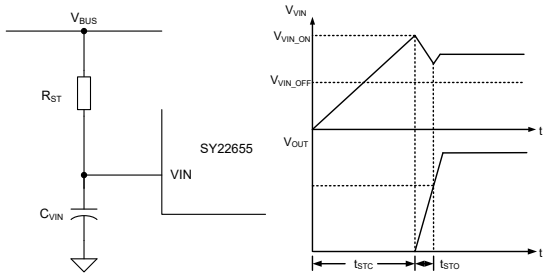


Fig.4 Start up

The start up resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time t_{ST}, and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}}$$

(c) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and re-do such design flow until the ideal start up procedure is obtained.

Internal pre-charge design for quick start up

After V_{VIN} exceeds V_{VIN_ON}, PWM output is enabled. If V_{FB} is lower than certain threshold V_{FB_LOW}, V_{COMP} is pre-charged by the internal current source I_{PRE_CHARGE}, so the output voltage can be built up quickly.

When V_{FB}<0.2V, V_{ISEN} will be limited at 0.4V, when 1.0V≥V_{FB}≥0.2V, V_{ISEN} will be limited at 1.0V.

The V_{COMP_INT} in start-up procedure can be programmed by R_{COMP}:

$$V_{COMP\_INT} = I_{PRE\_CHARGE} \times R_{COMP}$$

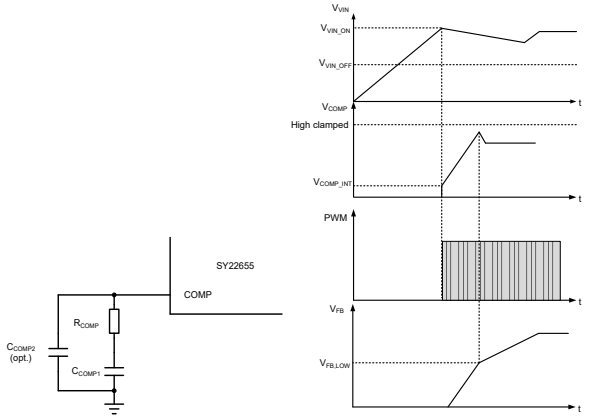


Fig.5 Pre-charge scheme in start up

Once V_{FB} is over V_{FB_LOW}, I_{PRE_CHARGE} is quit and V_{COMP} is under charged of the internal gain modulator. The quick start up process is finished.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer cannot supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working and V_{COMP} will be discharged to zero.

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Flyback converter.

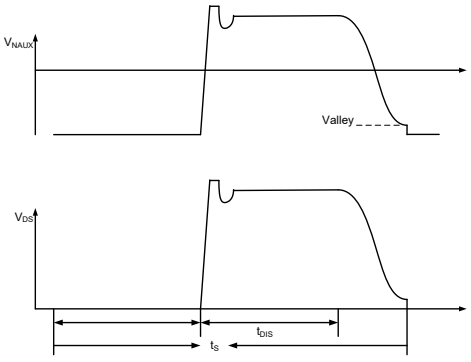


Fig.6 QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

Output Voltage Control

In order to achieve primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage.

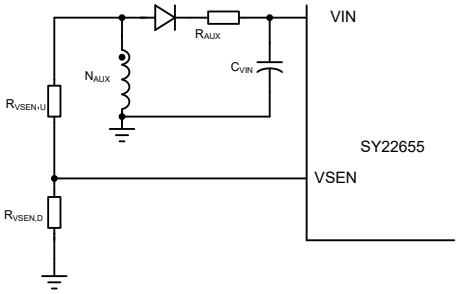


Fig.7 VSEN pin connection

As shown in Fig.6, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D\_F}) \times \frac{N_{AUX}}{N_S}$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage of the power diode.

At the current zero-crossing point, V_{D_F} is nearly zero, so V_{OUT} is proportional with V_{AUX} exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$V_{OUT} = \frac{V_{REFV}}{\frac{R_{VESN\_U}}{R_{VSEN\_U} + R_{VESN\_D}} + \frac{N_{AUX}}{N_S}}$$

Where V_{VSEN_REF} is the internal voltage reference.

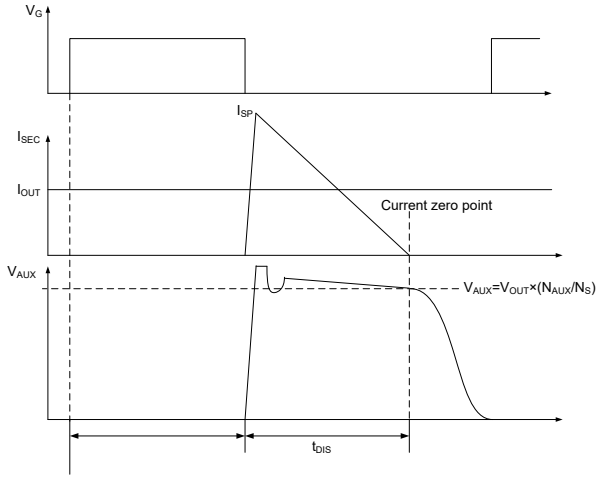


Fig.8 Auxiliary winding voltage waveforms

Special Design for Transition

Aim at good performance on transition, special design is integrate into SY22655.

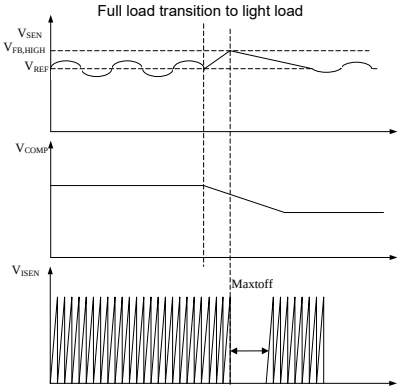


Fig.9 Full load transition to light load

When VSEN touch V_{FB_HIGH}, IC work at Max toff mode to decrease output energy, and COMP is pulled down to decrease the energy output.

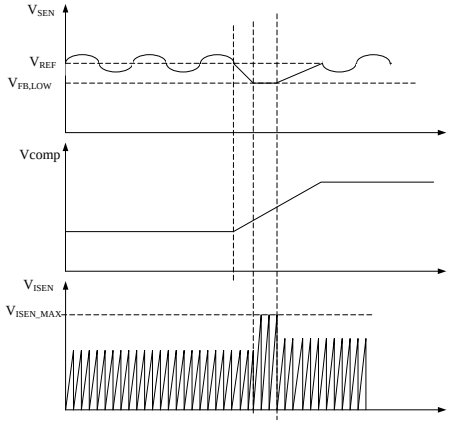


Fig.10 Light load transition to Full load

When VSEN touch V_{FB_LOW}, IC work at Max Ipeak to expedite output energy, and COMP is charged to increase the energy output.

Design of R_{ISEN}

The maximum power inductor current ($I_{P\_PK\_MAX}$) occur in minimum input voltage when full load. So R_{ISEN} could be selected by:

$$R_{ISEN} = \frac{90\% \times V_{ISEN\_LIMIT}}{I_{P\_PK\_MAX}}$$

Where V_{ISEN_LIMIT} is a protection for transformer (If V_{ISEN} touch this voltage, gate will turn off).

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. Without valley detection, MOSFET cannot be turned ON until maximum off time t_{OFF_MAX} is matched. If MOSFET is turned ON by t_{OFF_MAX} 64 times continuously, IC will be shut down and enter into hiccup mode.

Single fault design

If VSEN pin is shorted to GND pin or floating, valley detection is failed, which is similar to SLP, the system will operate in hiccup mode.

If the transformer is shorted, V_{ISEN} will exceeds V_{ISEN_EX}, which will trigger IC latch operation. In latch mode, IC won't work unless AC source restarts. The protection above is also suitable for secondary diode short.

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT}$$

Where V_{AC_MAX} is maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX}$$
$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX}$$
$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX}$$
$$I_{D\_AVG} = I_{OUT}$$

Where $I_{P\text{-}PK\text{-}MAX}$ and $I_{P\text{-}RMS\text{-}MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

Where $V_{MOS\_(BR)DS}$ is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.7.

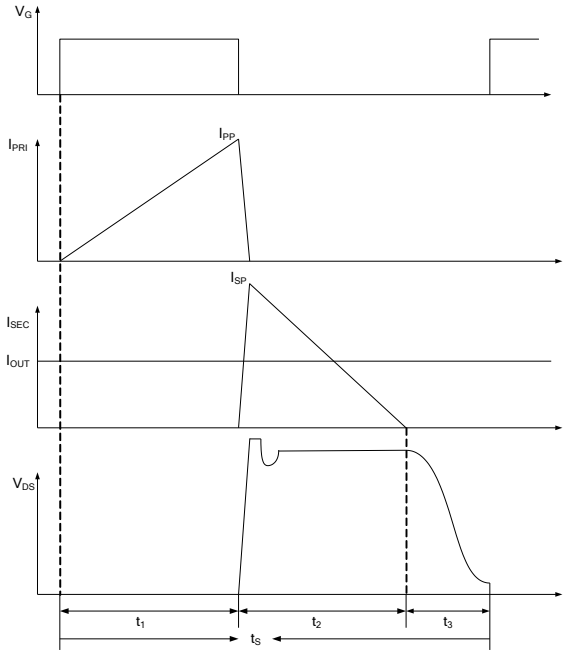


Fig.11 switching waveforms

The system operates in the constant on time mode to achieve high power factor. The ON time increases with the input AC RMS voltage decreasing and the load increasing. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency $f_{S\text{-}MIN}$ happens at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; meanwhile, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency $f_{S\text{-}MIN}$ is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

(b) Preset minimum frequency $f_{S\text{-}MIN}$ (Generally, f_{S_MIN} is not suggested higher than 70 kHz when the input voltage is whole range)

(c) Compute relative t_S, t_1 (t_3 is omitted to simplify the design here)

$$t_S = \frac{1}{f_{S\_MIN}}$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2}V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})}$$

(d) Design inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S}$$

(e) Compute t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}}$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET.

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$ and RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P\_PK\_MAX} = \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta}$$

(20)

Where η is the efficiency; P_{OUT} is rated full load power

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}}$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}}$$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX}$$

(g) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX}$$

$$t_2' = t_S' - t_1' - t_3 \quad (25)$$

$$I_{S\_RMS\_MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX}$$

Transformer design (N_P, NS, NAUX)

The design of the transformer is similar with ordinary Flyback transformer. The parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\text{-}PK\text{-}MAX}$
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e}$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}}$$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}}$$

Where V_{VIN} is the working voltage of VIN pin (10V~20V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT}$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; $V_{D\text{-}F}$ is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}}$$

The C_{RCD} is related with the voltage ripple of the snubber $\Delta V_{C\text{-}RCD}$:

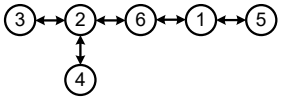
$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}}$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor
Ground ③: ground node of auxiliary winding

Ground ④: ground of signal trace
Ground ⑤: primary ground node of Y capacitor
Ground ⑥: ground node of current sample resistor.

(d) Bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) Loop of ‘Source pin – current sample resistor – GND pin’ should be kept as small as possible.

(f) The resistor divider connected to VSEN pin is recommended to be put beside the IC.

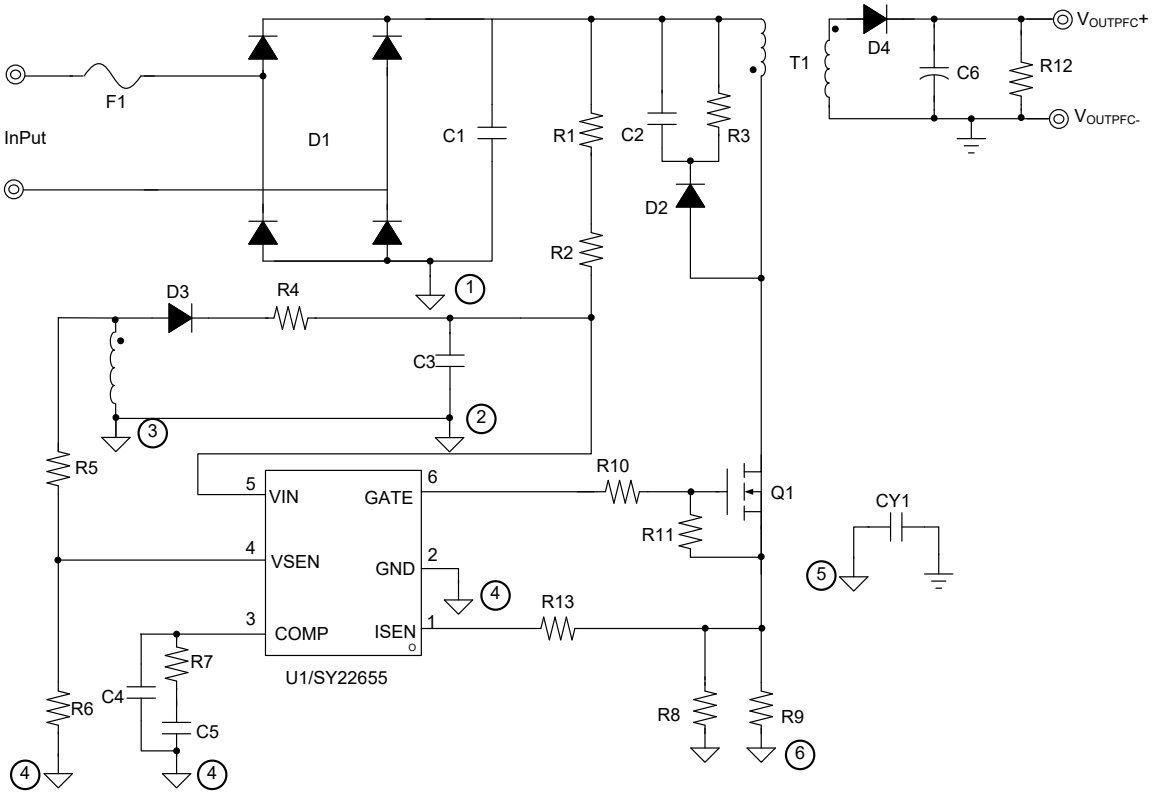
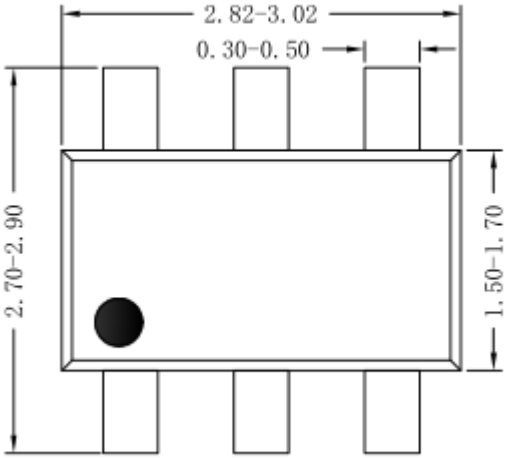
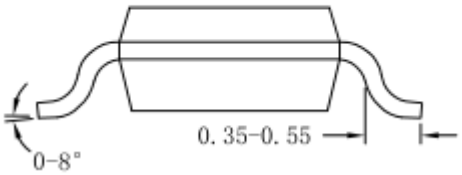


Fig.12 GND connection recommended

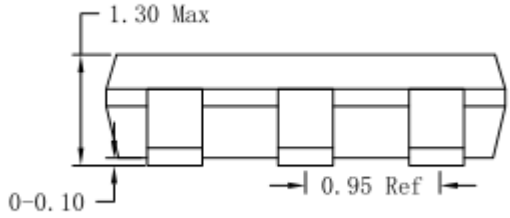
SOT23-6 Package outline & PCB layout design



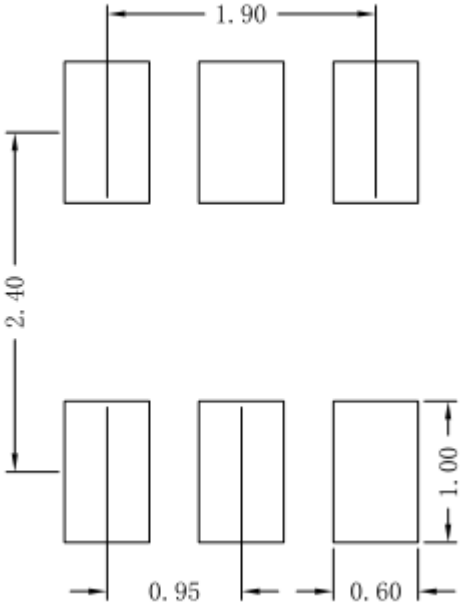
Top View



Side View



Side View

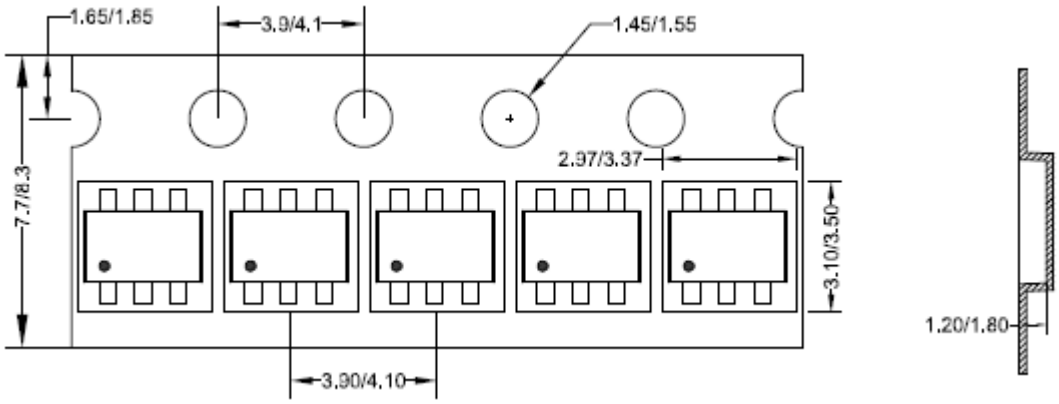


Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

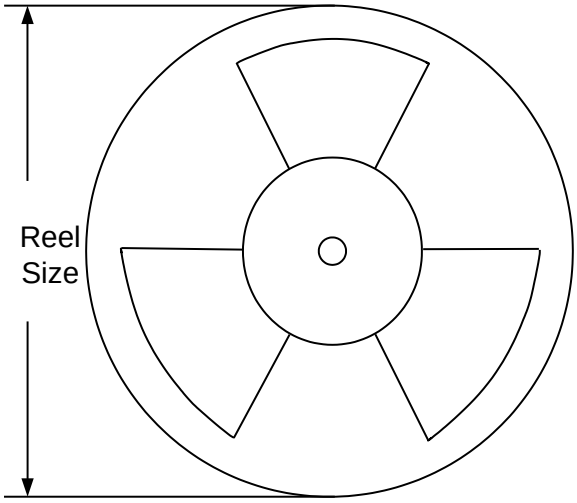
Taping & Reel Specification

1. Taping orientation for packages（SOT23-6）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

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