SY58561

Single Stage Buck PFC LED Driver
Dimmable, High PF and Low BOM Cost

General Description

SY58561 is a single-stage Buck PFC driver for LED lighting applications. Good compatibility is achieved with Leading/Trailing edge dimmer and high PF is achieved without any dimmer.

SY58561 drives the converter in Quasi-Resonant mode to achieve high efficiency. Reliable Open/Short LED protections are integrated.

SY58561 integrates high voltage power FET inside to save driver space further.

SY58561 is available in SOT23-5 package.

Ordering Information

SY58561□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY58561AAC	SOT23-5	----

Features

- Compatible with Leading edge/Trailing edge dimmer
- High PF without any dimmer
- 350V MOSFET integrated
- Quasi-Resonant operation
- Reliable Open/Short LED protection
- Thermal fold back
- Low BOM cost
- Maximum Output Power:10W
- RoHS Compliant and Halogen Free
- Compact package: SOT23-5

Applications

- LED lighting
- Leading edge dimming
- Trailing edge dimming

Typical Applications

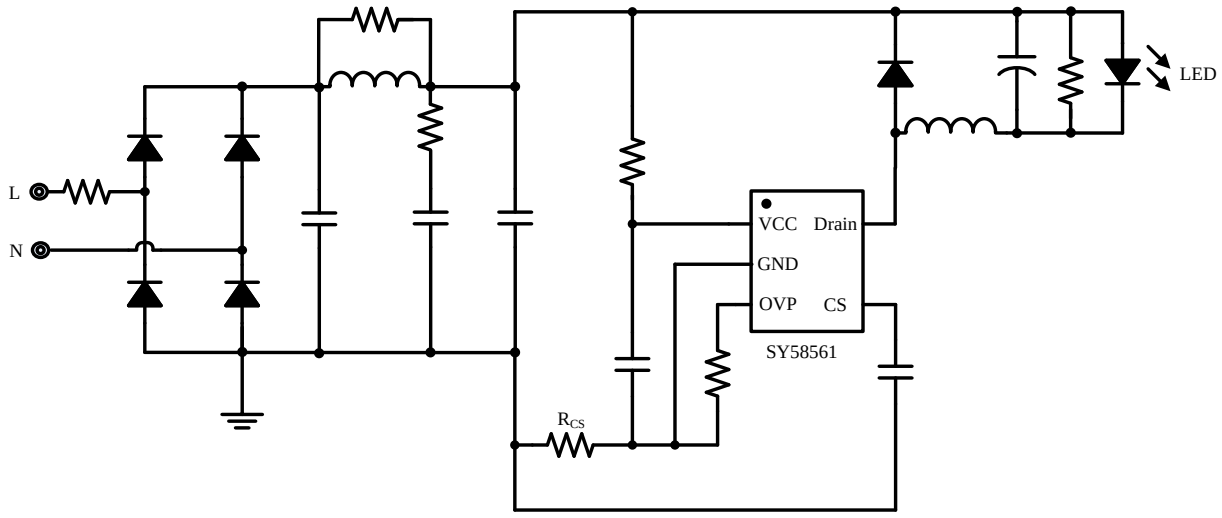
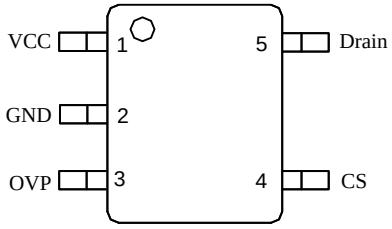


Fig.1 Typical application

Pinout (top view)



(SOT23-5)

Top Mark: Sa*xyz* (device code: Sa, ***x=year code, y=week code, z= lot number code***)

Pin name	Pin Number	Pin Description
VCC	1	Bias supply pin.
GND	2	Ground pin.
OVP	3	Over voltage protection set pin. Connect a resistor to GND.
CS	4	Current sense pin, connect a cap and sense res to GND pin.
Drain	5	Internal MOSFET drain node.

Block Diagram

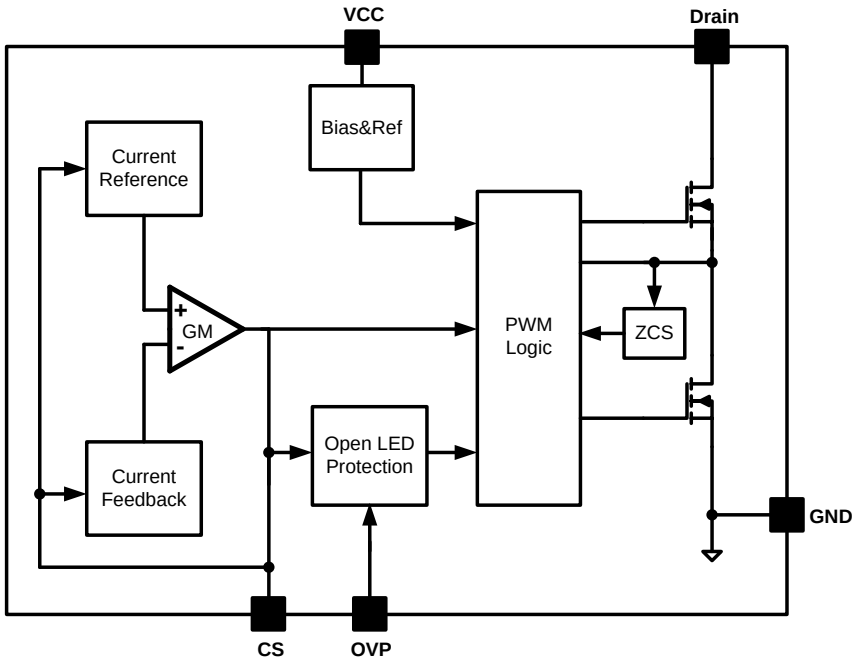


Fig.2 Simplified block diagram

Absolute Maximum Ratings (Note 1)

VCC ---------- -0.3V~20V
I_{VCC} ---------- 4mA
CS, OVP ---------- -0.3V~4V
Drain ---------- 350V
Power Dissipation, @ TA = 25°C SOT23-5---------- 0.6W
Package Thermal Resistance (Note 2)
SOT23-5, θ_{JA}---------- 170°C/W
SOT23-5, θ_{JC}---------- 130°C/W
Maximum Junction Temperature ---------- 165°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 165°C

Recommended Operating Conditions

Junction Temperature Range ---------- −40°C to 125°C

Electrical Characteristics

(V_{VCC} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VCC turn-on threshold	V_{VCC_ON}		13.2	14.1	15.0	V
VCC turn-off threshold	V_{VCC_OFF}		6.5	7.5	8.0	V
VCC shunt voltage	V_{VCC_Shunt}	Ivcc=1.0mA	13.5	14.5	15.5	V
Start up current	I_{ST}		38	50	60	μA
Quiescent current	I_Q		250	310	370	μA
CS pin Section						
Current reference	V_{REF}		500	518	536	mV
Current limit	V_{CS_MAX}		1.6	1.7	1.8	V
OVP pin Section						
OVP Time	T_{OVP}			4.8		us
Driver Section						
Min ON Time	t_{ON_MIN}			500		ns
Min OFF Time	t_{OFF_MIN}			1.5		μs
Max ON Time	t_{ON_MAX}			7.8		μs
Max OFF Time	t_{OFF_MAX}			250		μs
Integrated MOSFET Section						
BV of HV MOSFET	V_{BV}		350			V
HV MOS Drain source resistance	R_{DS_ON}			4.2	5.5	Ω
Thermal Section						
Thermal fold back temperature	T_{FB}			160		ºC
Thermal shut down temperature	T_{SD}			T_{FB} +5		ºC

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2 x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 3: Increase VCC pin voltage gradually higher than V_{VCC_ON} voltage then turn down to 12V.

Operation

The SY58561 is a single stage Buck PFC regulator targeting at LED lighting applications.

It is mainly used on dimming applications and has good compatibility with Leading/Trailing edge dimmer.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at the valley of drain voltage.

It also provides reliable open/short LED protections and over temperature protection.

The IC is available with SOT-23 package.

Applications Information

Start up

After AC supply is powered on, the capacitor C_{VCC} between VCC and GND pin is charged up by BUS voltage. Once V_{VCC} rises up to V_{VCC_ON}, the internal blocks start to work and V_{CS} is pre-charged to certain value.

The whole start up procedure is divided into three sections as shown below. t_{ST1} is the C_{VCC} charged up time. t_{ST2} is the time V_{CS} is charged up to certain value. t_{ST3} is the time IC works at steady state. Usually t_{ST2} is much smaller than t_{ST1}.

If bias supply has more power than IC consumption, V_{VCC} is greater than V_{VCC_Shunt}, then a shunt current starts to work.

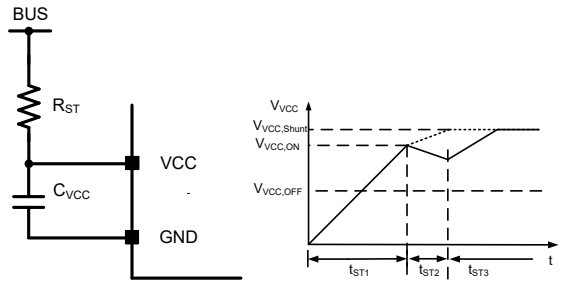


Fig.3 Start up

The start up component R_{ST} and C_{VCC} are designed as below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} .

$$R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

For dimming applications, make sure that the current through R_{ST} is larger than I_Q. In the minimum angle of dimmer, the V_{BUS_MIN} is equal to the LED voltage.

$$R_{ST} < \frac{V_{BUS\_MIN} - V_{VCC\_OFF}}{I_Q}$$

$$V_{BUS\_MIN} = V_{LED\_Min\_Current}$$

(b) Select C_{VCC} to obtain an ideal start up time t_{ST} , and to make sure that the V_{VCC}>V_{VCC_OFF} in t_{ST2}.
The recommended formula is as below:

$$C_{VCC} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VCC\_ON}}$$

Shut down

After AC supply is powered off, the energy stored in the BUS capacitor is discharged. When power supply for IC is not enough, V_{VCC} drops down. Once V_{VCC} is below V_{VCC_OFF}, the IC stops working.

LED current setting

The LED current is set by the resistor R_{CS}. The relationship is as below:

$$I_{LED} = \frac{V_{REF}}{2 \times R_{CS}}$$

Open LED protection

The protection voltage V_{OVP} for open LED is set by the resistor R_{OVP} between OVP pin and GND pin. The relationship is shown as below:

$$R_{OVP} = \frac{L_M \times K_{OVP}}{V_{OVP} \times R_{CS} \times T_{OVP}}$$

K_{OVP} is typically 2200(V • Ω). If over voltage protection is triggered, the PWM output is stopped and V_{VCC} is discharged. Once V_{VCC} drops down to V_{VCC_OFF}, the IC stops working and then starts up again.

Short LED protection

If LED is short, the PWM output is stopped and V_{VCC} is discharged. Once V_{VCC} drops down to V_{VCC_OFF} , the IC stops working and then starts up again.

Thermal treatment

Thermal fold back is adopted in this IC. Thermal fold back curve is shown as below.

When the junction temperature rises high, internal current reference decreases first; if the junction temperature still rises up over T_{SD}, IC will be shut down.

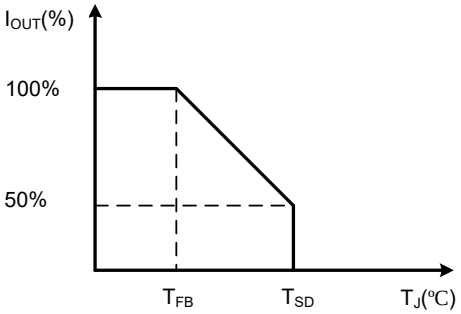


Fig.4 Thermal foldback curve

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage, the voltage stress of MOSFET and output power diode is maximized. MOSFET is integrated with 350V BV.

$$V_{DS\_MAX} = \sqrt{2}V_{AC\_MAX}$$

Where V_{AC_MAX} is maximum input AC RMS voltage.

Inductor (L)

In Buck converter, the power transfers from AC input to output only when the input voltage is larger than the output voltage. The input voltage and inductor current waveforms are shown below, where θ_3 and θ_4 are the time that input voltage is equal to output voltage.

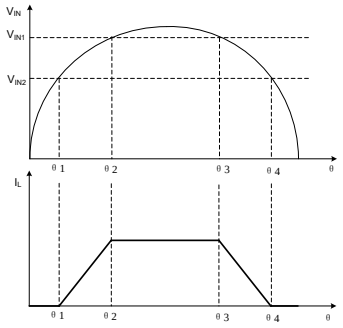


Fig.5 Input and output waveforms

The system operates in the peak current mode. The ON time increases with the input voltage decreasing. When the ON time reaches T_{ON_MAX}, the ON time is limit by T_{ON_MAX}. Where θ_1 and θ_2 are the time that ON time is equal to T_{ON_MAX}.

In Quasi-Resonant mode, each switching period t_S consists of three parts: inductor current rising time t_1, falling time t_2 and quasi-resonant time t_3.

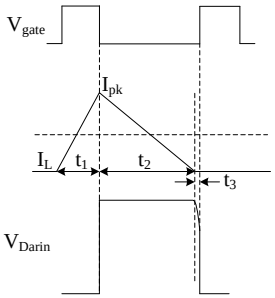


Fig.6 switching waveforms

The switching frequency is designed in rated input voltage considering conducted EMI test. Once the switching frequency f_{SW} is set, the inductance of the inductor could be calculated.

The design flow is shown as below:

(a) Preset frequency f_{SW}

(b) Compute relative t_S, t_1

$$t_S = \frac{1}{f_{SW}}$$

$$t_1 = \frac{t_S \times (V_{OUT} + V_{DF})}{(\sqrt{2}V_{AC\_MIN} + V_{DF})}$$

$$t_2 = t_S - t_1$$

Where V_{DF} is the forward voltage of diode, V_{AC_MIN} is the RMS value of minimum input voltage.

(c) Compute the peak current of inductance I_{PK}.

$$\theta_1 = \arcsin\left(\frac{V_{OUT}}{\sqrt{2}V_{AC\_MIN}}\right)$$

$$\theta_2 = \arcsin\left(\frac{\frac{\sqrt{2}V_{AC\_MIN} - V_{OUT}}{t_{ON\_MAX}} \times t_1 + V_{OUT}}{\sqrt{2}V_{AC\_MIN}}\right)$$

$$I_{PK}=\frac{2\times I_{OUT}}{1-\frac{\theta_1}{\pi}-\frac{\theta_2}{\pi}}$$

Where V_{OUT} is the rated output voltage, I_{OUT} is rated output current.

(d) Design inductance L

$$L=\frac{(\sqrt{2}V_{AC\_RMS\_R}-V_{OUT})\times t_1}{I_{PK}}$$

Inductor design (N)

Necessary parameters:	
Inductance	L
Io program resistor	R_{CS}
Current limit voltage	V_{REF}

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB.
For PC40, ΔB select 0.3~0.33T at 25° C.

(c) Compute inductor maximum peak current $I_{L\_PK\_MAX}$ and maximum RMS current $I_{L\_RMS\_MAX}$.

$$I_{L\_PK\_MAX}=\frac{V_{CS\_MAX}-V_{REF}}{R_{CS}}$$

$$I_{L\_RMS\_MAX}=\frac{1}{\sqrt{3}}I_{L\_PK\_MAX}$$

(d) Compute turn N

$$N=\frac{L}{\Delta B\times A_e}\times I_{L\_PK\_MAX}$$

(e) Select an appropriate wire diameter with $I_{L\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(f) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the inductor until the ideal inductor is achieved.

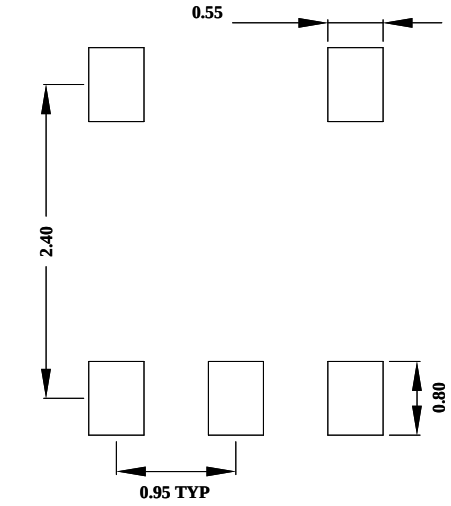
Output capacitor COUT

Choose proper output capacitance to satisfy current ripple. Output current ripple is set to ΔI_O, then,

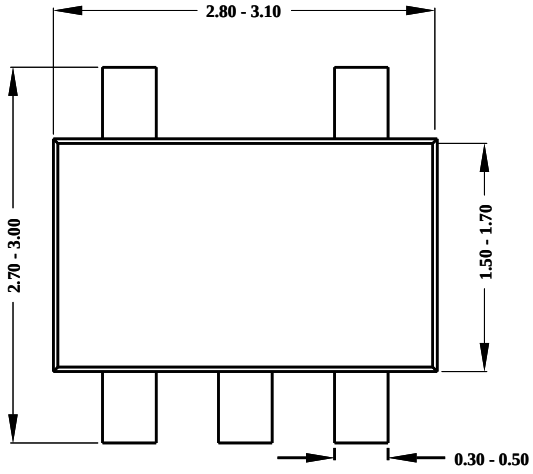
$$C_{OUT}=\frac{\sqrt{\left(\frac{2I_{OUT}}{\Delta I_O}\right)^2-1}}{4\pi\times R_{LED}\times f_{AC}}$$

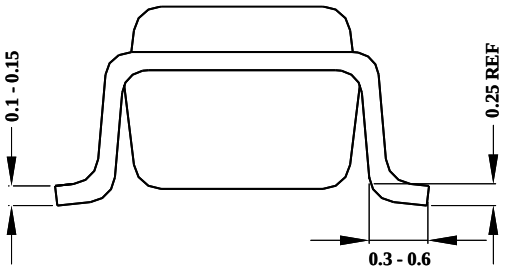
Where f_{AC} is the AC supply frequency; R_{LED} is the equivalent series resistor of LED load.

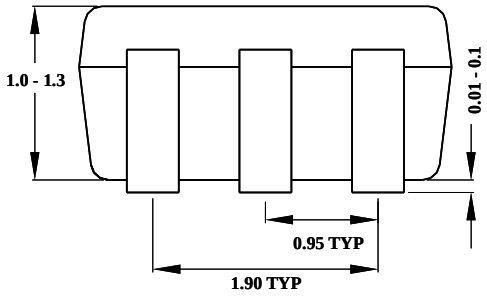
SOT23-5 Package outline & PCB layout design



Recommended Pad Layout



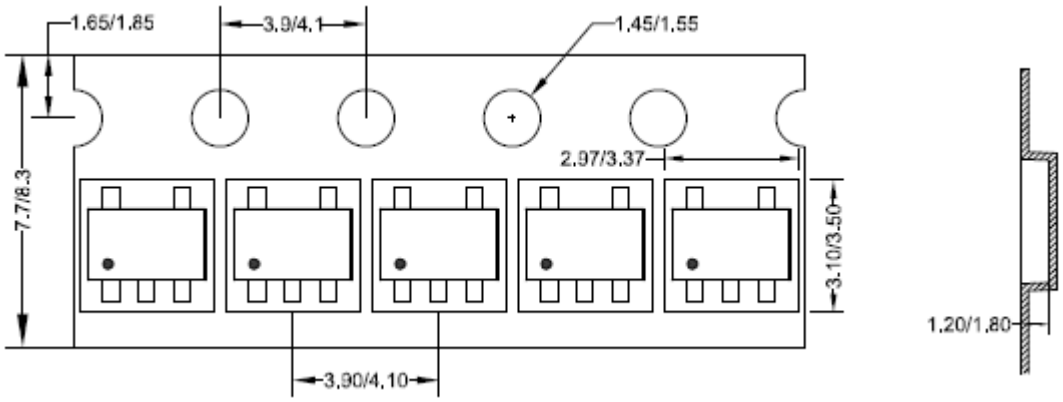




Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

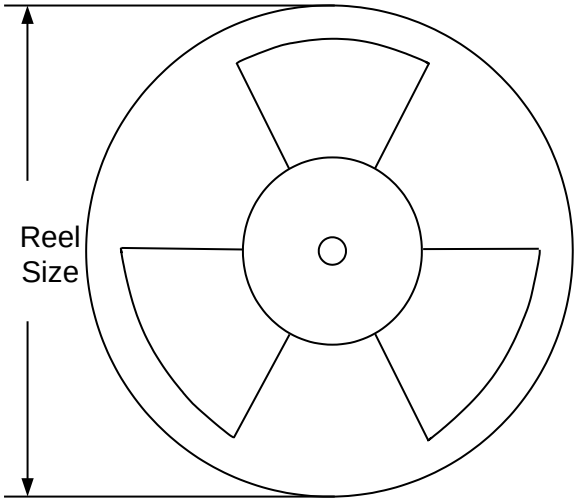
Taping & Reel Specification

1. Taping orientation for packages（SOT23-5）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	280	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
October 20,2018	Revision 0.9	Initial Risk Production Release
October 20,2019	Revision 1.0	Initial Production Release

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