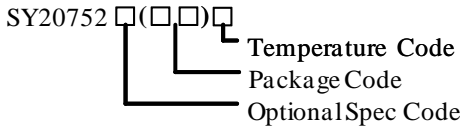


General Description

SY20752A is a 4.0-23V input, 2A single-cell synchronous buck Li-Ion battery charger. The compact package QFN4×4-16 is widely suitable for portable application. Select pin is convenient for different cell voltage. It allows the output power path management and input reverse blocking. Integrated 800 kHz synchronous Buck regulator consists of 23V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

Ordering Information



Ordering Number	Package type	Note
SY20752AQIC	QFN4×4-16	

Features

- Wide Input Voltage Range: 4.0V to 23V
- High Efficiency Int. Synchronous Buck Regulator with Fixed 800kHz Switching Frequency
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Adaptive input current limit
- Programmable Charging Timeout
- 4.35 and 4.2V selectable cell voltage
- Programmable (2A MAX) Constant Charge Current
- External Shutdown Function
- Input Voltage UVLO and Battery OVP
- Over Temperature Protection
- Output Short Circuit Protection
- Charge Status Indication
- Normal Synchronous Buck Operation when Battery Removed
- Compact package QFN4×4-16

Applications

- Cellular Telephones,
- PDA, MP3 Players, MP4 Players
- Digital Cameras
- Bluetooth Applications
- PSP Game Players, NDS Game Players
- Notebook

Typical Application

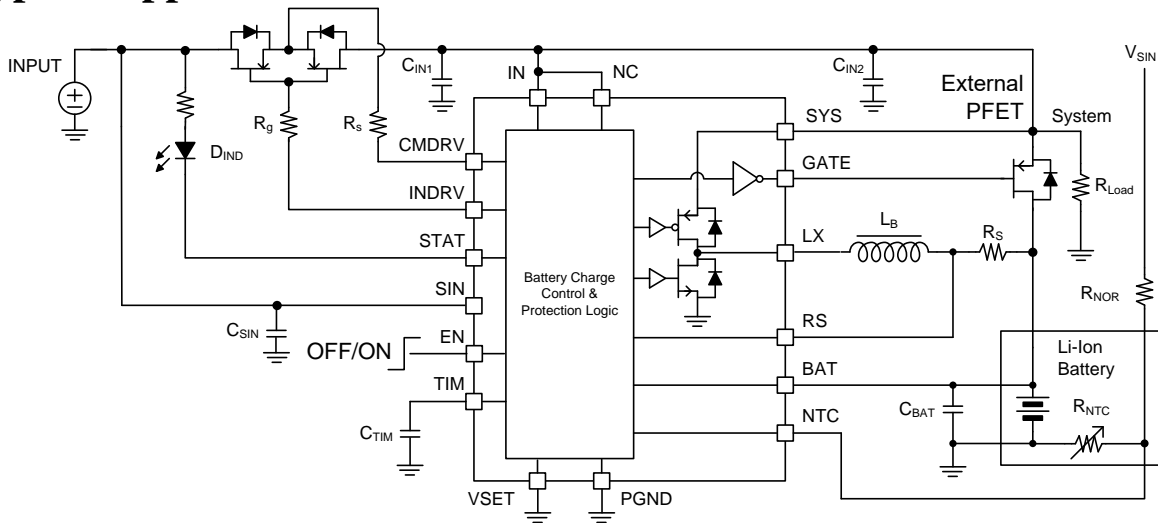
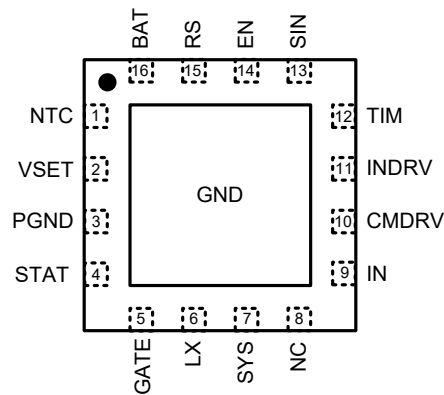


Figure1. Schematic Diagram

Pinout (top view)



(QFN4×4-16)

Top Mark: ALAxyz (device code: **ALA**, *x=year code*, *y=week code*, *z=lot number code*)

Name	Number	Description
NTC	1	Thermal protection pin. UTP threshold is about 75% V_{SIN} and OTP threshold is about 30% V_{SIN} . Pull up to V_{SIN} can disable charge logic and make the IC operate as normal buck regulator. Pull down to ground can shut down the IC.
VSET	2	VSET is for 4.2V and 4.35V selection.
PGND	3	Power ground pin.
STAT	4	Charge status indication pin. It is open drain output pin and can be used to turn on a LED to indicate the charge in process. When the charge is done, LED is off.
GATE	5	Drive the external bypass PFET from BAT pin to SYS pin.
LX	6	Switch node pin. This pin connects the drains of the integrated main and synchronous power MOSFET switches. Connect to external inductor.
SYS	7	System load pin. High side of the internal integrated half-bridge. Connect a MLCC from this pin to ground to decouple high frequency Noise.
NC	8	Null pin. Suggest connect this pin to IN. Do not connect to GND.
IN	9	Positive power supply input pin. V_{IN} ranges from 4V to 23V for normal operation.
CMDRV	10	Connect to common source of P-channel input reverse blocking Bi-directional FET.
INDRV	11	P-channel input reverse blocking Bi-directional FET gate driver pin. This internal gate driver is asymmetrical with quick turn-off speed and slow turn-on speed.
TIM	12	Charge time limit pin. Connect this pin with a capacitor to ground. Internal current source charge the capacitor for TC mode and CC mode's charge time limit. TC charge time limit is about 1/9 of CC charge time.
SIN	13	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic Noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area. It must be 300mV greater than the battery voltage to enable normal operation.
EN	14	System enable pin. Pull high to enable the normal operation and pull down to shut down the charger.
RS	15	Charge current program pin. Connect a current sensor from RS pin to BAT pin. Average charge current is detected for TC mode and CC mode both.
BAT	16	Battery positive pin.
GND	Exposed pad	Ground pin.



Absolute Maximum Ratings (Note 1)

IN, SIN, BAT, RS, LX, SYS, ILM, CMDRV	-0.5- 25V
EN, VSET, TIM, NTC, STAT	-0.5- 25V
INDRV	-0.5- 29V
LX Pin Current Continuous	2A
Power Dissipation, P _D @ T _A = 25°C, QFN4×4-16	2.4W
Package Thermal Resistance (Note 2)	
θ _{JA}	41°C/W
θ _{JC}	20°C/W
Junction Temperature Range	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 125°C
ESD Susceptibility (Note 2)	
HBM (Human Body Mode)	2kV
MM (Machine Mode)	200V

Recommended Operating Conditions

IN, SIN, BAT, RS, LX, SYS, ILM, CMDRV	less than 23V
EN, VSET, TIM, NTC, STAT	less than 23V
INDRV	less than 26V
LX Pin Current Continuous	less than 1.5A
Junction Temperature Range	-20°C to 100°C
Ambient Temperature Range	-40°C to 85°C

Electrical Characteristics

T_A=25°C, V_{IN}=15V, GND=0V, C_{IN}=10μF, L_B=6.8μH, R_S=25mΩ, C_{TIM}=330nF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{SIN})						
Supply Voltage	V _{SIN}		4.0		23	V
V _{SIN} Under Voltage Lockout Threshold	V _{UVLO}	V _{SIN} rising and measured from V _{SIN} to GND			3.9	V
V _{SIN} Under Voltage Lockout Hysteresis	ΔV _{UVLO}	Measured from V _{SIN} to GND		190		mV
Input Over Voltage Protection	V _{OVF}	V _{SIN} rising and measured from V _{SIN} to GND	23			V
Input Over Voltage Protection Hysteresis	ΔV _{OVF}	Measured from V _{SIN} to GND		750		mV
Quiescent Current						
Battery Discharge Current	I _{BAT}	Enable off			25	μA
Input Leakage Current	I _{SIN}	Disable Charge			1.5	mA
Oscillator and PWM						
Oscillator Frequency	f _{OSC}		640	800	960	kHz
PFET Duty Cycle	D				100	%
Power MOSFET						
R _{DS(ON)} of N-FET	R _{NFET}	Include bond-wire		150		mΩ
R _{DS(ON)} of P-FET	R _{PFET}			160		mΩ



Voltage Regulation						
Low VSET for 4.2V cell voltage	V _{CV}	0°C ≤ T _A ≤ 70°C	4.16	4.20	4.24	V
High VSET for 4.35V Cell Voltage			4.30	4.35	4.40	
4.2V CV Threshold for Recharge	ΔV _{RCH}	0°C ≤ T _A ≤ 70°C	50	100	150	mV
4.35V CV Threshold for Recharge			100	150	200	
TC Charge Mode Voltage Threshold	V _{TRK}	0°C ≤ T _A ≤ 70°C	2.2	2.5	2.8	V
Battery Connect Detection						
Detect Voltage Threshold	V _{DET}	V _{SHOT} < V _{BAT} < V _{RCH}	80%		90%	V _{SIN}
Detect Delay Time	t _{DET}		30	35	40	ms
Charge Current						
Internal Charge Current Accuracy for Constant Current Mode		I _{CC} =25mV/R _S	-10%		10%	
Internal Charge Current Accuracy for Trickle Current Mode		I _{TC} =2.5mV/R _S	-50%		50%	
Charge Termination						
Charge Termination Current	I _{TERM}			10%		I _{CC}
Termination Delay Time	T _{TERM}			30		ms
Input current limit slow response						
IN Voltage Falling Threshold at High Current	V _{INSL}			4.6		V
IN Voltage Hysteresis at High Current	ΔV _{INSL}			50		mV
Input Current Limit Quick Response						
IN Voltage Falling Threshold at High Current	ΔV			4.4		V
IN Voltage Hysteresis at High Current	ΔV _{INQK}			100		mV
Output Voltage OVP						
Output Voltage OVP Threshold	V _{OVP}		105%	110%	115%	V _{CV}
Output Short Protection						
Output Short Protection Threshold	V _{SHOT}	V _{BAT} falling edge	1.70	2.00	2.30	V
Frequency Fold Back	f _{FBK}	V _{BAT} < 2V/CELL		12.5%		f _{OSC}
Power FET Current Limit	I _{LM}			3.0		A
Reverse Blocking FET Driver						
Gate Voltage from CMDRV to INDRV	VGATE		4.2	6		V



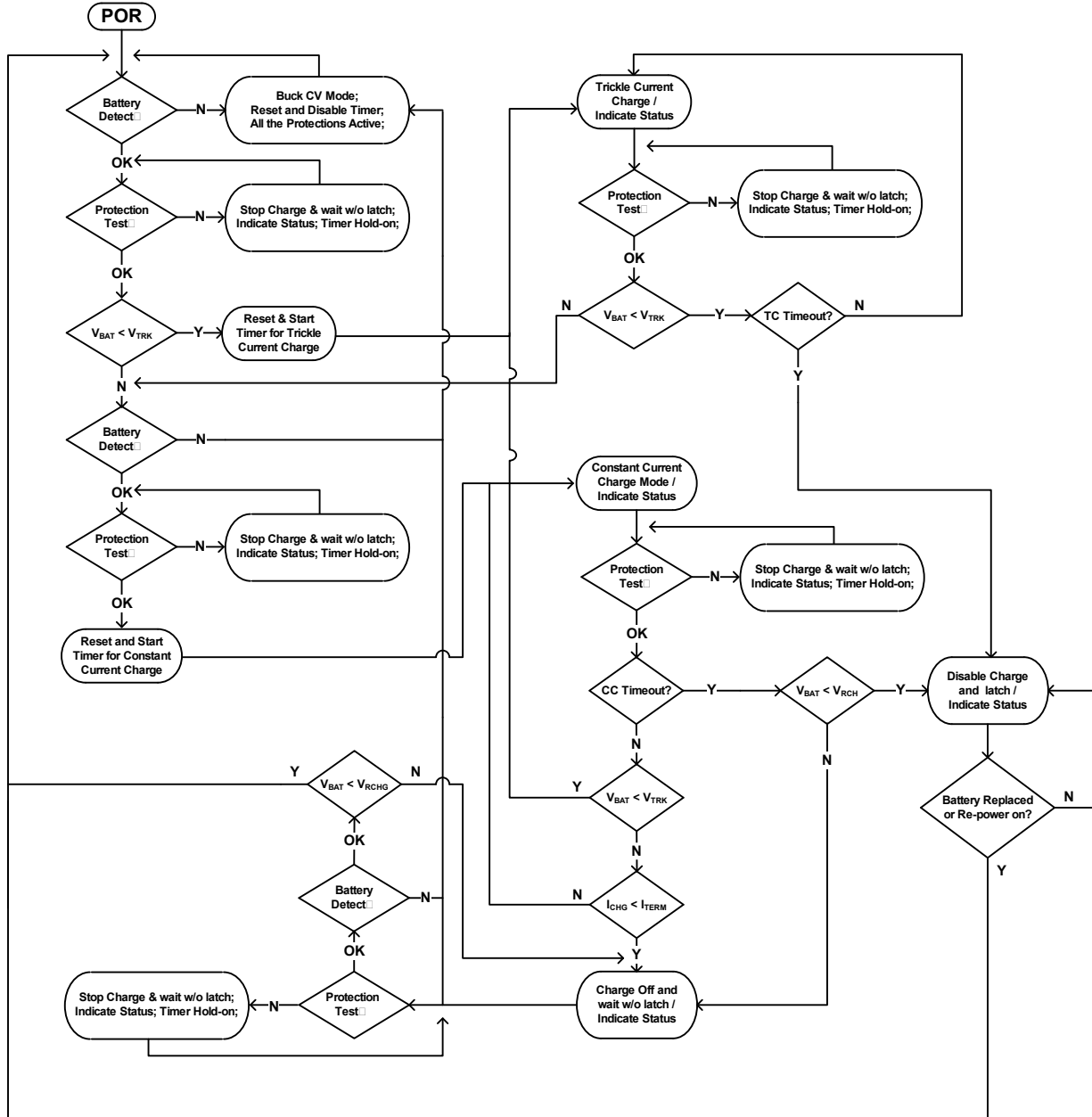
Enable						
Enable Voltage Rising Threshold	V_{ENH}		1.5			V
Enable Voltage Falling Threshold	V_{ENL}				0.4	V
Timer						
Trickle Current Charge Timeout	t_{TC}	$C_{TIM}=330nF$	0.23	0.5	0.67	hour
Constant Current Charge Timeout	t_{CC}		3.0	4.5	6.0	hour
Charge Mode Change Delay Time	t_{MC}			30		ms
Recharge Time Delay	t_{RCHG}			30		ms
Power Path Switch Dead Time						
Dead Time Between Power Path Switch	t_{DRV_DEAD}			10		us
Input Reverse Blocking FETs On/Off Threshold		Measured from V_{SIN} to V_{BAT}		120		mV
Output Power Path FETs On/Off Threshold		Measured from V_{SIN} to V_{BAT}		-160		mV
Battery Thermal Protection NTC						
Under Temperature Protection	UTP		70%	75%	80%	V_{SIN}
Under Temperature Protection Hysteresis		Falling edge			5%	
Over Temperature Protection	OTP		28%	30%	32%	
Over Temperature Protection Hysteresis		Rising edge			2%	
Automatic Shutdown						
ASD Voltage Threshold Hysteresis	ΔV_{ASD}	Measured from V_{SIN} to V_{BAT}		80		mV
Thermal Shutdown						
Thermal Shutdown Temperature	T_{SD}	Rising Threshold		160		°C
Thermal Shutdown Temperature Hysteresis	T_{SDHYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

Basic Li-Ion Battery Charge Operation Flow Chart



General Function Description

SY20752A is a 4.0-23V input, 2A single-cell synchronous Buck Li-Ion battery charger. The compact package QFN4×4-16 is widely suitable for portable application. VSET pin is convenient for selecting 4.35V or 4.2V cell voltage. Integrated 800kHz synchronous buck regulator consists of 23V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

Charging Status Indication Description

1. **Charge-In-Process** – Pulls and keeps STAT pin to Low;
2. **Charge Done** – Pulls and keeps STAT pin to High;
3. **Fault Mode** – Outputs high and low voltage alternatively with 0.5Hz frequency when the C_{TIM} is 330nF.

Connects a LED from V_{SIN} to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flash means Fault Mode.

Buck Regulator Operation Description

If the Li-Ion battery is absent suddenly, the output battery load current drawn from BAT pin pulls down the voltage across the C_{BAT} until reaching the recharge threshold 4V. Then, SY20752A can operate as a normal peak current mode controlled synchronous buck converter and the output voltage on BAT pin is regulated at V_{CV} . In this operation mode, the input current limit and the constant output current loop are still active, however the charge timeout and the trickle current charge are disabled both.

Protection Description

Thermal Protection-Thermal shutdown is active for battery and IC both. IC recovers to normal work when the temperature backs in normal range again. Timer stop and hold-on without reset.

Short Circuit Protection- When V_{BAT} voltage is lower than the short circuit protection threshold, short circuit protection is active. The switching frequency is fold

back to 12.5% of the default value. During this mode, if the battery exists, the trickle charge timer is still active and would timeout the IC finally.

Over Current Protection- The internal current loop with different constant current capability is always active no matter in Buck mode or Battery Charging mode for the over current protection.

Over Voltage Protection- When V_{BAT} voltage is higher than the over voltage protection threshold no matter with or without battery connecting, IC shuts down and recovers to normal work when V_{BAT} backs to normal level. Input voltage has UVLO and OVP, which would make IC shutdown and recover to normal work when the V_{SIN} backs to normal range.

Adaptive Input Current Limit- When the input is drawn from a USB port, SY20752A will adaptively limit the current if the input current is over the USB supply capability.

Timeout Protection-Programmable timeout protection is for both Trickle Current Charge Mode and Constant Current Charge Mode. Once timeout is active, IC stops the charge operation and latches off. Only power or battery re-plug in can get the latch logic reset and the IC restarted.

Output Power Path Management Description

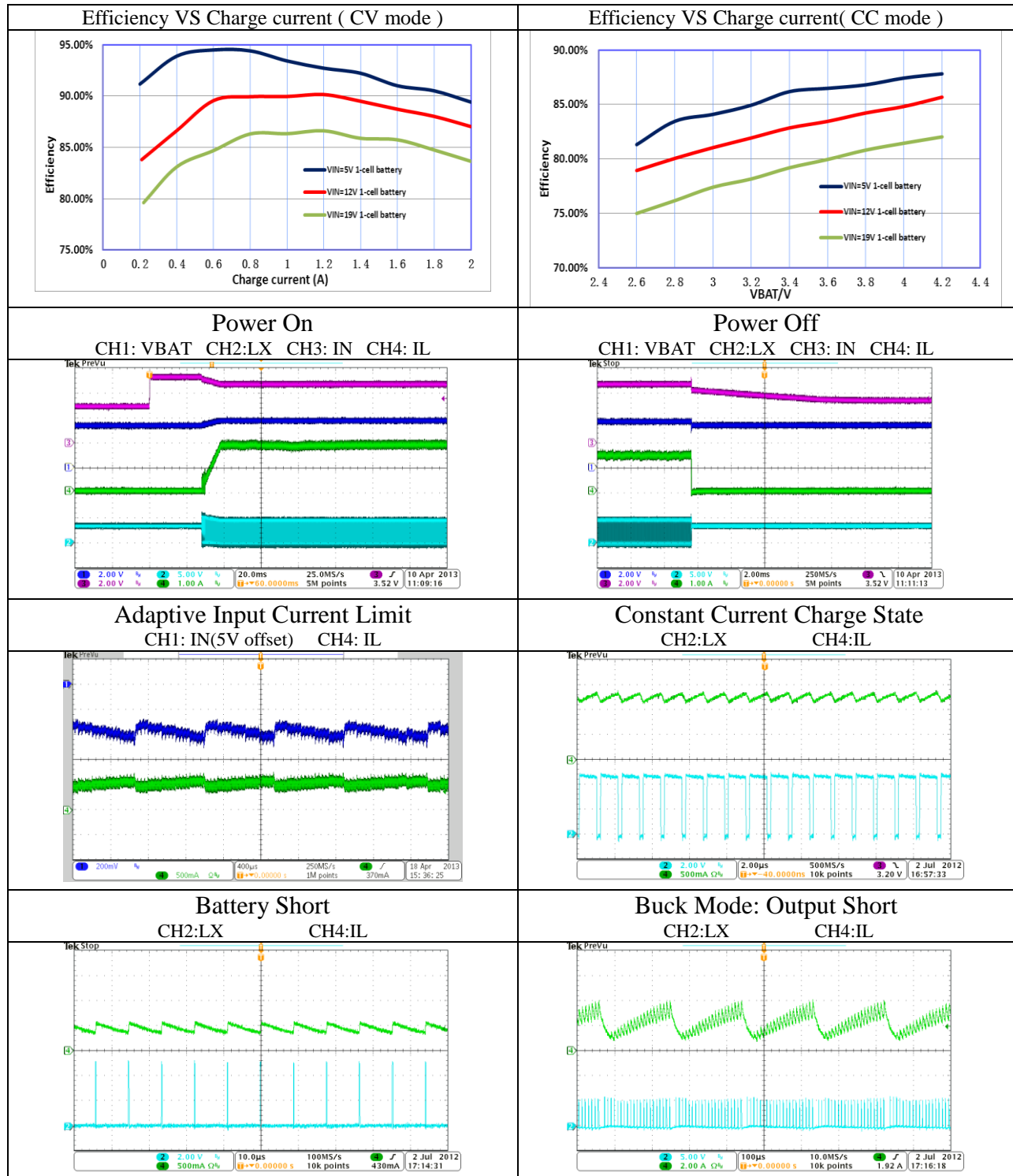
When the voltage on SIN pin rises up, if the voltage drop of V_{SIN} to V_{BAT} is higher than -100mV, the output power path FET turns off. When this voltage drop is higher than 120mV, the input reverse blocking FETs turn on, then system load draws power from input source directly.

When the voltage on SIN pin falls down, if the voltage drop of V_{SIN} to V_{BAT} is lower than 80mV, the charger stops working and the input reverse blocking FETs turn off. When this voltage drop is lower than -160mV, the output power path FET turns on, then system load draws power from battery.

The input current limit loop reduces the charging current adaptively when the system load is heavy.

Typical Performance Characteristics

$T_A=25^\circ\text{C}$, $V_{IN}=5\text{V}$, $R_S=20\text{m}\Omega$, 1cell battery, unless otherwise specified.



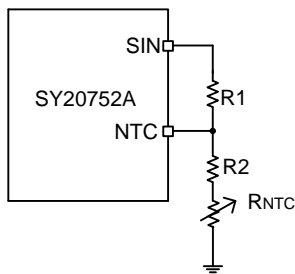
Applications Information

Because of the high integration of SY20752A, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN} , output capacitor C_{OUT} , inductor L , NTC resistors $R1, R2$, charge current sense resistor R_s and timer capacitor C_{TIM} need to be selected for the targeted applications specifications.

NTC Resistor

SY20752A monitors battery temperature by measuring the input voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K ($K = V_{NTC}/V_{SIN}$) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.

Choose $R1$ and $R2$ to program the proper UTP and OTP points.



The calculation steps are:

1. Define K_{UT} , $K_{UT} = 70\sim 80\%$
2. Define K_{OT} , $K_{OT} = 28\sim 32\%$
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate $R2$,

$$R2 = \frac{K_{OT}(1 - K_{UT})R_{UT} - K_{UT}(1 - K_{OT})R_{OT}}{K_{UT} - K_{OT}}$$

5. Calculate $R1$

$$R1 = (1 / K_{OT} - 1)(R2 + R_{OT})$$

If choose the typical values $K_{UT} = 75\%$ and $K_{OT} = 30\%$, then

$$R2 = 0.17R_{UT} - 1.17R_{OT}$$

$$R1 = 2.3(R2 + R_{OT})$$

Charge Current Sense Resistor R_s

The charge current sense resistor R_s is calculated as below:

$$R_s = \frac{25}{I_{CHG}}, \quad \text{Unit: } m\Omega$$

While the I_{CHG} is the battery constant charge current.

Timer Capacitor C_{TIM}

The charger also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is given by the formula:

$$C_{TIM} = 2 \times 10^{-11} T_{CC}$$

Unit: F

T_{CC} is the target constant charge time, measured in seconds.

Input Capacitor C_{IN}

The ripple current through input capacitor is greater than

$$I_{CIN_MIN} = I_{CHG} \sqrt{D(1 - D)}$$

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND pins.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor with 10uF capacitance.

Output Inductor L

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20752A regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times F_{SW} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with $DCR < 10\text{mohm}$ to achieve a good overall efficiency.

Layout Design

The layout design of SY20752A regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN} , L, R_1 and R_2 .

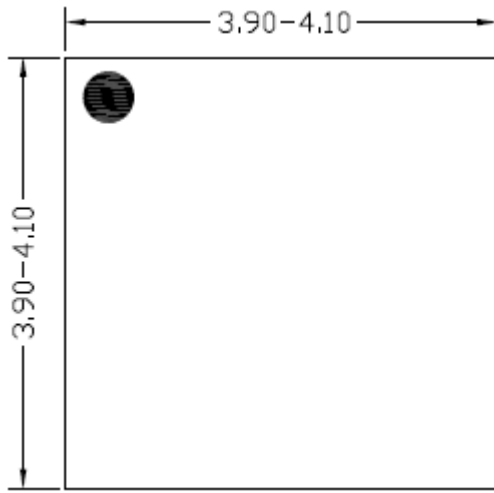
- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

- 2) C_{IN} must be close to pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

- 3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

- 4) The capacitor C_{TIM} and the trace connecting to the TIM pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem. It should be better to ground C_{TIM} to the output Capacitor's ground.

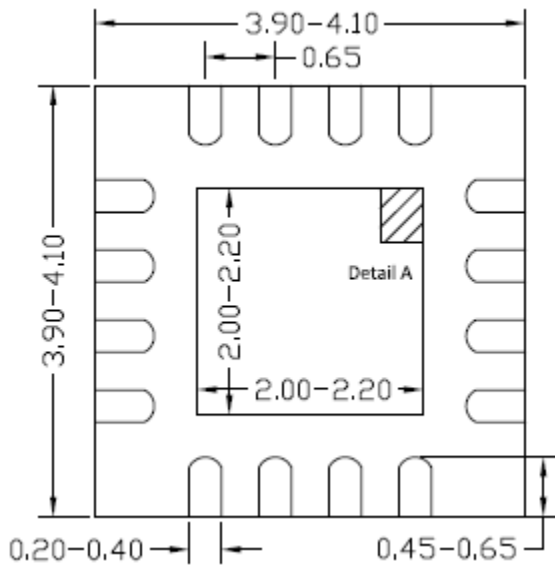
QFN4×4-16 Package Outline Drawing



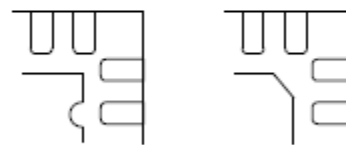
Top View



Side View



Bottom View



Detail A
Pin1 Identifier: two options

Notes: All dimension in millimeter and exclude mold flash & metal burr.



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