SY20761B
High Efficiency, 2A
Two-cell Boost Li-Ion Battery Charger

General Description

The SY20761B is a synchronous Boost Li-ion battery charger for 2-cell with 3.6V-5.5V input, which integrates the power MOSFETs working with 1MHz switching frequency and the full protection functions. The charge current is up to 2A which can be programmed by using an external resistor for different portable applications. The IC can indicate the charge current information simultaneously. It also has a programmable charge timeout for safe battery charge operation and a programmable input voltage threshold for adaptive input current limit. The SY20761B can disconnect output when there is an output short circuit or shutdown. The IC consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

The SY20761B is available in QFN3×3 package to minimize the PCB layout size for wide portable application.

Ordering Information

SY20761 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20761BQDC	QFN3×3-16	

Features

- Low Profile QFN3×3 Package
- Integrated Synchronous Boost with 18V Rating Low R_{DSON} FETs for High Charge Efficiency
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Programmable Input Voltage Threshold for Adaptive Current Limit.
- Maximum 2A Constant Charge Current
- Charge Current Information Indication.
- Programmable Charge Timeout
- Programmable Constant Charge Current
- Selectable Constant Voltage
- ±0.5% Battery Voltage Accuracy
- Thermal Foldback Protection
- External Shutdown Function
- Input Voltage UVLO and OVP
- Over Temperature Protection
- Output Short Circuit Protection
- Charge Status Indication
- Normal Synchronous Boost Operation When Battery is Removed

Applications

- Cellular Telephones, PDA, MP3/MP4 Players
- Digital Cameras
- Bluetooth Applications
- PSP Game Players, NDS Game Players

Typical Applications

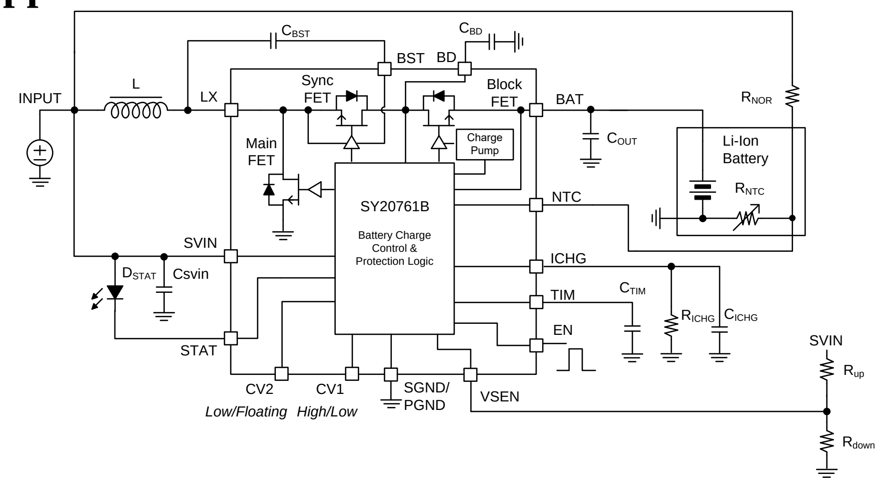
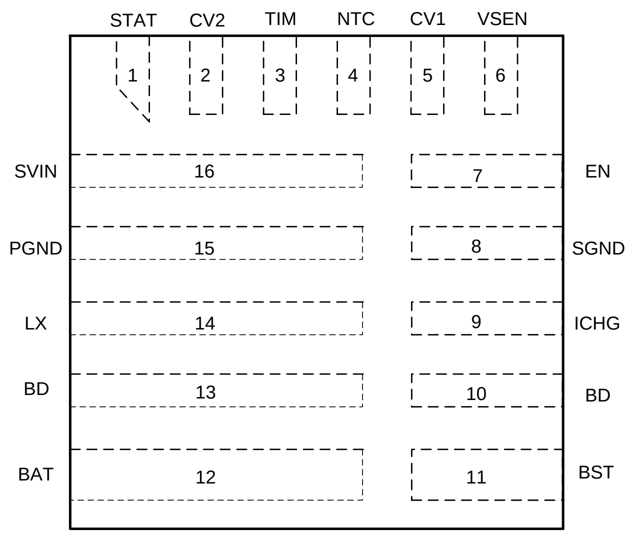


Figure1. Schematic Diagram

Pinout (top view)



(QFN3×3-16)

Top Mark: **CKU*xyz***, **(**Device code: CKU, ***x=year code, y=week code, z= lot number code*****)**

Name	Pin Number	Description
STAT	1	Charge status indication pin. It is open-drain output pin and pulled high to SVIN through a LED to indicate the charge in process. When the charge is done, the LED will be off.
CV2	2	Battery CV voltage selection pin. Program 4 different CV thresholds by setting different voltage on this pin and pin5. Floating or grounding this pin in the application. CV2 pin can't be pulled high to any bias voltage higher than 3.3V.
TIM	3	Charge time limit pin. Connect this pin to GND with a capacitor. Internal current source charges the capacitor for TC mode and CC mode's charge time limit. TC charge time limit is about 1/9 of CC charge time limit.
NTC	4	Thermal protection pin. UTP threshold is typical 75% of V_{SVIN} and OTP threshold is typical 45% of V_{SVIN}. Pull up to SVIN can disable charge logic and make the IC operate as a normal Boost regulator. Pull down to ground can shut down the IC.
CV1	5	Battery CV voltage selection pin. Program 4 different CV thresholds by setting different voltage on this pin and pin2. The detailed information is shown in description section.
VSEN	6	Voltage sense of SVIN. If the voltage drops to internal 1.195V reference voltage, the SVIN will be clamped to setting value and input current will be limited.
EN	7	Enable control pin. High logic for enable on, and low logic for enable off.
SGND	8	Signal ground pin.
ICHG	9	Charge current program pin. Connect this pin to GND with a resistor $R_{ICHG.}$ The mirror current about 1/10000 of the blocking FET current will dump into the external RC network through ICHG pin and compared to the internal reference 1V. So $I_{CC} = (1V/ R_{ICHG}) \times 10000$, $I_{TC} = (1V/ R_{ICHG}) \times 1000 + 0.02$.
BD	10, 13	Connect it to the drain of internal blocking FET. Bypass at least a 4.7µF ceramic capacitor to GND.
BST	11	Boot-strap pin. Supply rectified FET's gate driver. Connect this pin to LX with a 0.1µF ceramic capacitor.
BAT	12	Battery positive pin.
LX	14	Switch node pin. Connect it to the external inductor.
PGND	15	Power ground pin.
SVIN	16	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage range.

Absolute Maximum Ratings (Note1)

STAT, NTC, CV1, VSEN, EN, ICHG, BD, BAT, LX, SVIN -- 18V
CV2, TIM, BST-LX -- 4V
LX Pin Continuous Current --- 5A
Power Dissipation, P_D @ T_A = 25°C, QFN3×3 --- 2.6W
Package Thermal Resistance (Note2)
θ_{JA} -- 38°C/W
θ_{JC} -- 4°C/W
Junction Temperature Range --- -40°C to 125°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range -- -65°C to 125°C

Recommended Operating Conditions (Note3)

SVIN --- 3.6V to 5.5V
STAT, NTC, CV1, VSEN, EN, ICHG, BD, BAT, LX, --- -0.3V to 16V
CV2, TIM, BST-LX -- -0.3V to 3.3V
LX Pin Continuous Current --- 3.5A
Ambient Temperature Range -- -40°C to 85°C

Electrical Characteristics

T_A=25°C, V_{IN}=5V, GND=0V, C_{IN}=4.7μF, L=0.68μH, R_{ICHG}=10kΩ, C_{TIM}=470nF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{SVIN})						
Supply Voltage	V_{SVIN}		3.6		16	V
V_{SVIN} Under Voltage Lockout Threshold	V_{UVLO}	V_{SVIN} rising and measured from V_{SVIN} to GND			3.6	V
V_{SVIN} Under Voltage Lockout Hysteresis	ΔV_{UVLO}	Measured from V_{SVIN} to GND		100		mV
Input Over Voltage Protection	V_{OVP}	V_{SVIN} rising and measured from V_{SVIN} to GND	5.8			V
Input Over Voltage Protection Hysteresis	ΔV_{OVP}	Measured from V_{SVIN} to GND		0.5		V
Quiescent Current						
Battery Discharge Current	I_{BAT}	Shut down IC, EN=NTC=0			10	μA
Input Quiescent Current	I_{IN}	Disable charge, EN=1,NTC=0			1.5	mA
Oscillator and PWM						
Switching Frequency	f_{SW}			1000		kHz
Main N-FET Minimum Off Time	t_{MIN_OFF}			100		ns
Main N-FET Maximum Off Time	t_{MAX_OFF}			30		μs
Main N-FET Minimum On Time	t_{MIN_ON}			100		ns
Power MOSFET						
$R_{DS(ON)}$ of Main N-FET	R_{NFET_M}			80		mΩ
$R_{DS(ON)}$ of Rectified N-FET	R_{NFET_R}			40		mΩ
$R_{DS(ON)}$ of Blocking N-FET	R_{NFET_B}			40		mΩ
Voltage Regulation						
Battery Charge Voltage	V_{BAT_REG}	V_{CV1}>1.5V, CV2 is floating	8.159	8.2	8.241	V
		V_{CV1}<0.4V, CV2 is floating	8.358	8.4	8.442	
		V_{CV1}<0.4V, V_{CV2}<0.4V	8.458	8.5	8.542	
		V_{CV1}>1.5V, V_{CV2}<0.4V	8.657	8.7	8.743	
High Level Logic for CV1	V_{CV_H}		1.5			V
Low Level Logic for CV1,CV2	V_{CV_L}				0.4	V
Recharge Threshold refer to V_{BAT_REG}	ΔV_{RCH}		100	200	300	mV
Trickle Current Charge Mode Battery Voltage Threshold	V_{TRK}	BAT rising edge	5.4	5.6	5.8	V

Battery Connect Detection						
NTC Voltage Threshold for Battery Detect	V_{DET}	NTC falling edge	85		95	$\%V_{SVIN}$
Detect Delay Time	t_{DET}			30		ms
Charge Current						
Internal Charge Current Accuracy for Constant Current Mode		I_{CC}=1000mA	-10		10	%
Internal Charge Current Accuracy for Trickle Current Mode		I_{TC}=120mA	-50		50	%
Termination Current	I_{TERM}	I_{CC}=1000mA	50	100	150	mA
Output Voltage OVP						
Output Voltage OVP Threshold	V_{OVP}		105	110	115	$\%V_{BAT\_REG}$
Input Voltage Threshold for Adaptive Current Limit						
Voltage Reference of VSEN	V_{SEN}		1.17	1.195	1.22	V
Timer						
Trickle Current Charge Timeout	t_{TC}	C_{TIM}=330nF	0.4	0.5	0.65	hour
Constant Current Charge Timeout	t_{CC}		3.8	4.5	5.82	hour
Charge Mode Change Delay Time	t_{MC}			30		ms
Termination Delay Time	t_{TERM}			30		ms
Recharge Time Delay	t_{RCHG}			30		ms
Short Circuit Protection						
Output Short Protection Threshold	V_{SHORT}		1.70	2.00	2.30	V
Linear Charger Mode						
Battery Charger Current when the Blocking FET is in Linear Mode	I_{SC}	$V_{BAT}<V_{SHORT}$	4%	10%		I_{CC}
BD Voltage Regulation	V_{BD}	$V_{SHORT}<V_{BAT}<V_{TRK}$	5.8	6	6.2	V
Enable ON/OFF Control						
High Level Logic for Enable Control	V_{EN_H}		1.5			V
Low Level Logic for Enable Control	V_{EN_L}				0.4	V
Battery Thermal Protection NTC						
Under Temperature Protection	V_{NTC_UTP}		74	75	76	$\%V_{SVIN}$
Under Temperature Protection Hysteresis	$V_{NTC\_UTP\_HYS}$	Falling edge		1.3		$\%V_{SVIN}$
Over Temperature Protection	V_{NTC_OTP}		44	45	46	$\%V_{SVIN}$
Over Temperature Protection Hysteresis	$V_{NTC\_OTP\_HYS}$	Rising edge		1.3		$\%V_{SVIN}$
Thermal Fold-back and Thermal Shutdown						
Thermal Fold-back Threshold	T_{Fold}	Rising edge		120		ºC
Thermal Fold-back Threshold Hysteresis	T_{Fold_HYS}			20		ºC
Thermal Fold-back Ratio				0.25		I_{CC}
Thermal Shutdown Temperature	T_{SD}	Rising edge		160		ºC
Thermal Shutdown Temperature Hysteresis	T_{SD_HYS}			30		ºC

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

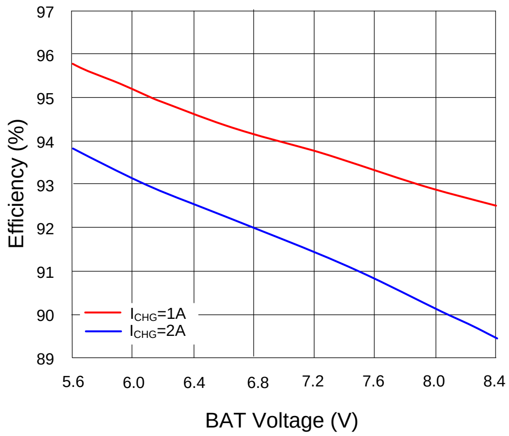
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

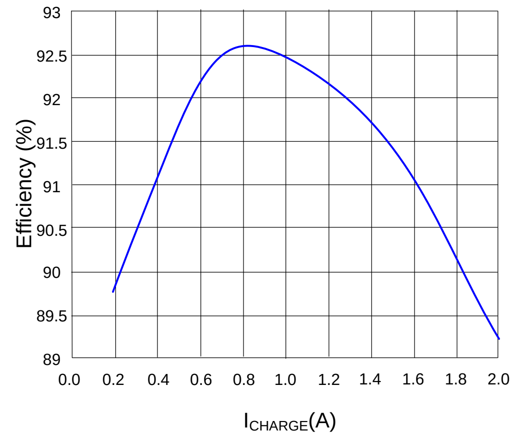
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V, R_{ICHG}=10kΩ, unless otherwise specified.)

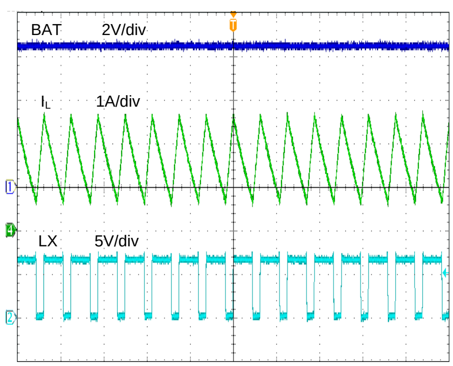
Efficiency vs. BAT Voltage (CC Mode)



Efficiency vs. Charge Current (CV Mode)

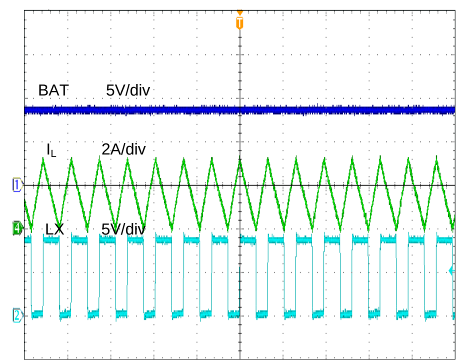


Steady Waveform (CC Mode)



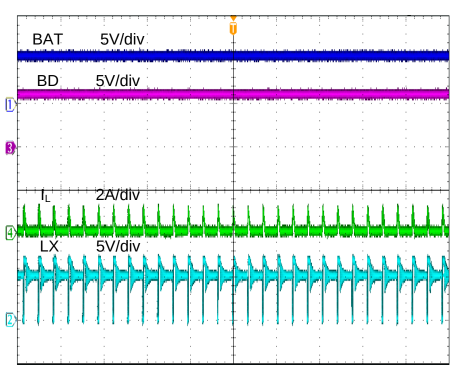
Time (2μs/div)

Steady Waveform (CV Mode)



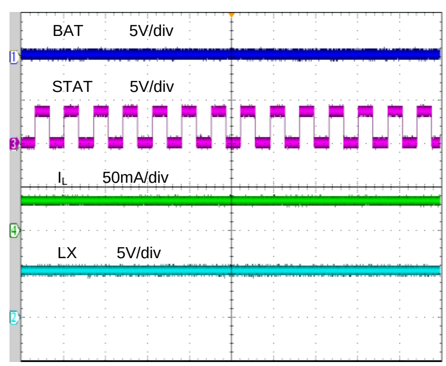
Time (2μs/div)

Steady Waveform (TC Mode)



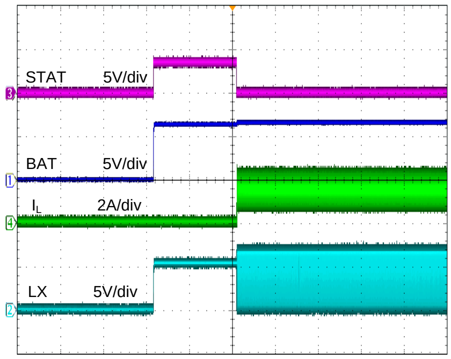
Time (10μs/div)

Steady Waveform (Short Mode)



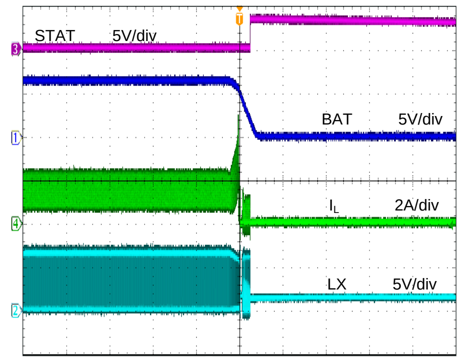
Time (1s/div)

Power ON (CC Mode)



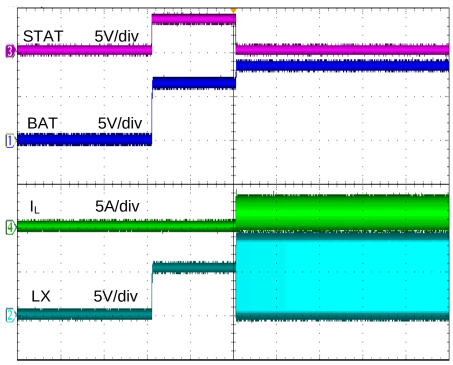
Time (400ms/div)

Power OFF (CC Mode)



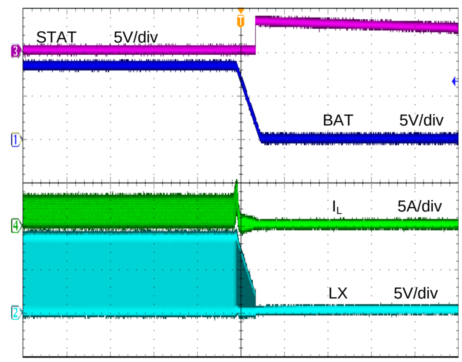
Time (2ms/div)

Power ON (CV Mode)



Time (400ms/div)

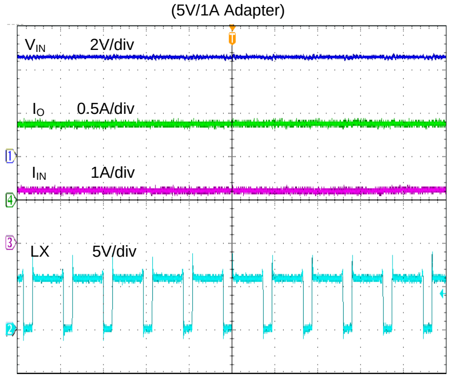
Power OFF (CV Mode)



Time (4ms/div)

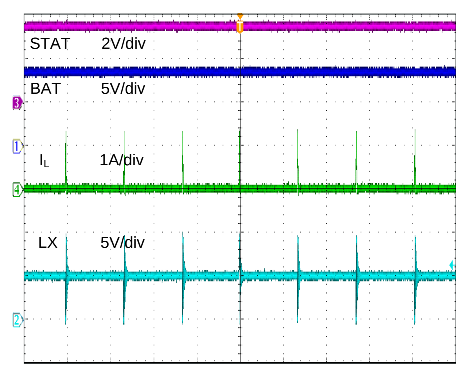
Adaptive Input Current Limit

(5V/1A Adapter)



Time (1μs/div)

Boost Mode (Null load)



Time (20μs/div)

General Function Description

The SY20761B is a synchronous Boost Li-ion battery charger for 2-cell with 3.6V-5.5V input, which integrates the power MOSFETs working with 1MHz switching frequency and the full protection functions. The charge current is up to 2A which can be programmed by using an external resistor for different portable applications. The IC can indicate the charge current information simultaneously. It also has a programmable charge timeout for safe battery charge operation and a programmable input voltage threshold for adaptive input current limit. The SY20761B can disconnect output when there is an output short circuit or shutdown. The IC consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

Charging Status Indication Description

1. Charge-in-process – Pull and keep STAT pin low;
2. Charge Done – Pull and keep STAT pin high;
3. Fault Mode – Output high and low voltage alternatively at the frequency of 1.3Hz. Connect a LED from SVIN to STAT pin, LED on means charge-in-process, LED off means charge done, LED flashing at 1.3Hz means fault mode.
   Fault Mode includes Input OVP, BAT OVP, BAT Short Circuit, NTC(UTP/OTP), Thermal Shutdown and Charge Timeout.

Switching Mode Boost Charger Basic Operation Description

Switching Mode Control Strategy

The SY20761B is a switching mode Boost charger for the applications with USB power input. The 1MHz fixed frequency is easy for the size minimization of peripheral circuit design.

Operation Principle

The SY20761B can normally work with or without Li-Ion battery.

Battery Present

When the battery is present, the SY20761B will work on trickle current charge, constant current charge and constant voltage charge mode according to the battery voltage.

Battery Absent

If there's no battery connection detected through NTC pin, SY20761B will operate as a normal switching mode Boost converter. The internal constant current loop and voltage loop are both active.

Basic Protection Principle

The SY20761B has fully battery charging protection. When the input over voltage protection, the output over voltage protection, the thermal protection or the timeout protection happens, the Boost charger will stop switching immediately. When the V_{BAT} is lower than V_{SHORT}, the short circuit protection will happen. The main FET will be turned off firstly. The block FET will enter linear mode with 1/10 of I_{CC} charging current. When V_{BAT} returns to be higher than V_{SHORT}, the Boost charger will restart to work at light load and regulate V_{BD} at 6V. The linear charge current will keep nearly 1/10 I_{CC}+0.02. When V_{BAT} returns to be higher than V_{TRK}, the Boost switching charger will take over.

Adaptive Input Current Limit Principle

The SY20761B can protect the input DC source from over load by the special loop control. The high charging current will cause a voltage drop at SVIN when the input DC source is over load. When VSEN drops below the internal 1.195V reference, SY20761B will decrease the duty cycle to reduce the charging current.

Constant Voltage Threshold Program Principle

The SY20761B can program the constant voltage threshold thru the CV1 and CV2. When V_{CV1} is higher than 1.5V and CV2 is floating, the constant voltage threshold is 8.2V; when V_{CV1} is lower than 0.4V and CV2 is floating, the constant voltage threshold is 8.4V; when V_{CV1} and V_{CV2} are lower than 0.4V both, the constant voltage threshold is 8.5V; when V_{CV1} is high than 1.5V and V_{CV2} is lower than 0.4V, the constant voltage threshold is 8.7V.

Applications Information

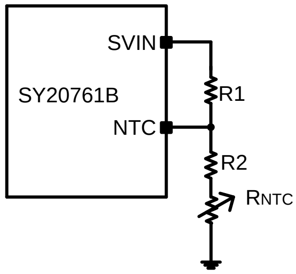
Because of the high integration of the SY20761B, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, NTC resistors R1, R2, input voltage threshold resistors R_{UP}, R_{DOWN} and timer capacitor C_{TIM} need to be selected for the target applications specifications.

NTC Resistor

The SY20761B monitors battery temperature by measuring the input voltage and NTC voltage. The controller will trigger the UTP or OTP when the rate

K (K= V_{NTC}/V_{SVIN}) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.

Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps are:

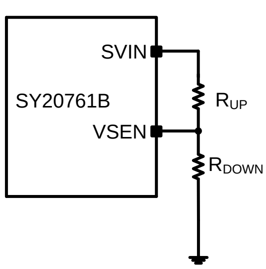
1. Define K_{UT}, K_{UT} =74~76%
2. Define K_{OT}, K_{OT} =44~46%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2,
$$R_2=\frac{K_{OT}(1\text{-}K_{UT})R_{UT}\text{-}K_{UT}(1\text{-}K_{OT})R_{OT}}{K_{UT}\text{-}K_{OT}}$$
5. Calculate R1,
$$R_1=(1/K_{OT}\text{-}1)(R_2+R_{OT})$$

If choose the typical values K_{UT}=75% and K_{OT}=45%, then

$$R_2=0.375R_{UT}\text{-}1.375R_{OT}$$
$$R_1=1.222(R_2+R_{OT})$$

Input Voltage Threshold for Adaptive Current Limit

The SY20761B will monitor input voltage by measuring the VSEN voltage, when VSEN drops below the internal 1.195V reference, SY20761B will decrease the duty cycle to reduce the charging current. The input voltage sense network shows below, choose R_{UP}, R_{DOWN} to set the input voltage threshold V_{INT}:



$$V_{INT}=\frac{V_{SEN}\times(R_{DOWN}+R_{UP})}{R_{DOWN}} \qquad \text{unit: V}$$

V_{SEN} is 1.195V.

Timer Capacitor C_{TIM}

The charger also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is given by the formula:

$C_{TIM}=2\times10^{-11}S\times t_{CC}$ unit: F

t_{CC} is the target constant charge time, unit: s.

Input Capacitor C_{IN}

The ripple current through input capacitor is greater than

$$I_{C_{IN}\_RMS}=\frac{V_{IN}\times(V_{OUT}\text{-}V_{IN})}{2\sqrt{3}\times L\times F_{SW}\times V_{OUT}}$$

X5R or X7R ceramic capacitors with greater than 4.7µF capacitance are recommended to handle this ripple current.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. This ripple voltage is related to the capacitance and its equivalent series resistance (ESR). For the best performance, it is recommended to use X5R or a better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required capacitance can be calculated as:

$$C_{OUT}=\frac{I_{CC}\times(V_{OUT}-V_{IN})}{F_{SW}\times V_{OUT}\times V_{RIPPLE}}$$

V_{RIPPLE} is the peak to peak output ripple, I_{CC} is the setting charge current.

For the SY20761B, output capacitor is paralleled by C_{BD} and C_{BAT}, for smaller output ripple noise, each capacitor with greater than 10µF capacitance is recommended.

Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:
$$L=\left(\frac{V_{IN}}{V_{OUT}}\right)^2\frac{(V_{OUT}-V_{IN})}{I_{CC}\times F_{SW}\times 40\%}$$
Where F_{SW} is the switching frequency and I_{CC} is the setting charge current.
The SY20761B is quite tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{CC} + \left(\frac{V_{IN}}{V_{OUT}}\right) \times \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good overall efficiency.

Layout Design

The layout design of the SY20761B regulator is relatively simple. For the best efficiency and to minimize noise problems, we should place the following components close to the IC: C_{SVIN}, L, C_{BD}.

1) The loop of main MOSFET, rectifier diode, and C_{BD} must be as short as possible
2) It is desirable to maximize the PCB copper area connected to GND pin to achieve the best thermal and noise performance.
3) C_{SVIN} must be close to pin SVIN and GND.
4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
5) The small signal components R_{ICHG}, R_{UP} and R_{DOWN} must be placed close to the IC and must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

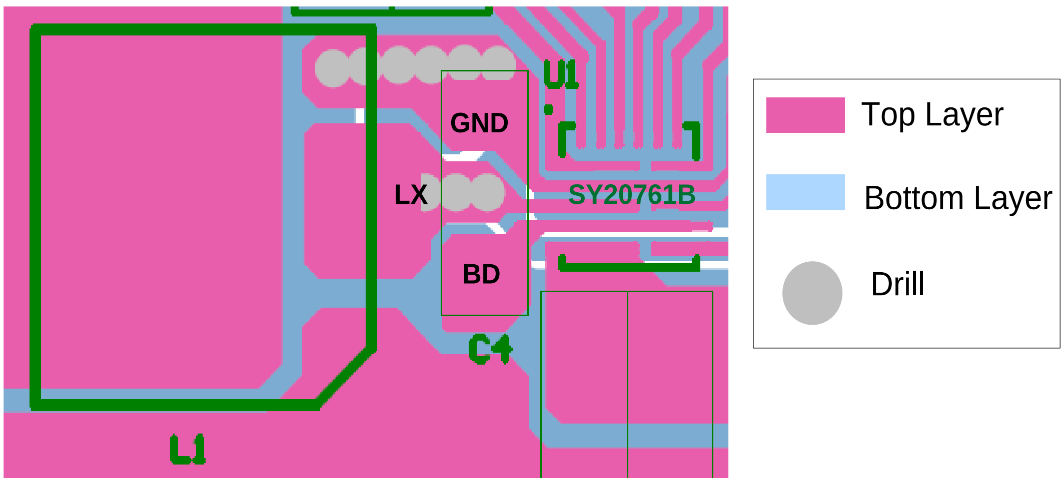
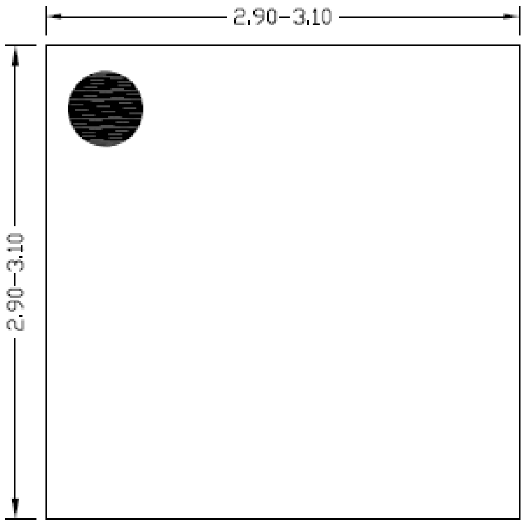
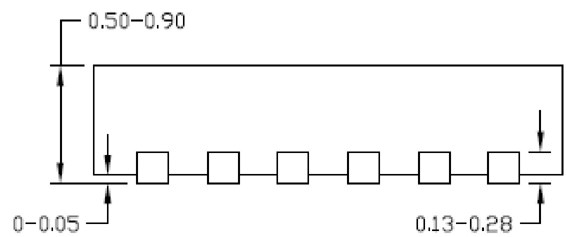


Figure2. PCB Layout Suggestion

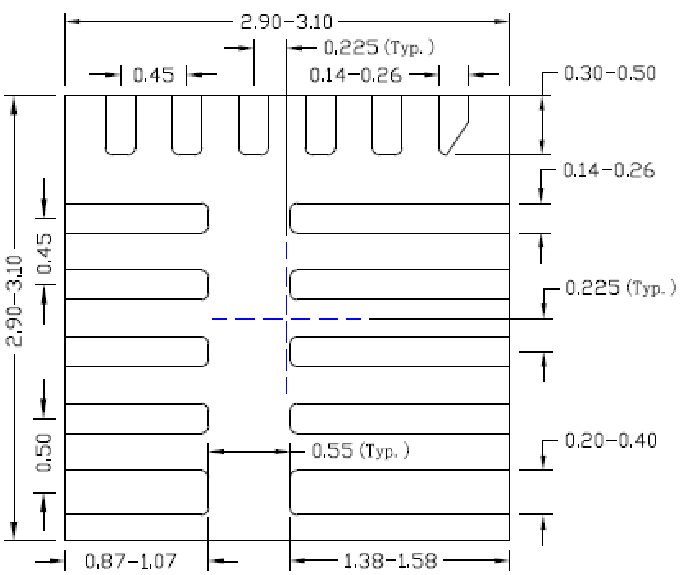
QFN3×3-16 Package Outline Drawing



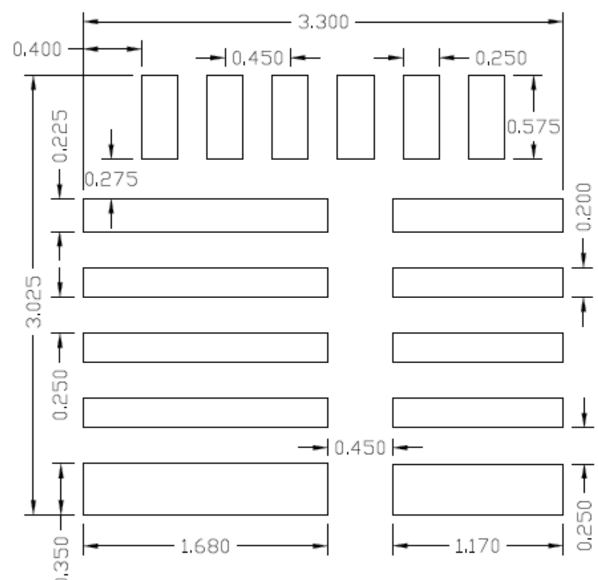
Top View



Side View



Bottom View



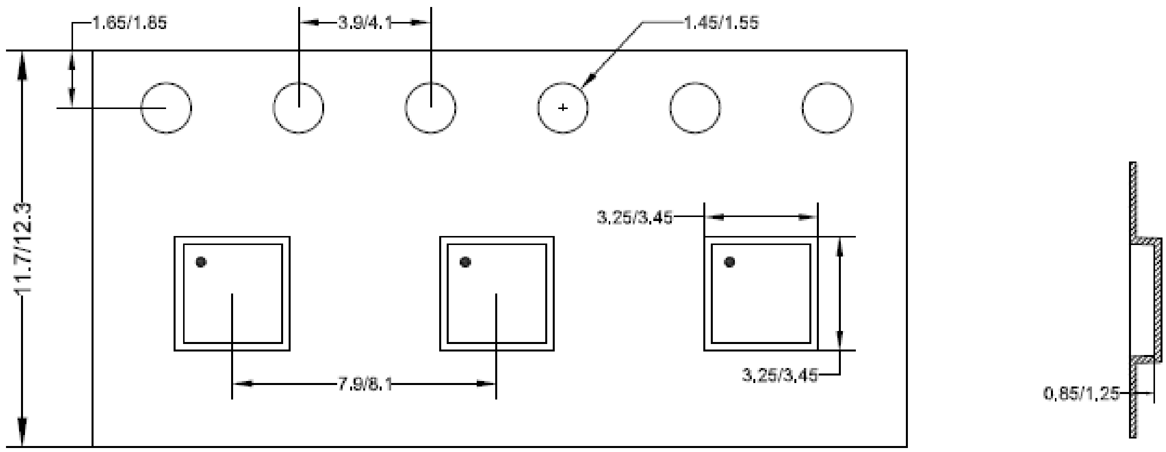
Recommended PCB layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

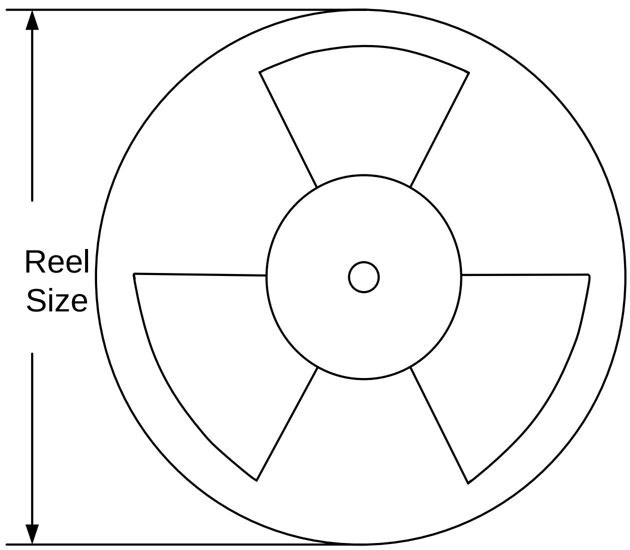
1. Taping orientation

QFN3×3



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA

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