SY21612C

High-Efficiency, 38V Maximum Input Single-Inductor Synchronous Step-Up/Down Regulator

General Description

The SY21612C high-voltage synchronous buck-boost converter operates over a wide input voltage range from 4V to 28V with 10A maximum average inductor current capability. The four integrated low-$R_{DS(ON)}$ switches minimize conduction loss.

The SY21612C offers protection against multiple conditions, including short-circuit, overcurrent, overvoltage, and overtemperature.

The SY21612C is highly integrated, so only the input and output capacitors, inductor, and feedback resistors need to be selected for the targeted application specifications.

The SY21612C is available in a compact QFN4×4-32 package.

Features

- 4V to 28V Operating Input Voltage Range
- 38V Absolute Maximum Input Voltage
- Low $R_{DS(ON)}$ for Internal Switches: 25mΩ
- 250kHz/500kHz Selectable Switching Frequency
- Soft-Start Inrush Current limit
- Hiccup Mode for Output Overcurrent, Short-Circuit and Overvoltage Protection
- Thermal Shutdown with Auto-Recovery
- 6A/10A Selectable Average Inductor Current Limit
- 1.0V±1.5% Reference Voltage Accuracy
- Resistor Programmable Output Current Limit
- RoHS-Compliant and Halogen-Free
- Compact Package: QFN4×4-32

Applications

- Docking Station
- Laptop
- High-End Power Bank
- Monitor
- Car Charger
- USB PD

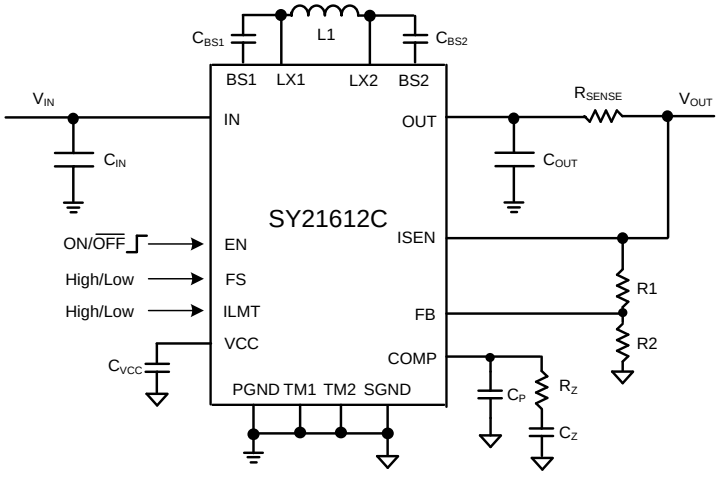


Figure1. Typical Application Circuit

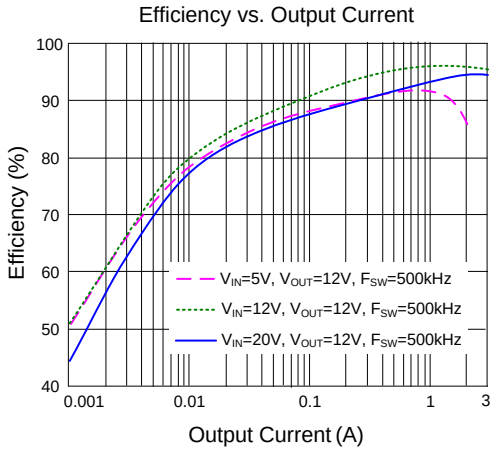


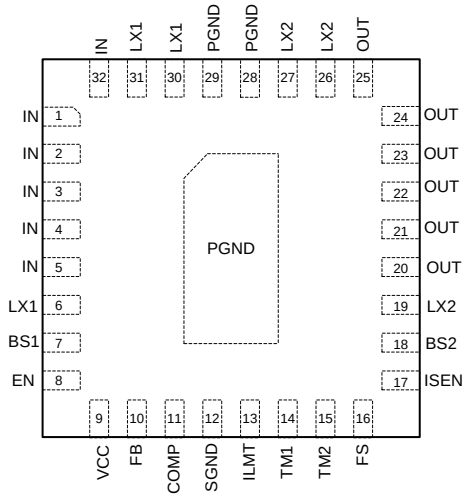
Figure2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21612CQFC	QFN4×4-32 RoHS Compliant and Halogen Free	**BXX*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin Name	Pin Number	Description
IN	1, 2, 3, 4, 5, 32	Power input pin. Decouple from PGND with at least a 10μF ceramic capacitor.
LX1	6, 30, 31	Switching node 1
BS1	7	Bootstrap pin. Supply high-side gate driver. Connect a 0.1μF ceramic capacitor between the BS1 and the LX1 pin. Do not connect a resistor in series with the capacitor.
EN	8	IC enable control pin. Logic-high enable. This pin is internally pulled high by a 400nA current source.
V_{CC}	9	3.3V Internal LDO output. Power supply for internal driver and control circuits. Decouple to SGND with a minimum 2.2μF ceramic capacitor.
FB	10	Output feedback pin. Connect this pin to the center point of the output resistor-divider to program the output voltage: $V_{OUT} = 1V \times (R_1 + R_2) / R_2$
COMP	11	Compensation pin. Connect the RC network between this pin and ground.
SGND	12	Signal ground
I_{LMT}	13	Average inductor current limit threshold select pin. Connect this pin to VCC for a 10A threshold, or to SGND for a 6A threshold.
TM1	14	Test pin. For factory use only. Connect to SGND.
TM2	15	Test pin. For factory use only. Connect to SGND.
FS	16	Switching frequency select pin. Connect this pin to V_{CC} for 500kHz switching frequency, or to SGND for 250kHz switching frequency.
I_{SEN}	17	Current-sense pin. Connect resistor R_{SENSE} between OUT and ISEN to set the output current limit threshold. $I_{OUT,LMT} = 30m/R_{SENSE}$.
BS2	18	Bootstrap pin. Supply high-side gate driver. Connect a 0.1μF ceramic capacitor between the BS2 and the LX2 pins. Do not connect a resistor in series with the capacitor.
LX2	19, 26, 27	Switching node 2
PGND	28, 29, Exposed Pad	Power ground
OUT	20, 21, 22, 23, 24, 25	Power output pin. Decouple to PGND with at least a 10μF ceramic capacitor.

Block Diagram

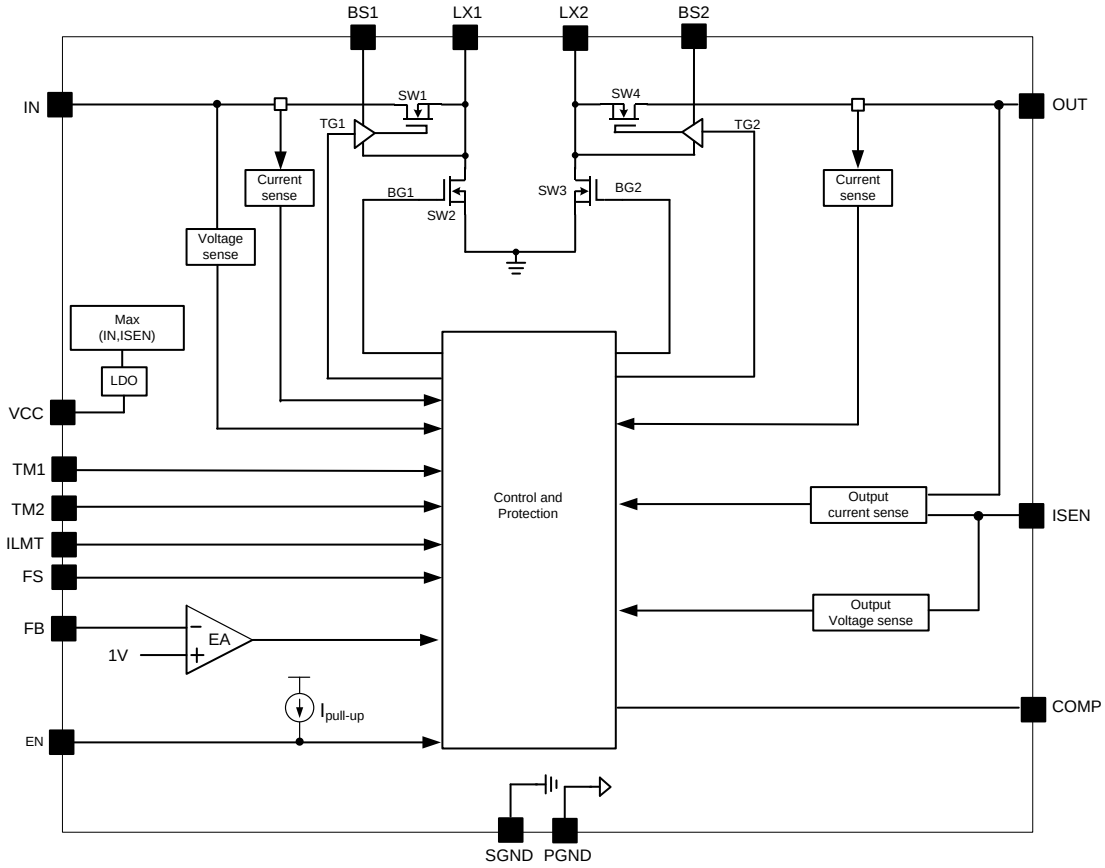


Figure 3. Block Diagram

Absolute Maximum Ratings

Absolute Maximum Ratings (1)	Min	Max	Unit
IN, LX1, LX2, OUT, I_{SEN}, EN, FB, COMP	-0.3	38	V
BS-LX, V_{CC}, FS, I_{LMT}	-0.3	4	
LX, 50ns Duration	-5	31	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information (2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		28	°C/W
θ_{JC} Junction-to-case Thermal Resistance		2.8	
P_D Power Dissipation T_A = 25°C		4	W

Recommended Operating Conditions (3)	Min	Max	Unit
IN	4	28	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 12V, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		28	V
Input UVLO Threshold	$V_{IN,UVLO}$		2.9		3.5	V
UVLO Hysteresis	$V_{UVLO,HYS}$			0.2		V
V_{CC} LDO Voltage	V_{CC}	I_{LDO} = 10mA	3.09	3.26	3.44	V
Quiescent Current	I_Q	EN = high, no switching			300	μA
Shutdown Current	I_{SD}	EN = low			11.5	μA
Feedback Reference Voltage	V_{REF}		0.985	1	1.015	V
FB Input Current	I_{FB}		-50		50	nA
Output OVP Threshold	$V_{FB,OVP}$	FB voltage rising		120		% V_{REF}
Output OVP Delay Time	$t_{OVP,DLY}$			10		μs
Output UVP Threshold	$V_{FB,UVP}$	FB voltage falling		50		% V_{REF}
Output UVP Delay Time	$t_{UVP,DLY}$			200		μs
Internal Power MOSFET $R_{DS(ON)}$	$R_{DS(ON)}$			25		mΩ
Inductor Average Current Limit	I_{AVG}	I_{LMT} connected to SGND		6		A
		I_{LMT} connected to V_{CC}		10		A
Inductor Peak Current Limit	I_{PK}	I_{LMT} connected to SGND	6.4	8.4	10.5	A
		I_{LMT} connected to V_{CC}	9.2	13	16.5	A
EN Input Logic High	V_{ENH}		1.5			V
EN Input Logic Low	V_{ENL}				0.5	V
Output Current-Limit Voltage Threshold	$V_{IOUT,LIM}$		33	37	41	mV
Oscillator Frequency	f_{OSC}	FS connected to V_{CC}	425	500	575	kHz
		FS connected to GND	190	250	320	kHz
Minimum ON Time	t_{ON_MIN}			150		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Soft-Start Time	t_{ss}			1.5		ms

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

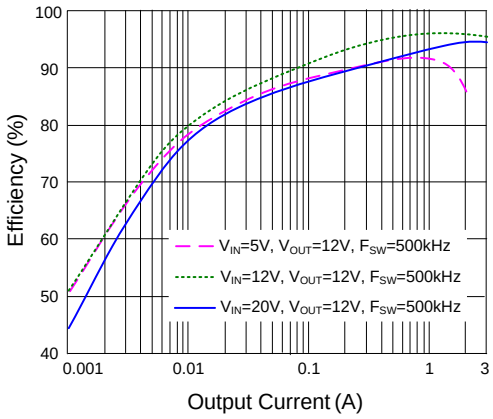
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

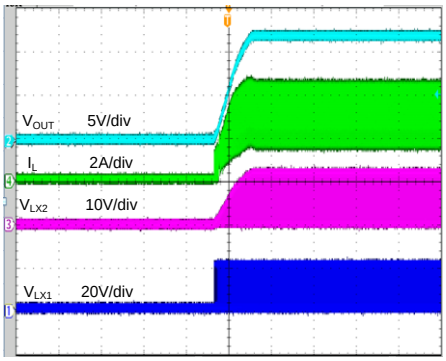
(T_A= 25℃, V_{OUT} = 12V, f_{SW}=500kHz, L = 3.3μH, C_{OUT}= 30μF, unless otherwise specified.)

Efficiency vs. Output Current



Regulator Enable

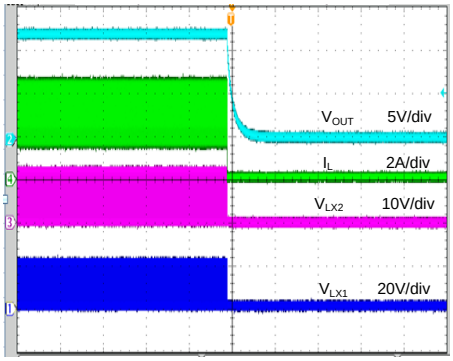
(V_{IN}=20V,V_{OUT}=12V,R_{LOAD}=4Ω)



Time (2ms/div)

Regulator Disable

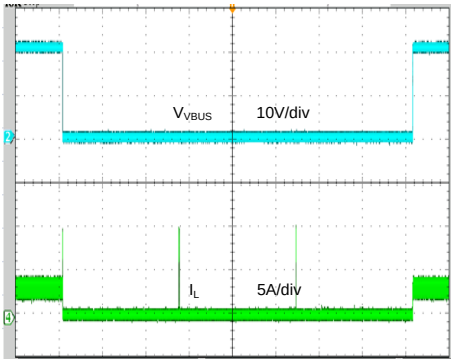
(V_{IN}=20V,V_{OUT}=12V,R_{LOAD}=4Ω)



Time (2ms/div)

Short Circuit Test

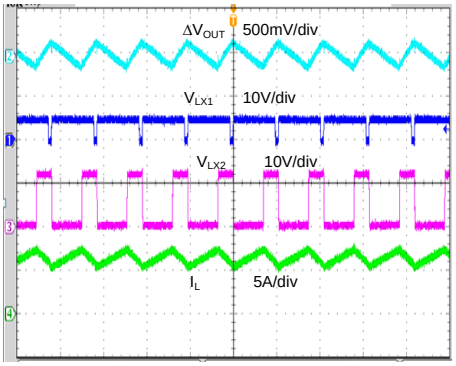
(V_{IN}=20V,V_{OUT}=20V,R_{LOAD}=6.7Ω)



Time (1s/div)

Output Ripple

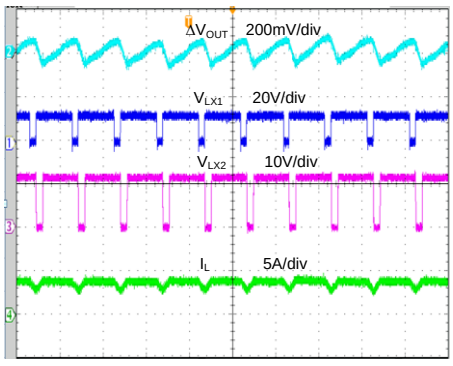
(V_{IN}=5V,V_{OUT}=12V,I_{LOAD}=2A)



Time (2μs/div)

Output Ripple

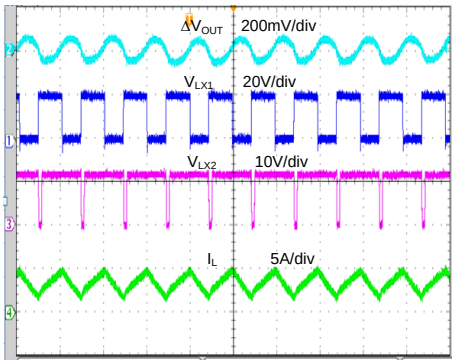
(V_{IN}=12V,V_{OUT}=12V,I_{LOAD}=3A)



Time (2μs/div)

Output Ripple

(V_{IN}=20V,V_{OUT}=12V,I_{LOAD}=3A)



Time (2μs/div)

Operation

The SY21612C high-voltage synchronous buck-boost converter operates over a wide input voltage range from 4V to 28V with a 10A maximum average inductor current capability. The four integrated low-$R_{DS(ON)}$ switches minimize conduction loss.

The SY21612C offers protection against multiple conditions, including short-circuit, overcurrent, overvoltage, and overtemperature.

The SY21612C is highly integrated, so only the input and output capacitors, inductor, and feedback resistors need to be selected for the targeted application specifications.

The SY21612C is available in a compact QFN4×4-32 package.

Application Information

Input Undervoltage Lockout

The SY21612C incorporates input undervoltage lockout (UVLO) protection to prevent operation before all internal circuitry is ready, and to ensure that the power and synchronous rectifier switches are properly biased. The device remains in a low-current state and all switching is inhibited until V_{IN} exceeds the input UVLO (rising) threshold. At that time, if EN is enabled, the IC will start up by initiating a soft-start ramp. If V_{IN} falls below the input UVLO (falling) threshold, switching will be suppressed again.

Enable Control

The EN input is a high-voltage-capable input with logic-compatible threshold. When EN is driven above 1.5V normal device operation is enabled. When driven below 0.5V, the device will be shut down, reducing input current to less than 11.5μA. EN is internally pulled high by using a 400nA current source. In applications where EN is pulled high to the power input V_{IN}, a 10kΩ to 100kΩ resistor should be added between the power input and EN.

Soft-Start

The SY21612C incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1.5ms, which avoids high current flow and transients during startup.

External Bootstrap Capacitor Connection

The SY21612C integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 100nF low-ESR ceramic capacitor connected between BS1 and LX1, as shown in Figure 4, and another one between BS2 and LX2. The bootstrap capacitors provide the gate-driver supply voltage for the high-side N-channel power MOSFET switches.

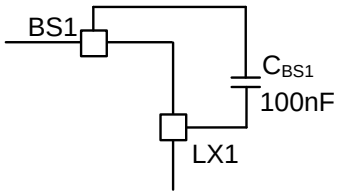


Figure 4. External Bootstrap Capacitor Connection

V_{CC} Linear Regulator

An internal linear regulator (V_{CC}) produces a 3.3V supply from V_{IN}, which powers the internal gate drivers, PWM logic, analog circuit and other blocks. Connect a 2.2μF low-ESR ceramic capacitor from V_{CC} to SGND, as shown in Figure 5.

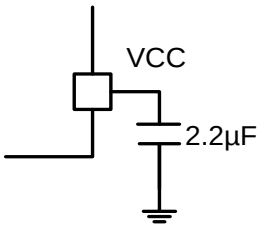


Figure 5. V_{CC} Regulator

Fault-Protection Modes

Average Inductor Current Limit

The SY21612C incorporates an average inductor current limit. When the average inductor current is greater than the threshold, the internal control loop will regulate the average inductor current by decreasing the duty cycle. The device resumes normal operation when the fault condition is removed. The average inductor current limit threshold is selectable by pulling the I_{LMT} pin low or to V_{CC}.

Peak Inductor Current Limit

The SY21612C also incorporates a cycle-by-cycle peak current limit. The inductor current is measured in SW1 when it is on. If the current exceeds the current limit, both SW1 and SW3 turn off, and SW2 and SW4 turn on. Select the peak-current-limit threshold by pulling the I_{LMT} pin low or to V_{CC}.

Short-Circuit Protection

If V_{OUT} is less than approximately 50% of the setpoint and the device is at the current limit (average or peak inductor current) continuously for approximately 200μs, the short-circuit protection mode will be initiated, and the device will shut down for approximately 2.6s. The device will then restart with a complete soft-start cycle. If the short-circuit condition remains, then the hiccup cycle of shutdown and restart will continue indefinitely unless the UVP threshold is reached. See Figure 6.

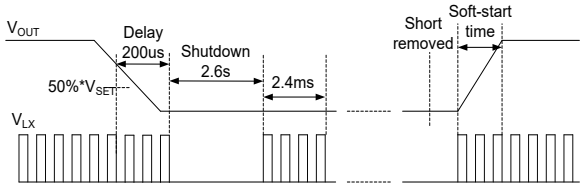


Figure 6. Short-Circuit Protection

Output Overvoltage Protection (OVP)

The SY21612C includes output overvoltage protection (OVP). If the output voltage exceeds the feedback regulation level, SW1 and SW3 turn off and the synchronous rectifier turns on. If the output voltage remains high, SW2 and SW4 remain on until the inductor current reaches zero. If the output voltage continues to rise and exceeds the output overvoltage threshold for more than 10μs, then output overvoltage protection mode is triggered. The SY21612C resumes regulation once the overvoltage condition is removed.

Overtemperature Protection (OTP)

The SY21612C includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the operation when the junction temperature exceeds 150°C. Once the junction temperature decreases by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Output Current Limit

The SY21612C provides a function for limiting output current by sensing the voltage drop between the OUT pin and the I_{SEN} pin (as shown in Figure 7). When the differential voltage on R_{SENSE} exceeds the voltage threshold, the internal current-control loop will regulate the output current by decreasing the duty cycle until UVP or OTP is triggered. Considering the effects of R_{PIN} and R_{WIRE}, the actual current limit I_{LIMIT} can be calculated as shown in Equation 1:

$$I_{LIMIT} = \frac{V_{OUT} - V_{ISEN}}{R_{SENSE} + R_{PIN} + R_{WRIE}} \quad (1)$$

where $R_{PIN} \approx 1.65m\Omega$.

R_{WIRE} depends on PCB layout.

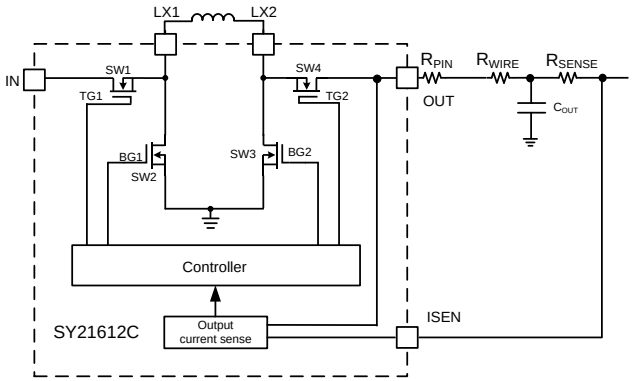


Figure 7. Output Current Limit

Feedback Resistor Selection

Choose R1 and R2 to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. A value of between 10kΩ and 100kΩ is highly recommended for both resistors. The output voltage V_{OUT} is programmed by an external voltage divider with the 1V internal voltage reference as given in Equation 2:

$$V_{OUT} = 1V \times \frac{R_1 + R_2}{R_2} \quad (2)$$

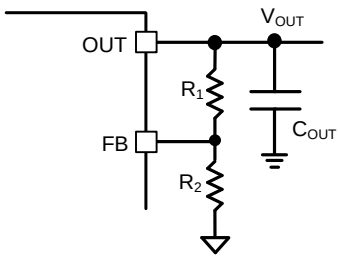


Figure 8. V_{OUT} Programming

Input Capacitor C_{IN}

In buck mode, the input capacitor supplies high ripple current. For the best performance, select a typical X5R or better grade ceramic capacitor with a 10V rating, and at least 22μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by CIN and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)} \qquad (3)$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2} \qquad (4)$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D) \qquad (5)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}} \qquad (6)$$

The capacitance value is less important than the RMS current rating. A single 22μF X5R capacitor is sufficient in most applications.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use an X5R or better grade ceramic capacitor with a 16V rating, and capacitance of at least 30μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor-current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR \qquad (7)$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} \qquad (8)$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Inductor Selection

For the buck-boost converter, the inductor must support buck applications with the maximum input voltage and boost applications with the minimum input voltage. The critical inductance values for buck mode are calculated with Equation 9:

$$L_{BUCK} = \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times \Delta I_L} \qquad (9)$$

where ΔI_L is the peak-to-peak inductor ripple current, and it is approximately 30% to 50% of the maximum output current.

The critical inductance for boost mode is calculated with Equation 10 and Equation 11:

$$L_{BOOST} = \frac{V_{IN,MIN} \times (V_{OUT} - V_{IN,MIN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \qquad (10)$$

$$I_{IN,MAX} = \frac{V_{OUT} \times I_{OUT}}{V_{IN,MIN} \times \eta} \qquad (11)$$

where η is the efficiency, and ΔI_L is the peak-to-peak inductor ripple current, which is about 30% to 50% of the maximum input current ($I_{IN,MAX}$). The recommended minimum inductor

values are either L_{BUCK} or L_{BOOST}, whichever is higher.

In addition to the inductance value, the inductor must support the peak current based on Equation (12) and Equation (13) to avoid saturation:

$$I_{PEAK\text{-}BUCK} = I_{OUT} + \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L} \quad (12)$$

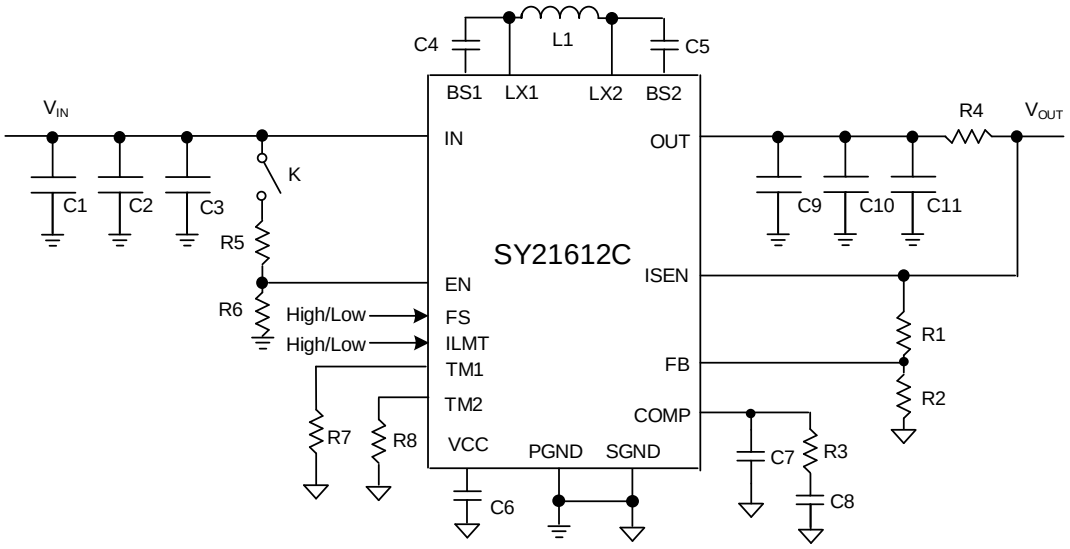
$$I_{PEAK\text{-}BOOST} = \frac{V_{OUT} \times I_{OUT}}{V_{IN,MIN} \times \eta} + \frac{V_{IN,MIN} \times (V_{OUT} - V_{IN,MIN})}{2 \times V_{OUT} \times f_{SW} \times L} \quad (13)$$

Choosing a larger inductance reduces the ripple current, but also increases the size of the inductor and reduces the achievable bandwidth of the converter by moving the right-half-plane zero to a lower frequency. The appropriate balance should be chosen based on the application requirements.

Loop Compensation

The SY21612C incorporates an average-current-mode control strategy. The average-current-mode control strategy has two feedback loops. The inner loop is the voltage loop, with compensation components that are adjusted automatically with the frequency setting. The outer loop is the current loop, which is compensated with external components. A fixed compensation network is recommended for stability, as follows: a 10kΩ resistor and 2.2nF capacitor in series between COMP and SGND, and a 4.7–10pF capacitor in parallel.

Typical Design



Design Specifications

Input Voltage (V)	Output Voltage (V)	Maximum Output Current (A)
4–28	5–20	3

BOM List

Designator	Description	Part Number	Manufacturer
U1		SY21612CQFC	Silergy
C1, C2, C3, C9, C10, C11	10μF/50V/X5R, 1206	C3216X5R1H106K	TDK
C4,C5	0.1μF/50V/X7R, 0603	C1608X7R1H104K	TDK
C6	2.2μF/16V/X5R, 0603	C1608X5R0J225K	TDK
C7	10pF/50V/C0G, 0603	C1608C0G1H100J	TDK
C8	2.2nF/50V/C0G, 0603	C1608C0G1H222J	TDK
R1	110kΩ, 1%, 0603		
R2, R3, R5	10kΩ, 1%, 0603		
R4	0.01Ω, 1%, 1206		
R6	1MΩ, 1%, 0603		
R7, R8	0Ω, 1%, 0603		
L1	3.3μH	PCMB104T3R3MS	

Recommend Table for Typical Applications

V_{OUT} (V)	fsw (Hz)	L	C_{OUT}
5	500k	2.2μH	3×22μF/50V, 1206, X5R
12	500k	3.3μH	3×22μF/50V, 1206, X5R
12	250k	4.7μH	3×22μF/50V, 1206, X5R
20	250k	6.8μH	3×22μF/50V, 1206, X5R

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- For minimum noise and maximum efficiency, place the following components close to the IC: C_{IN}, L, R1, and R2.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Place reasonable vias underneath the ground pad to enhance the thermal performance.
- C_{IN} must be close to pins IN and GND. Minimize the loop area formed by C_{IN}, IN, and GND.
- C_{OUT} must be close to pins OUT and GND. Minimize the loop area formed by C_{OUT}, OUT, and GND.
- The BS pin is sensitive. The bootstrap capacitors must be placed between, and as close as possible to, BS and LX.
- To prevent the circulating currents in the ground plane from disrupting operation of the regulator, all small-signal grounds should return to GND by a different route. This primarily concerns the ground connection for the FB pin resistor and the feedback network in sink mode.
- If the IN pin is connected directly to a power source such as a Li-ion battery, and the system chip that interfaces with the EN pin has a high impedance state during shutdown mode, add a 1MΩ pulldown resistor between the GND and EN pins to prevent noise from falsely triggering the regulator during shutdown mode.

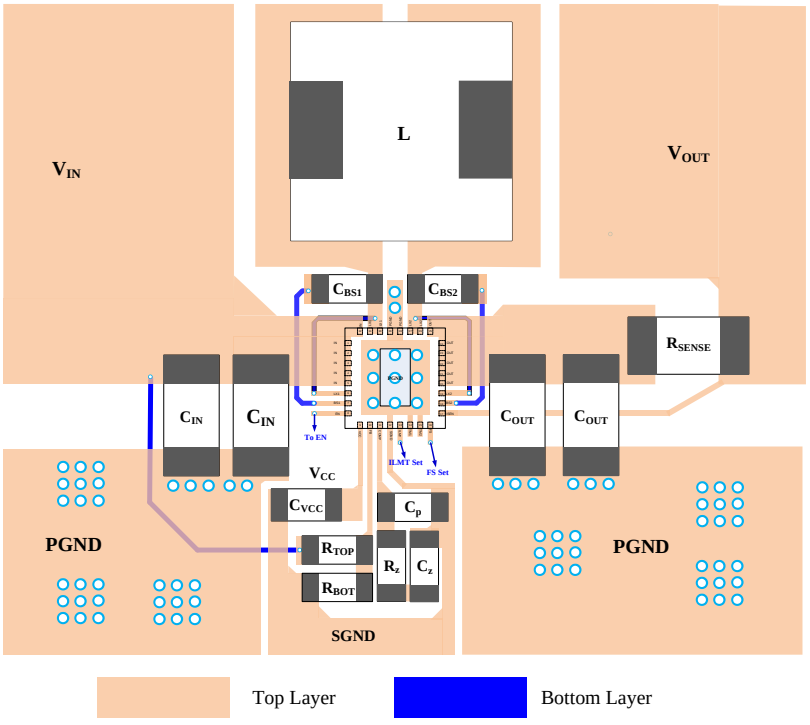
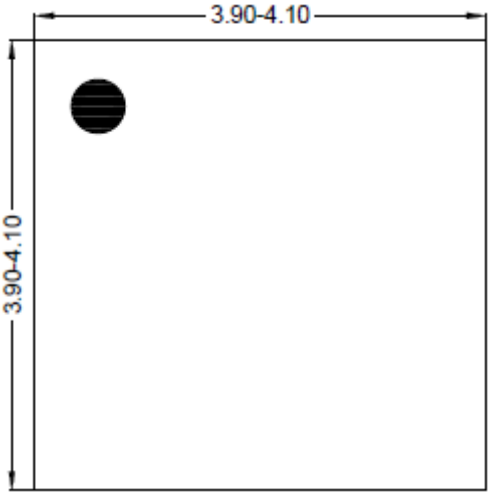
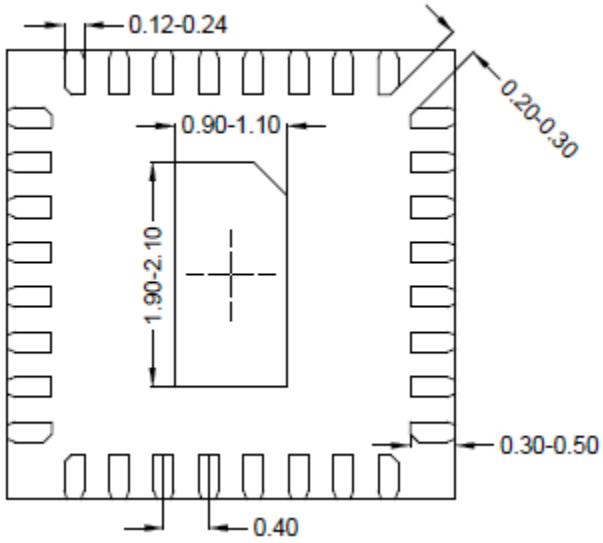


Figure 9. Recommended PCB Layout

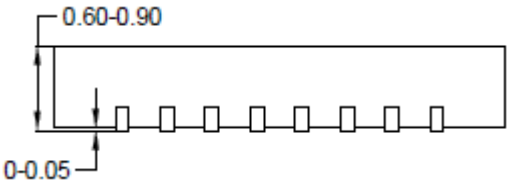
QFN4×4-32 Package Outline and PCB Layout Design



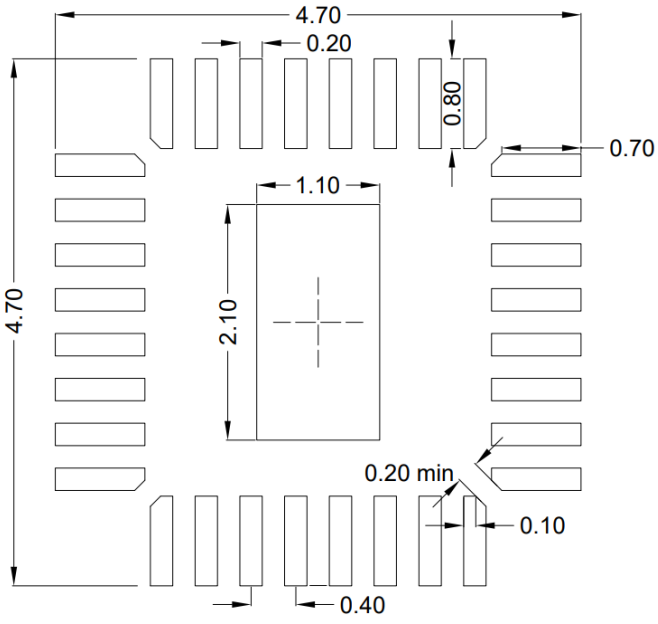
Top view



Bottom view



Side view

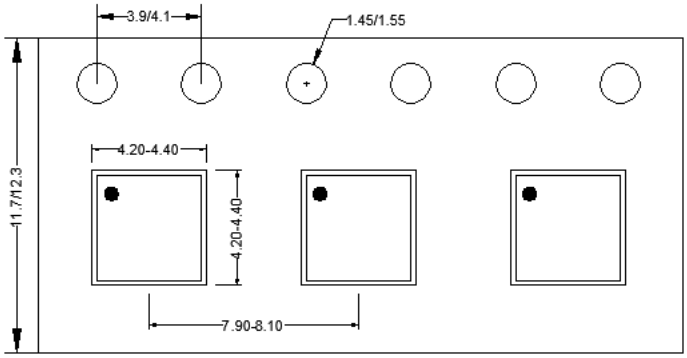


Recommended PCB layout
(reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

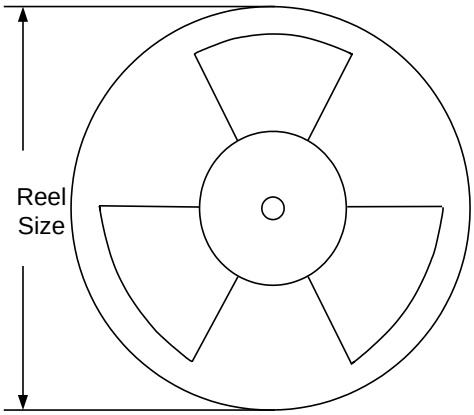
Taping and Reel Specification

QFN4×4 taping orientation



Feeding direction ⟶

Carrier tape and reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN4×4	12	8	13"	400	400	5000

Others: N/A

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
June 13, 2025	Revision 1.0A	Add the following description to the BS1 pin description and the BS2 pin description (Page2): ---- Do not connect a resistor in series with the capacitor.
Mar.24, 2023	Revision 1.0	Language improvements for clarity.
May.6, 2020	Revision 0.9C	Update the Recommended PCB layout in the page9
Nov.19, 2018	Revision 0.9B	Update in Features: 1: change “4V to 28V Input Voltage Range” to “ 4V to 28V **Operating** Input Voltage Range”; 2: Add “38V Absolute Maximum Input Voltage” in Feature. Change “28V Input” to “38V Maximum Input” in the header.
Oct. 24, 2018	Revision 0.9A	change the Absolute Maximum Rating of IN, LX1, LX2, OUT, ISEN, EN, FB, COMP from “-0.3V to 30V” to “-0.3V to 38V”
July 10, 2018	Revision 0.9	Initial Release

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