

General Description

The SY20704 is a high input voltage, low-ground current, low-dropout voltage regulator capable of sourcing 150mA with only 300mV of dropout. The SY20704 wide input-voltage range supports operation as low as 2.3V and up to 30V. It provides a resistor programmable output voltage with $\pm 2\%$ accuracy over temperature.

The SY20704 provides protection features including logic enable control, thermal shutdown, current limit, and reverse leakage current protection for reliable operation. Its internal compensation enables stable operation using low ESR ceramic capacitors. The device also provides reverse input voltage protection up to -20V Abs. Max.

The device is suitable for use in multiple consumer and industrial applications.

The SY20704 is available in SOT23-5 or DFN 2mm $\times$ 2mm-6pin packages.

Features

- Input Voltage Range: 2.3V to 30V
- Low Dropout Voltage (300mV @ 150mA)
- 150mA Output Current Capability
- Low Ground Current
- Ultra-Low Shutdown Current
- High Output Accuracy of $\pm 2\%$ Over Operating Temperature Range
- Stable with Small Ceramic Capacitors
- Excellent Load and Line Regulation
- Reverse Leakage Current Protection
- Reverse Input Voltage Protection
- TTL Logic Enable Input
- Thermal Shutdown
- Compact SOT23-5 or DFN2 $\times$ 2-6 Packages
- RoHS Compliant and Halogen Free

Applications

- Battery-Powered Applications
- Consumer and Portable Products
- Notebooks
- Smartphones
- SMPS Post-Regulator/ DC-DC Modules

Typical Applications

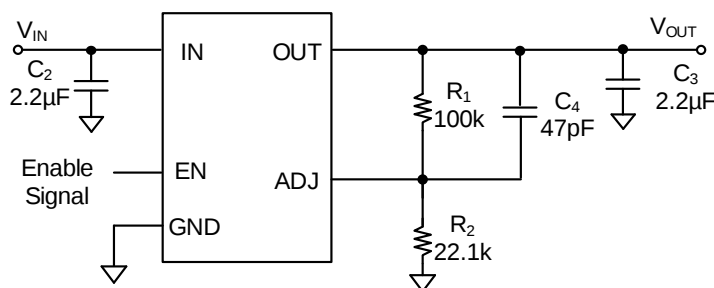


Figure 1. Schematic Diagram

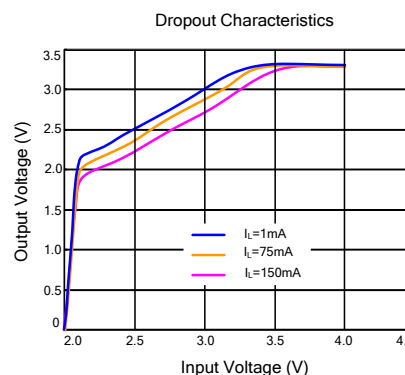


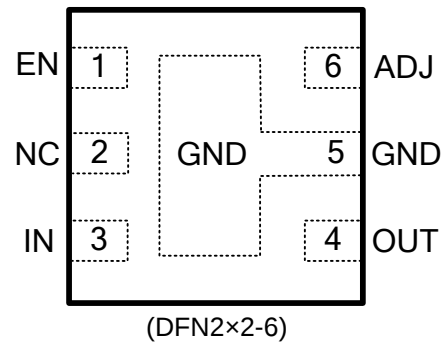
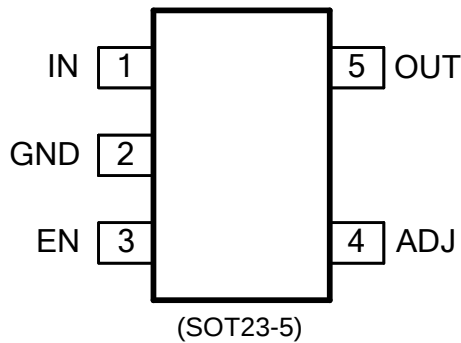
Figure 2. Dropout Characteristics

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20704AAC	SOT23-5 RoHS Compliant and Halogen Free	JNxyz
SY20704DEC	DFN2×2-6 RoHS Compliant and Halogen Free	PExyz

x=year code, y=week code, z= lot number code

Pinout (top view)

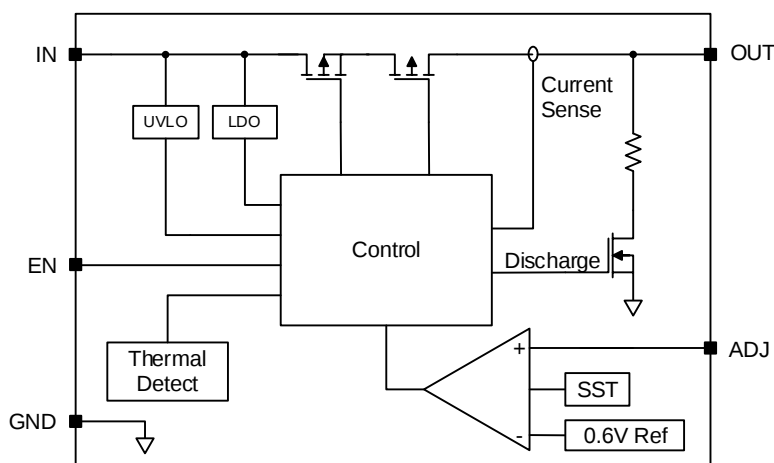


Pin Description

Pin Name	SOT23-5	DFN2×2-6	Pin Description
IN	1	3	Supply input pin.
GND	2	5	Ground pin.
OUT	5	4	LDO output pin.
EN	3	1	Enable pin. A low level placed the part in shutdown. A high level enables operation. Do not leave floating.
ADJ	4	6	Output voltage configuration pin. The output voltage can be set using a resistor divider: $V_o = 0.6 \times (1 + \frac{R1}{R2})$



Block Diagram



Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN	-20	36	V
OUT		V _{IN} +0.3	
EN	-0.3	V _{IN} +0.3	
ADJ	0	3.6	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance (SOT23-5/ DFN2×2-6)	100/62	°C/W
θ_{JC} Junction-to-case Thermal Resistance (SOT23-5/ DFN2×2-6)	25/8.5	
P_D Power Dissipation $T_A = 25^\circ\text{C}$ (SOT23-5/ DFN2×2-6)	1/1.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.3	30	V
OUT		V _{IN} +0.3	
EN	0	V _{IN} +0.3	
Junction Temperature, Operating	-40	125	°C

Electrical Characteristics

($V_{IN} = V_{OUT} + 1V$, or $V_{IN} = 2.3V$, $V_{EN} = V_{IN}$, $T_A = 25^\circ C$ unless otherwise specified)

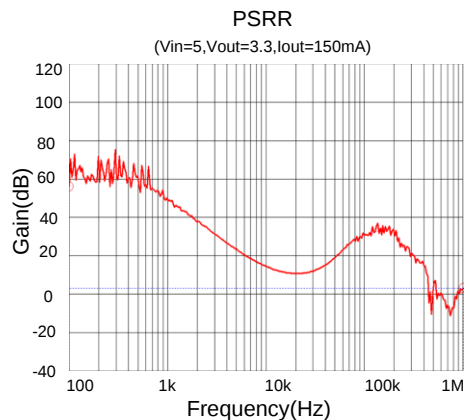
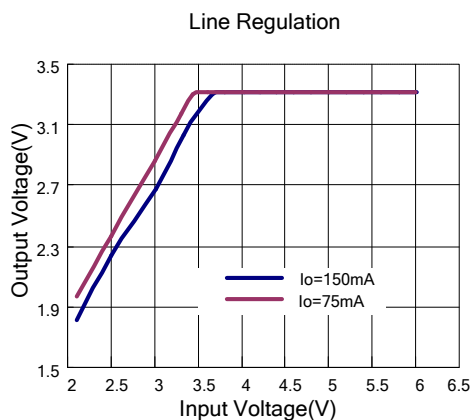
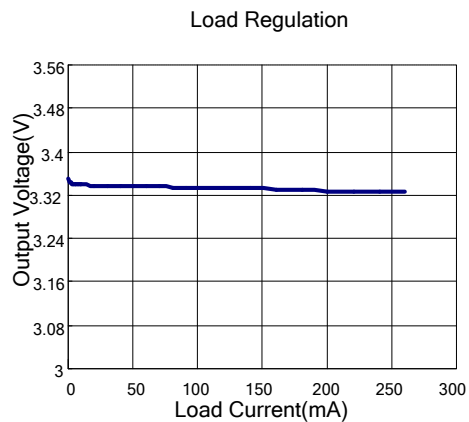
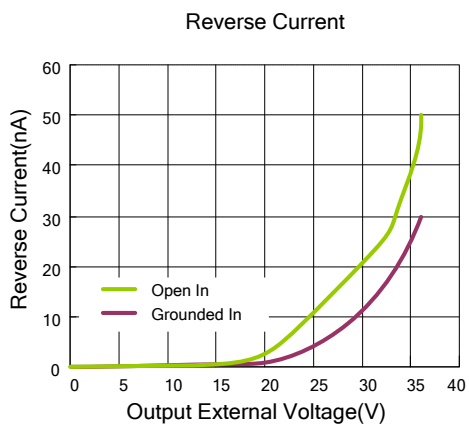
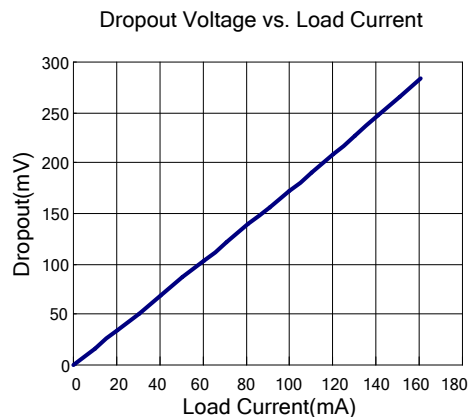
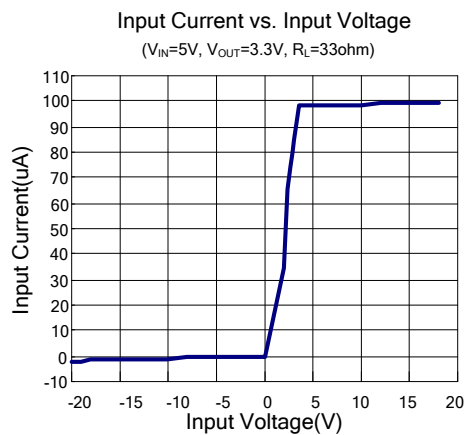
Parameter	Symbol	Test Conditions	Min	Typical	Max	Unit
Input Voltage	V_{IN}		2.3		30	V
Output Voltage Accuracy	V_{OUT}	$I_O = 100\mu A$	-2		2	%
Line Regulation	ΔV_{LNR}	$V_{IN} = (V_{OUT} + 0.3)$ to 30V, $I_O = 100\mu A$		0.04		%
Load Regulation	ΔV_{LDR}	$I_O = 0.1mA$ to 150mA		0.25	1	%
Dropout Voltage	$V_{IN} - V_{OUT}$	$I_O = 10mA$		20		mV
		$I_O = 50mA$		100		mV
		$I_O = 100mA$		200		mV
		$I_O = 150mA$		300		mV
Shutdown Current	I_{SHDN}	$V_{EN} = 0V$, $V_{IN} = 24V$		1		μA
Quiescent Current	I_Q	$I_O = 0.1mA$		18	30	μA
		$I_O = 150mA$		450		μA
Current Limit	I_{LIM}	$V_{OUT} = 0.9 \times V_{OUT}(\text{normal})$		350	500	mA
Reverse leakage current limit	I_{RLK}	$V_{IN} = -15V$, Load=500 Ω		-0.1		μA
Power-supply Rejection Ratio	PSRR	f=1kHz, $C_{OUT} = 10\mu F$		50		dB
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			2.25	V
UVLO Hysteresis	V_{UVLO_TH}			100		mV
Shutdown Discharge Resistor				500		Ω
Enable Input Logic-High Voltage	V_{EN_H}	$V_{IN} = 2.8$ to 5.5V	1.5			V
Enable Input Logic-Low Voltage	V_{EN_L}	$V_{IN} = 2.8$ to 5.5V			0.6	V
Thermal Shutdown Temperature	T_{SD}			150		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYS}			20		$^\circ C$

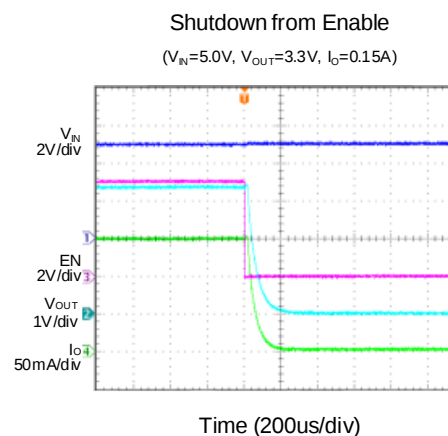
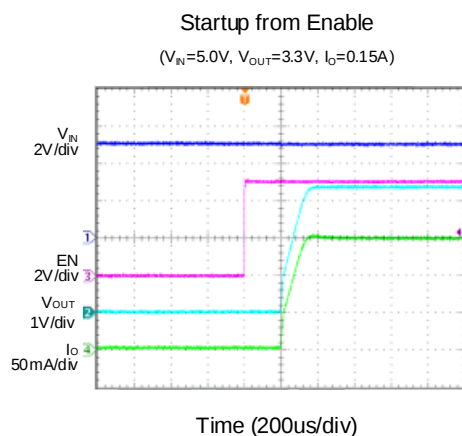
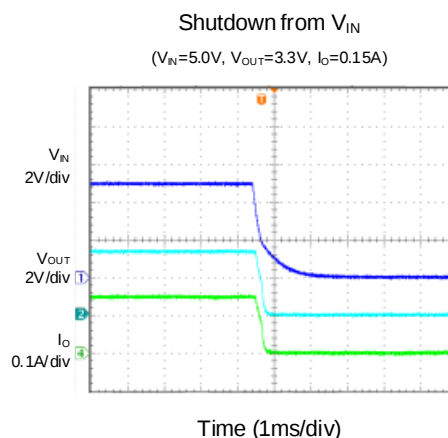
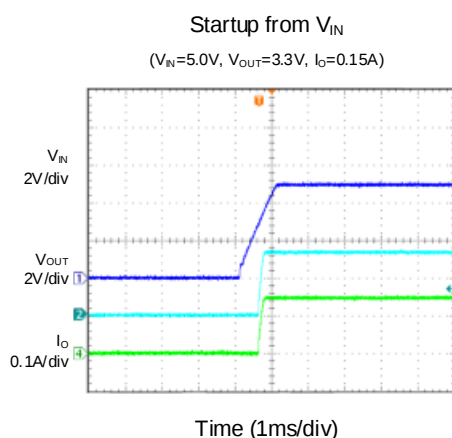
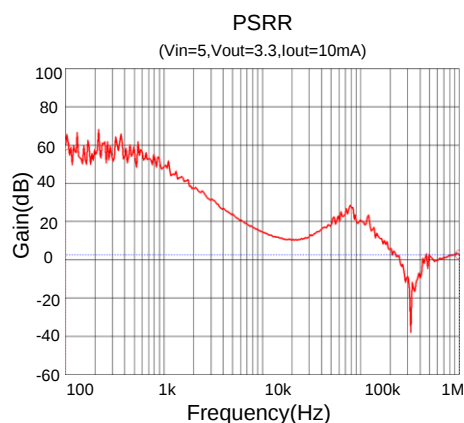
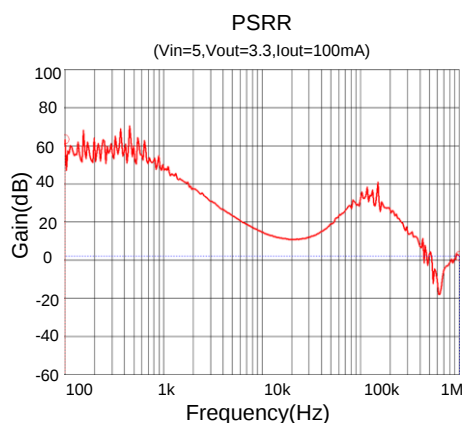
Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

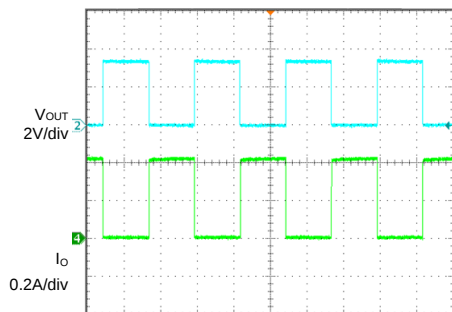
Typical Performance Characteristics





Hard Short Protection

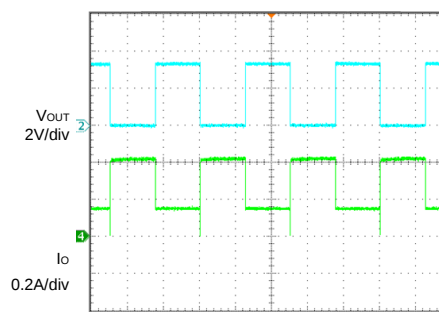
($V_{IN}=5.0V$, $V_{OUT}=3.3V$, Null load to short)



Time (200ms/div)

Hard Short Protection

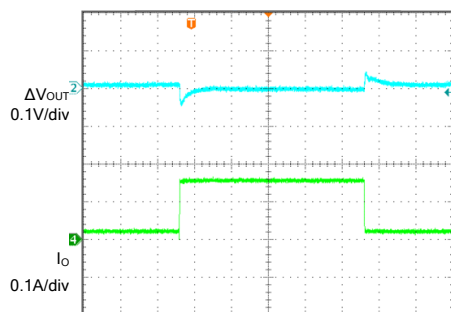
($V_{IN}=5.0V$, $V_{OUT}=3.3V$, 0.15A to short)



Time (200ms/div)

Load Transient

($V_{IN}=5.0V$, $V_{OUT}=3.3V$, $I_O=15\sim150mA$)



Time (40μs/div)

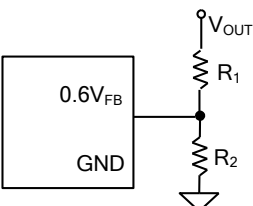
Application Information

The SY20704 is a linear voltage regulator supporting an input voltage range between 2.3V and 30V. It regulates the voltage with a 2% accuracy and has a 150mA maximum output current. Low equivalent series resistance (ESR) ceramic capacitors are recommended at the input and output pins for stable operation.

Feedback Resistor Dividers R_1 and R_2 :

The output voltage of the SY20704 can be adjusted using a resistor divider network, as shown below. To minimize power consumption under light loads, choosing large resistance values for both R_1 and R_2 is recommended. A value of between 10k Ω and 2M Ω is recommended for both resistors.

If the target V_{OUT} is 3.3V, and $R_1=100k$ is selected, then using following equation, R_2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$


Input Capacitor C_{IN} :

A 2.2 μ F decoupling capacitor is recommended between the IN terminal and GND. Locate the input and output capacitors as near as practical to the input and output pins to minimize the trace inductance from the capacitor to the device.

Output Capacitor C_{OUT} :

The SY20704 is designed to operate using low equivalent series resistance (ESR) ceramic capacitors. This forms a zero to provide phase lead which is required for loop stability. A 2.2 μ F or higher ceramic capacitor can be used in this application. Higher capacitance values help to improve transient response.

Dropout Voltage:

The SY20704 has a very low dropout voltage due to its extra low $R_{DS(ON)}$ of the main PMOS, which determines the lowest usable supply voltage.

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

Over-Current and Short-Circuit Protection:

The device includes over-current and short-circuit protection. The device regulates the output current to its threshold limit to protect the device from damage. During over-current or short circuit conditions, the output voltage drops while in the current limiting state, increasing power

dissipation of the internal FET. In cases where often over-current or short-circuits are expected, the input voltage it recommended to be below 9V.

Thermal Considerations:

The SY20704 can source a current of up to 150mA over the full operating junction temperature range. However, the maximum output current must be derated at a higher ambient temperature to limit junction temperature to a maximum of 125°C. The junction temperature must be within the operating range specified under all operating conditions. The LDO power dissipation depends on the input-to-output voltage difference and load current.

The dissipated power, P_D , can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

The operating junction temperature can be estimated by using the following formula:

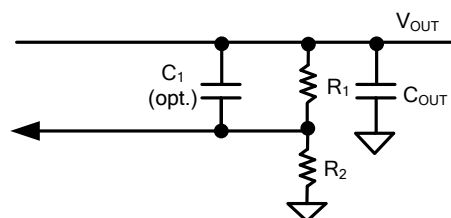
$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum junction temperature of die (125°C), and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) footprint is 100°C/W for the SOT23-5 package and 62°C/W for the DFN2 $\times$ 2-6 package.

Load Transient Considerations:

The SY20704 integrates the compensation components to achieve good stability and fast transient response.

In some applications, adding a small ceramic capacitor in parallel with R_1 may optimize the load transient performance and is thus recommended for applications with large load transient step requirements.

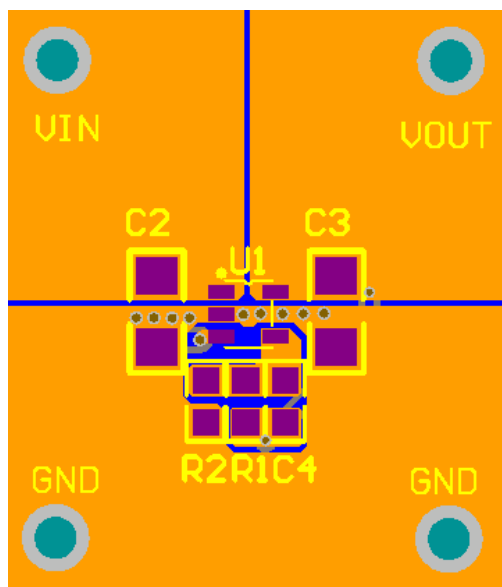


PCB Layout Guide

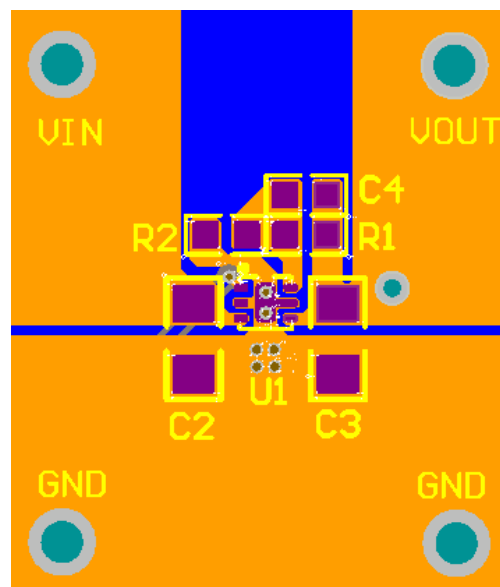
Good board layout practices must be used for stable operation, and a large PCB copper area can improve thermal performance. The input and output capacitors must be directly connected to the input, output, and ground pins of the device using traces which have no other currents flowing through them.

Place C_{IN} and C_{OUT} near the device with short traces to the V_{IN} , V_{OUT} , and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a “single point ground”.

Below are the recommended PCB layout diagrams:

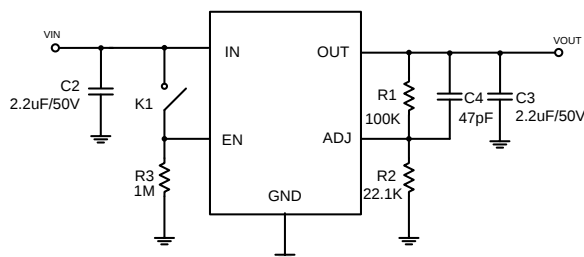


SOT23-5



DNF2x2-6

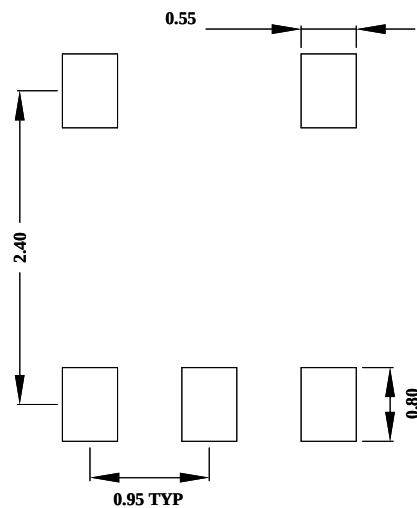
Application Schematic ($V_{OUT} = 3.3V$)



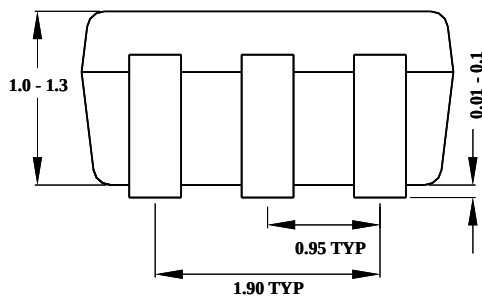
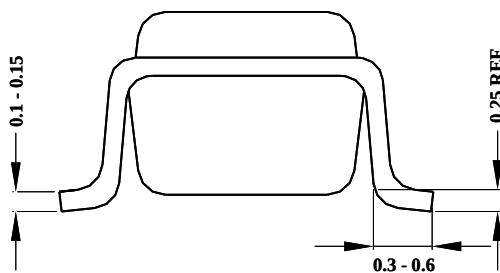
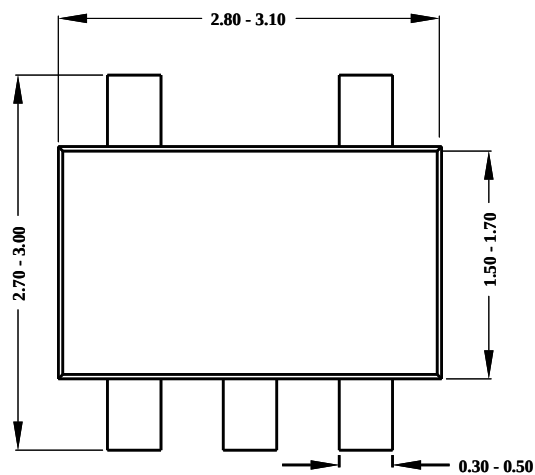
BOM List

Reference Designator	Description	Part Number	Manufacturer
U1	24V, 150mA	SY20704	Silergy
C2, C5	CHIP CAP X7R 2.2μF ±10% 50V 1206	C3216X7R1H225K	TDK
C6	CHIP CAP C0G 47pF ±5% 50V 0603	C1608C0G1H680J	TDK
R1	100KΩ ±1% 0.1W 0603		
R2	22.1KΩ ±1% 0.1W 0603		
R3	1MΩ ±1% 0.1W 0603		

SOT23-5 Package Outline & PCB Layout

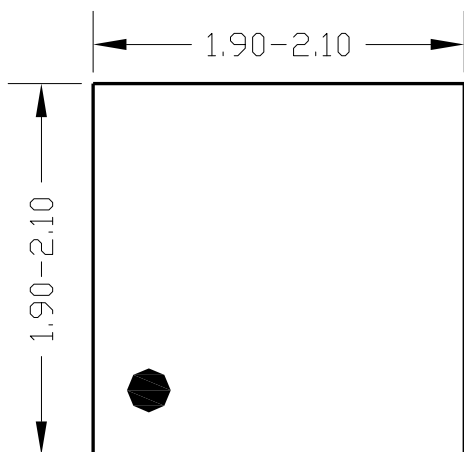


Recommended Pad Layout

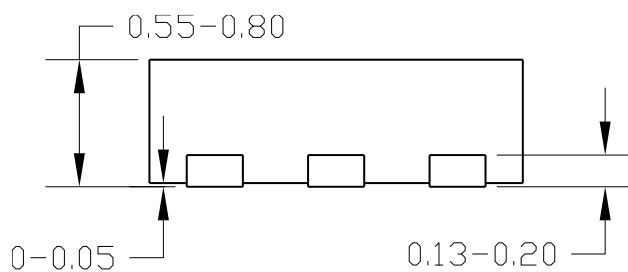


Note: All dimensions are in millimeters and exclude mold flash and metal burr.

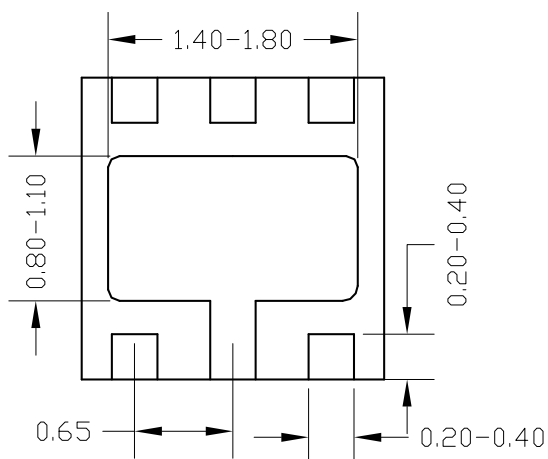
DFN2×2-6 Package Outline



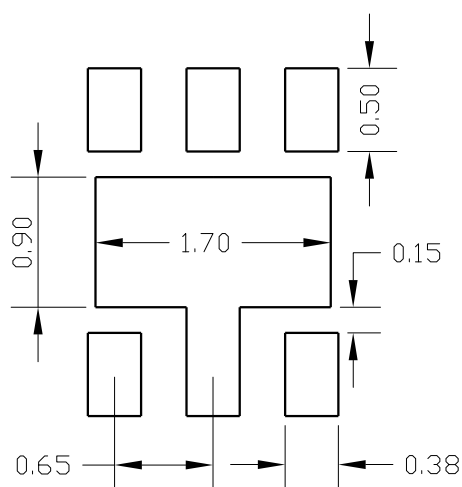
Top View



Side View



Bottom View

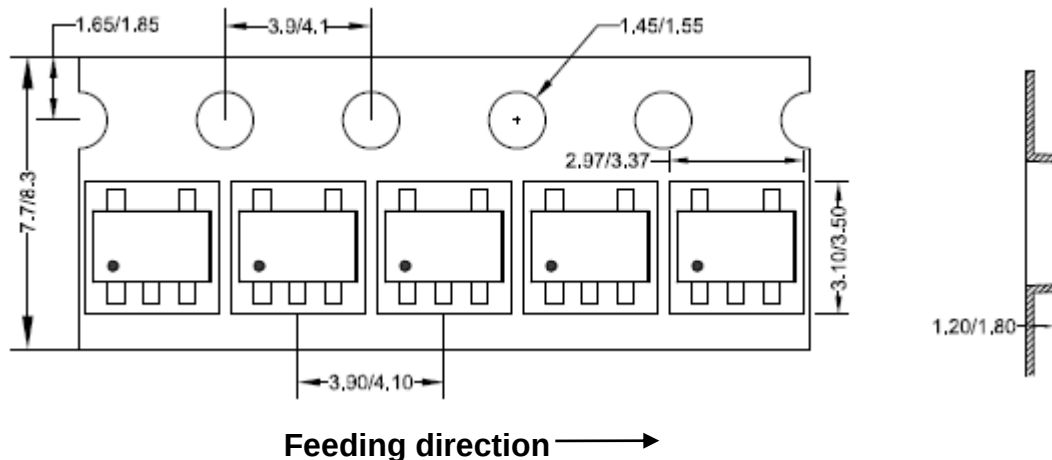


Recommended PCB Layout

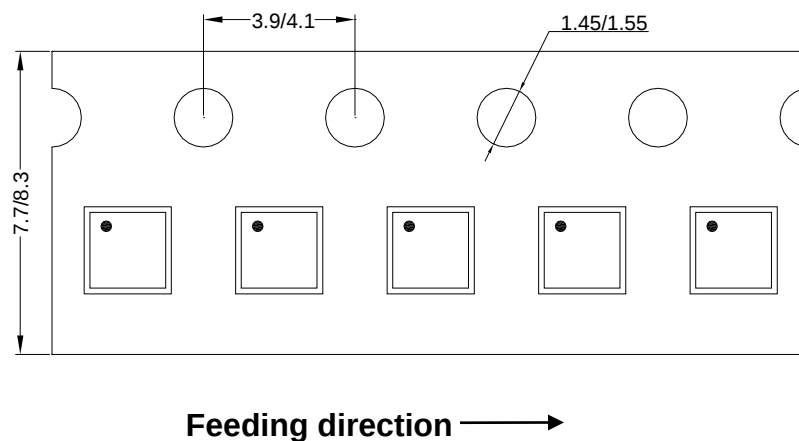
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping & Reel Specification

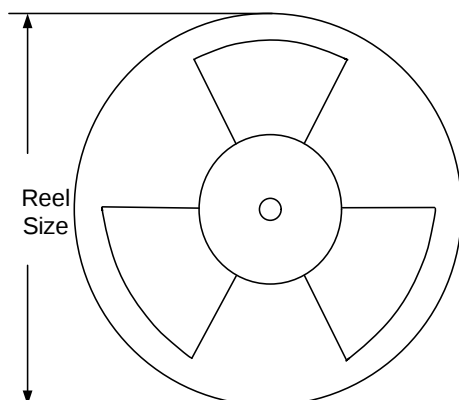
1. SOT23-5 Taping Orientation



2. DFN2x2 Taping Orientation



3. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	280	160	3000
DFN2x2	8	4	7"	400	160	3000

4. Others: NA

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