SY24112

Capacitor-less Headphone/Lineout Driver with LDO & Charge Pump

General Description

The SY24112 is a stereo headphone/lineout driver designed to allow the removal of the output DC blocking capacitors for reducing the component counts and the cost. It is composed of a LDO and a charge pump. The SY24112 is an ideal choice for small portable electronics where size and cost are critical design parameters. The SY24112 is capable of driving 21mW into a 32Ω load at 3.3V when R_S=47Ω. The gain of SY24112 is set by the Gain Control pin. The charge pump and the headphone power are supplied by the LDO.

Ordering Information

SY24112 □(□,□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY24112QDC	QFN3×3-16	----

Features

- 21mW/Ch Output Power into 32Ω Load at 3.3V When R_S=47Ω
- 86mW/Ch Output Power into 32Ω Load at 3.3V When R_S=0Ω
- Wide Power Supply Range: 2.2V-5.5V
- Ground Referenced Outputs Eliminate the DC Bias Voltage on the Headphone Ground Pin
- No Output DC Blocking Capacitors
- Reduced Board Area
- Reduced Component Cost
- Improved THD+N Performance
- No Degradation of the Low Frequency Response Due to the Output Capacitors
- Built in the LDO and the Charge Pump
- Short Circuit Protection, Thermal Protection and Under Voltage Protection
- Click and Pop Suppression Circuit
- Surface Mount, QFN, 16 Pin, 3mm×3mm

Applications

- Notebook Computers
- CD/MP3 Player
- Smart Phones
- Cellular Phones
- PDA

Typical Application

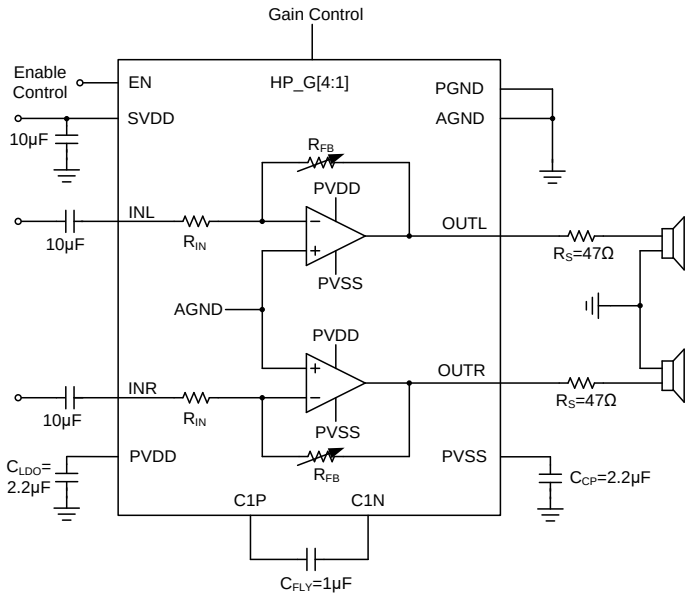
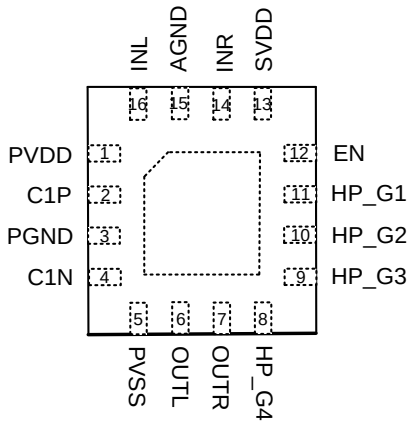


Figure1. Typical Application

Pinout (Top View)



(QFN3×3-16)

Top Mark: cB*xyz* (device code: cB, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Description
PVDD	1	LDO output / HP-amp positive supply.
C1P	2	Charge pump flying capacitor positive terminal.
PGND	3	Power ground (connected to GND).
C1N	4	Charge pump flying capacitor negative terminal.
PVSS	5	Output from negative Charge Pump / HP-amp negative supply.
OUTL	6	Left audio channel output signal.
OUTR	7	Right audio channel output signal.
HP_G4	8	Gain control.
HP_G3	9	Gain control.
HP_G2	10	Gain control.
HP_G1	11	Gain control.
EN	12	Enable pin, active high logic.
SVDD	13	Supply voltage.
INR	14	Right audio channel input signal.
AGND	15	Analog ground (connect to GND).
INL	16	Left audio channel input signal.

Block Diagram

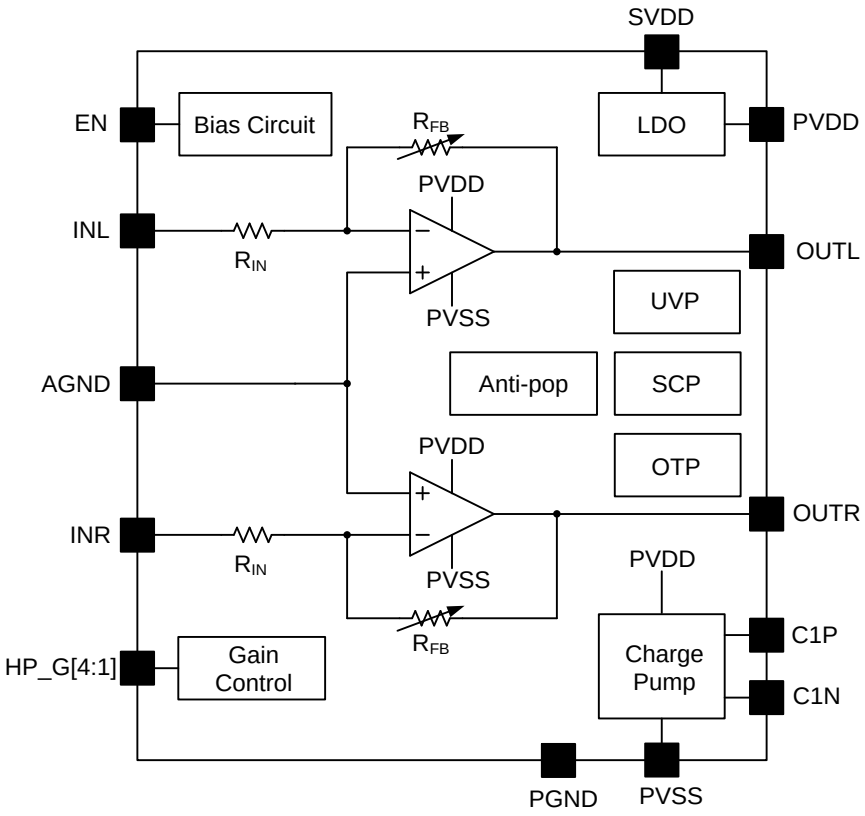


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Voltage Range (SVDD) ---------- -0.3V to 6V
Input Voltage ---------- -0.3V to (SVDD+0.3)V
Junction Temperature Range ---------- -40°C to 150°C
Storage Temperature Range ---------- -40°C to 125°C

Recommended Operating Conditions

Supply Voltage Range ---------- 2.2V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(T_A=25°C, SVDD=3.3V, Gain=6dB, R_S=47Ω, R_L=32Ω, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Characteristics						
Quiescent Supply Current	I_Q	EN=1, no load (Note 2)		9.5		mA
		EN=1, no load, V_{DD}=2.4V (Note 2)		7.2		mA
		EN=1, no load, V_{DD}=5V (Note 2)		9.6		mA
		EN=0, no load		0.5	1	μA
High-level Input Voltage	V_{IH}	EN, HP_G1, HP_G2, HP_G3, HP_G4	1.2			V
Low-level Input Voltage	V_{IL}	EN, HP_G1, HP_G2, HP_G3, HP_G4			0.45	V
High-level Input Current	$\|I_{IH}\|$	EN, HP_G1, HP_G2, HP_G3, HP_G4, SVDD=5V, V_I=5V		0.1	1	μA
Low-level Input Current	$\|I_{IL}\|$	EN, HP_G1, HP_G2, HP_G3, HP_G4, SVDD=5V, V_I=0V		0.1	1	μA
High-level Output Voltage (Note 2)	V_{OH}	Gain=0dB, V_I=-3.3V		3		V
		Gain=0dB, R_L=10kΩ, V_I=-3.3V		3.25		V
Low-level Output Voltage (Note 2)	V_{OL}	Gain=0dB, V_I=3.3V		-2.8		V
		Gain=0dB, R_L=10kΩ, V_I=3.3V		-3.25		V
Gain	A_V	HP_G[4:1]=0, no load	-0.5	0	0.5	dB
		HP_G[4:1]=2, no load	5.5	6	6.5	
		HP_G[4:1]=15, no load	18.5	19	19.5	
Gain Matching	ΔA_V	HP_G[4:1]=0, no load	-1		1	%
		HP_G[4:1]=2, no load	-1		1	
		HP_G[4:1]=15, no load	-1		1	
Output Offset Voltage	$\|V_{OS}\|$	V_I=0V		1	10	mV
LDO Output Voltage	PVDD	No load	3.05	3.25		V
Charge Pump Output Voltage	PVSS	No load		-3.2	-2.95	V
Charge Pump Switching Frequency	f_{OSC}		750	1000	1350	kHz
Input Impedance (Note 2)				20		kΩ
Turn-on Time (Note 2)	t_{ON}	EN=1		1.5		ms
Turn-off Time (Note 2)	t_{OFF}	EN=0		15		μs

AC Characteristics (Note 2)						
Output Power	P_O	1% THD+N, f=1kHz		21		mW
		1% THD+N, f=1kHz, V_{DD}=5V		22		
		1% THD+N, f=1kHz, R_L=16Ω		16		
		1% THD+N, f=1kHz, R_S=0Ω (Note 3)		86		
		1% THD+N, f=1kHz, V_{DD}=5V, R_S=0Ω (Note 3)		89		
		1% THD+N, f=1kHz, R_L=16Ω, R_S=0Ω (Note 3)		98		
Signal to Noise Ratio	SNR	10mW output, f=1kHz, A-weighted		103		dB
		Max output at THD+N<1%, f=1kHz, A-weighted		106		
		2Vrms output, f=1kHz, R_L=47kΩ, A-weighted		107		
		Max output at THD+N<1%, f=1kHz, R_L=47kΩ, A-weighted		109		
Total Harmonic Distortion +Noise	THD+N	Po=10mW, f=1kHz		0.015		%
		Po=10mW, f=20Hz		0.01		
		V_O=2Vrms, f=1kHz, R_L=47kΩ		0.007		
Output Integrated Noise	V_n	20Hz to 22kHz, A-weighted filter, Gain=0dB		2.7		μV
Crosstalk	CT	Po=10mW, f=1kHz		-90		dB
		V_O=2Vrms, f=1kHz, R_L=47kΩ		-90		dB
Power Supply Rejection Ratio	PSRR	200mV_{PP} ripple, f=1kHz		-83		dB
Shutdown Attenuation		EN=0, reference to Po=10mW f=1kHz		-130		dBr
Slew Rate	SR	Gain=0dB, V_I=3V pulse		3		V/μs
Protection						
Under Voltage Protection	V_{UVP}	V_{DD} rising		2	2.2	V
		V_{DD} falling	1.65	1.85		V
Short Circuit Protection Current Limit (Note 2)	I_{SC}	Short to SVDD		300		mA
		Short to GND		200		mA
Thermal Shutdown Temperature (Note 2)	T_{SD}	Threshold		155		°C
		Hysteresis		30		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

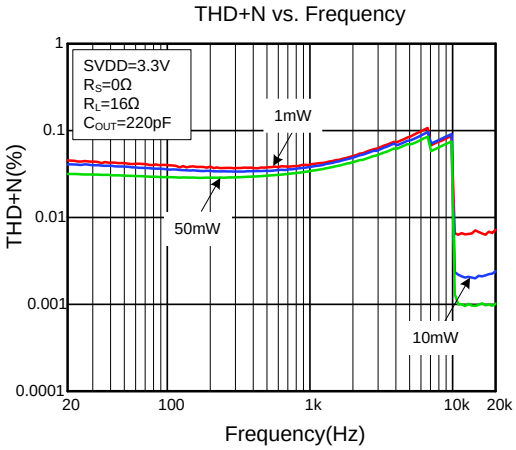
Note 2: Typical test value on the demonstration board (C_{LDO}=2.2μF, C_{FLY}=1μF, C_{CP}=2.2μF), guaranteed by design.

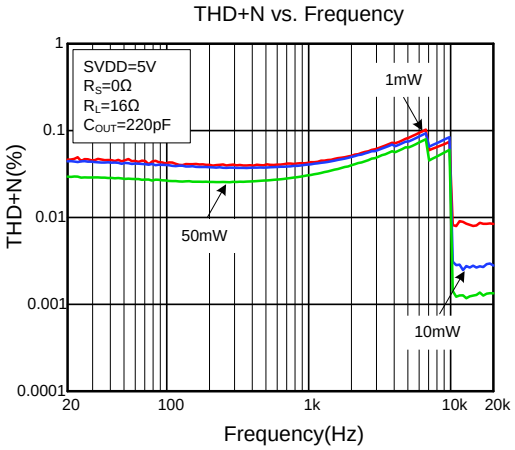
Note 3: For R_S=0Ω application, the output capacitor is 220pF on the demonstration board.

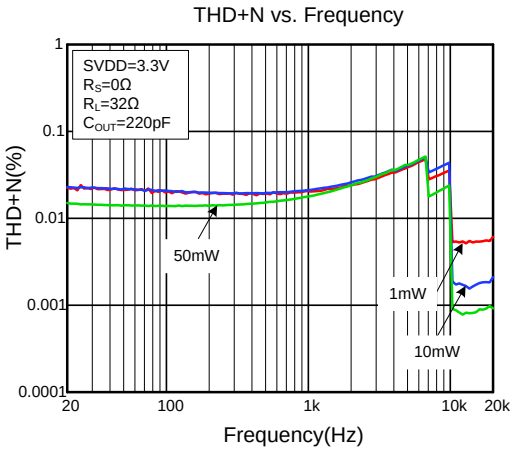
Typical Performance Characteristics

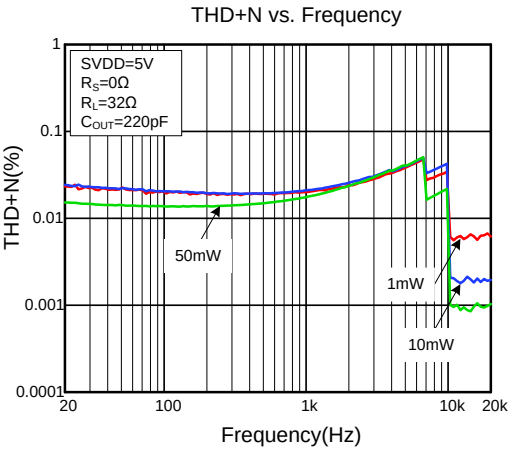
(All Measurements taken at C_{LDO}=2.2μF, C_{FLY}=1μF, C_{CP}=2.2μF, f=1 kHz, Gain=6dB, unless otherwise noted.)

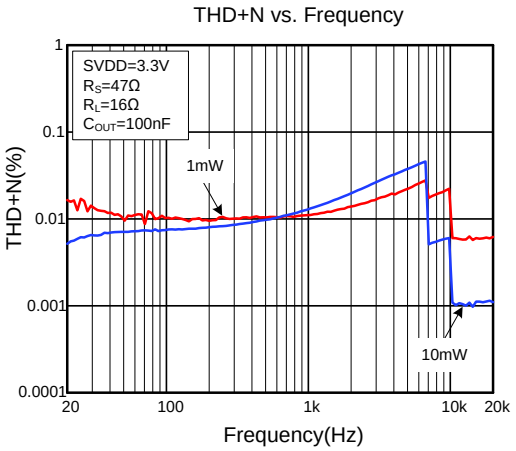
Headphone

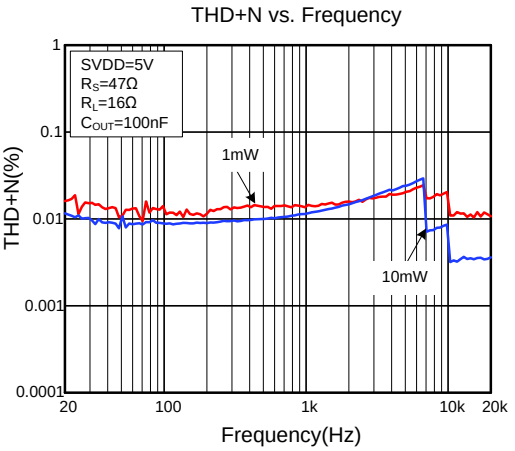




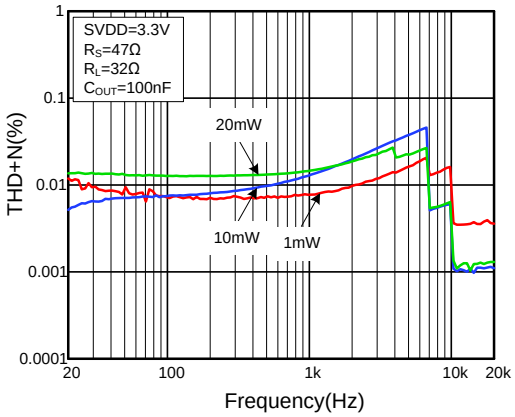




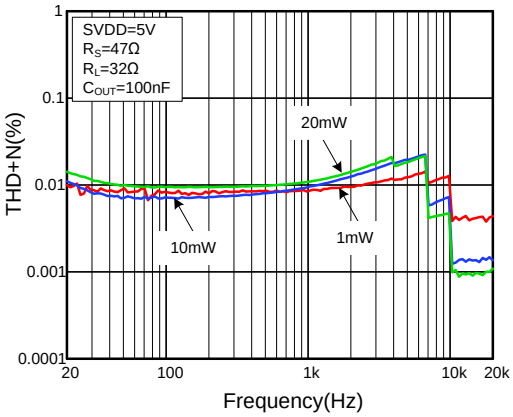




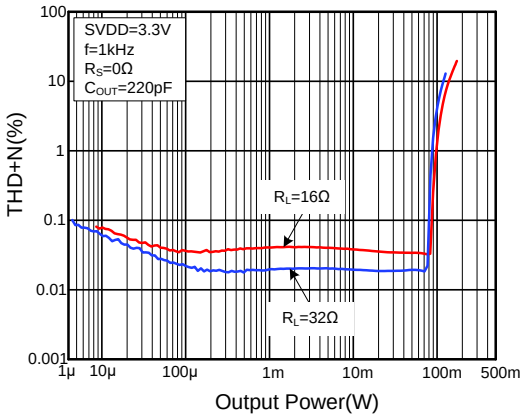
THD+N vs. Frequency



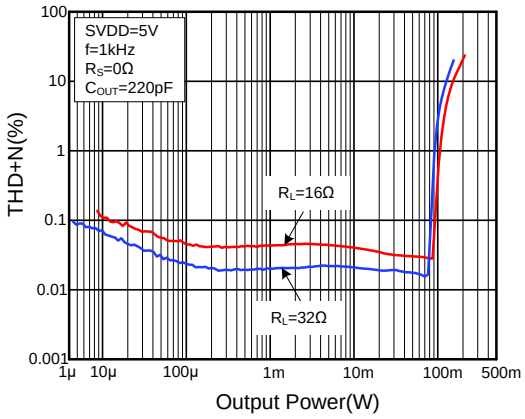
THD+N vs. Frequency



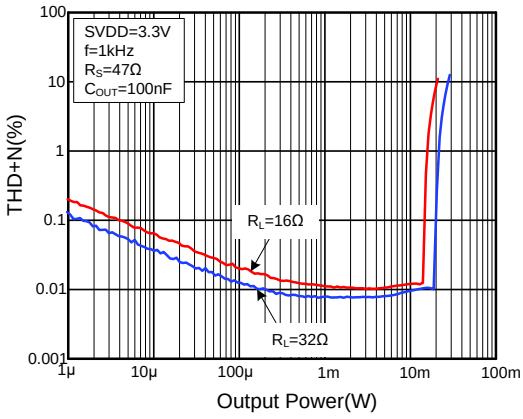
THD+N vs. Output Power



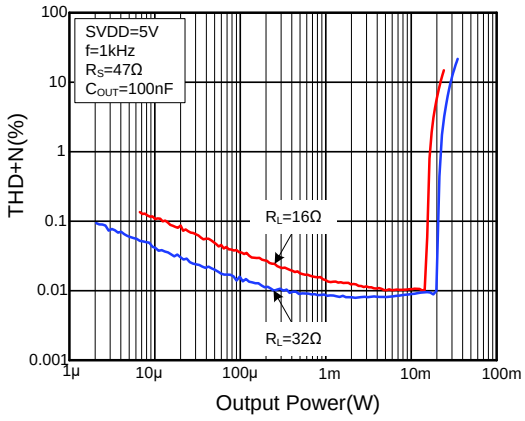
THD+N vs. Output Power



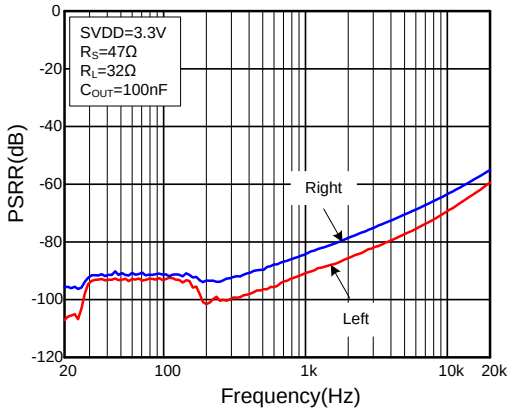
THD+N vs. Output Power



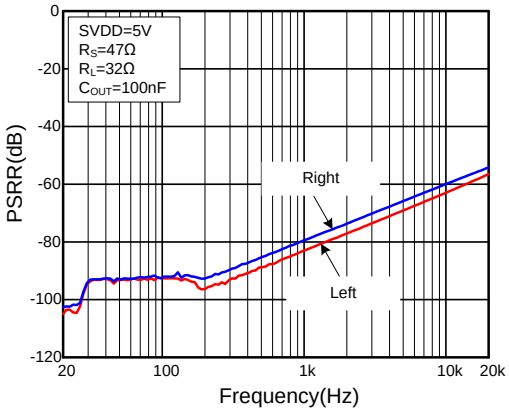
THD+N vs. Output Power



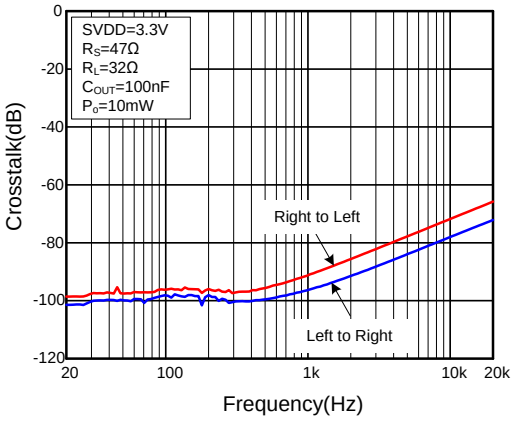
PSRR vs. Frequency



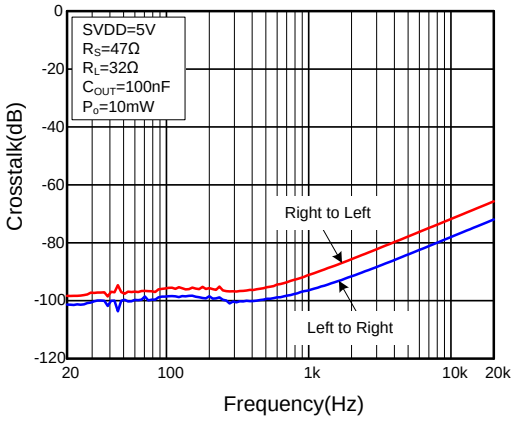
PSRR vs. Frequency



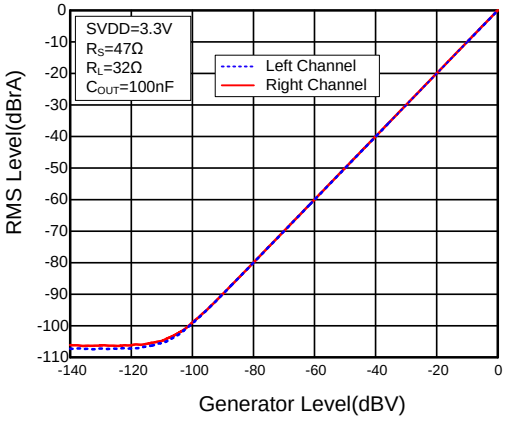
Crosstalk vs. Frequency



Crosstalk vs. Frequency



SNR



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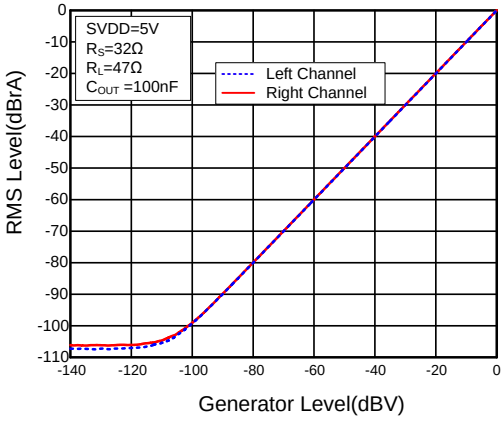
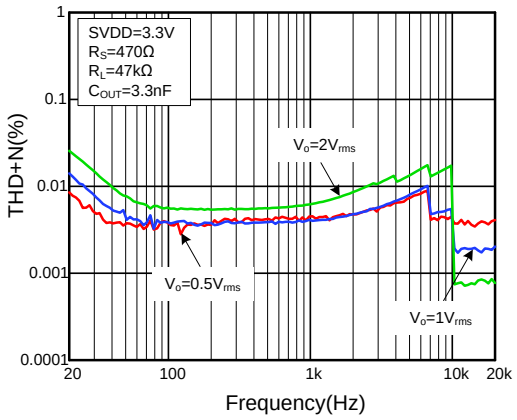
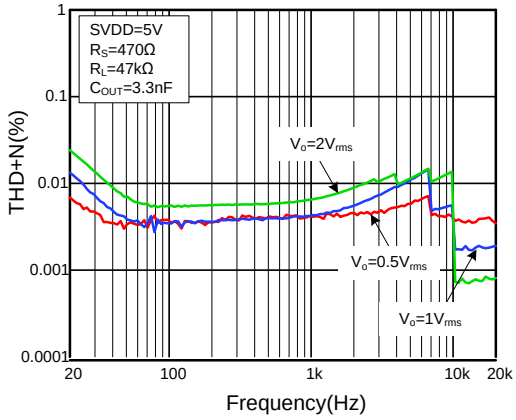


Line Out

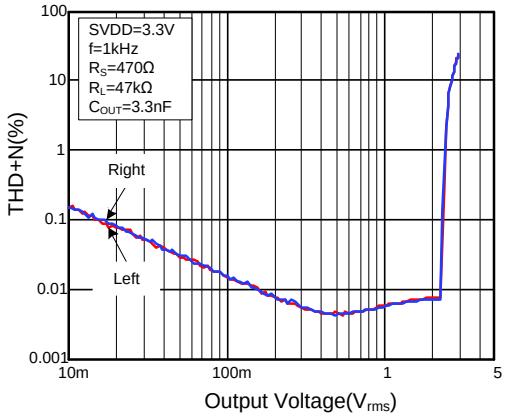
THD+N vs. Frequency



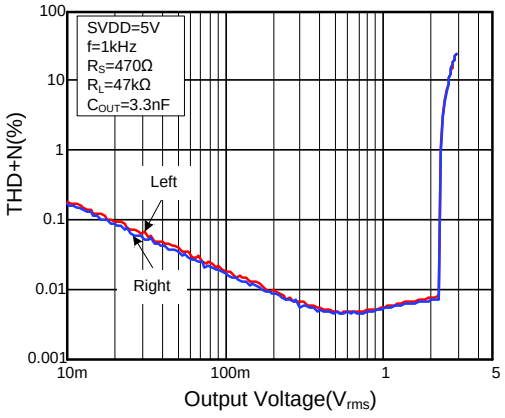
THD+N vs. Frequency



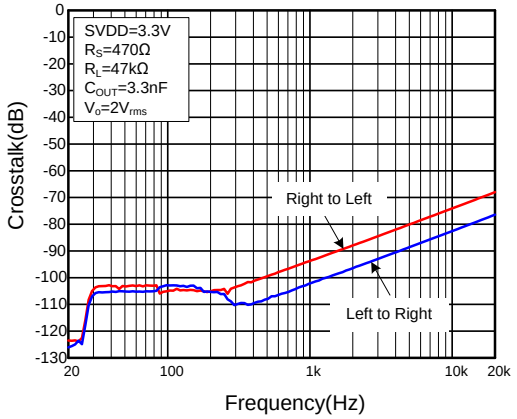
THD+N vs. Output Voltage



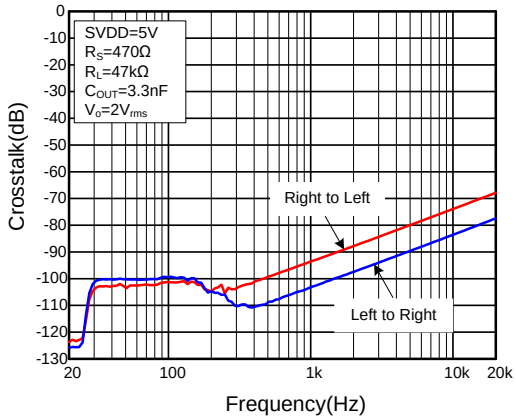
THD+N vs. Output Voltage

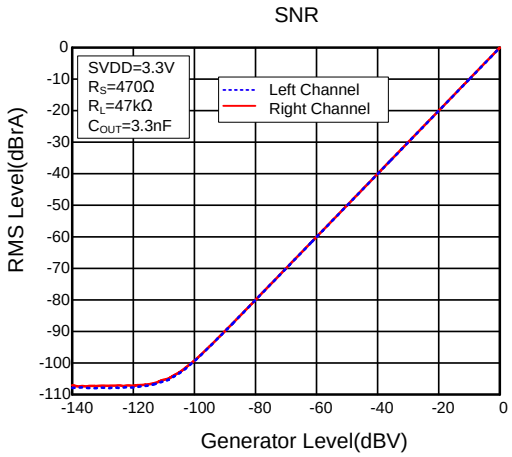


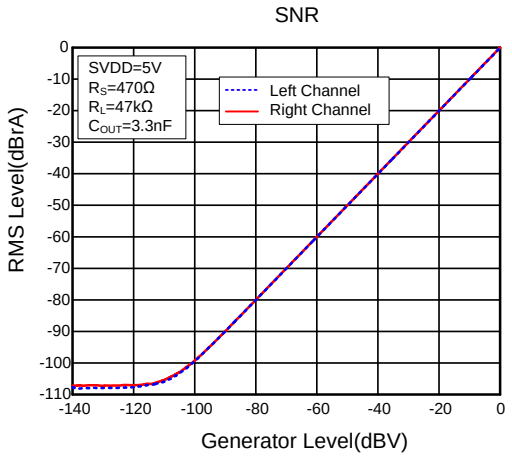
Crosstalk vs. Frequency



Crosstalk vs. Frequency







Function Description

This section focuses on the description of the SY24112 capacitor-less headphone/lineout driver function block operation.

Capacitor-less Headphone Amplifier

Single-supply headphone amplifiers typically require DC-blocking capacitors. The capacitors are required because most headphone amplifiers have a DC bias on the output pin. If the DC bias is not removed, the power consumption will be higher, the large DC current will rush through the headphones and potentially damage them. The top drawing in Figure 3 illustrates the conventional headphone amplifier connection.

The DC blocking capacitors are always large in value. The headphone speakers (typical resistive values of 16Ω or 32Ω) combine with the DC blocking capacitors to form a high-pass filter. The -3dB frequency of the filter is very low, so the capacitor must have a large value because the load resistance is small. The large capacitance values require large package sizes. The large package sizes consume the PCB area, stand high above the PCB and increase the cost of assembly, which will reduce the fidelity of the audio output signal.

The capacitor-less amplifier architecture operates from a single supply but uses an internal charge pump to provide a negative voltage rail. Combining the positive rail provided by the LDO and the negative rail generated by the charge pump, the device operates in an effective split supply mode. The output voltages are centered at 0V now with the capability to swing to the positive rail or the negative rail. The capacitor-less amplifier requires no output DC blocking capacitors. It does not place any voltage on the sleeve. The bottom block diagram and the waveform of Figure 3 illustrate the ground-referenced headphone architecture. This is the architecture of the SY24112.

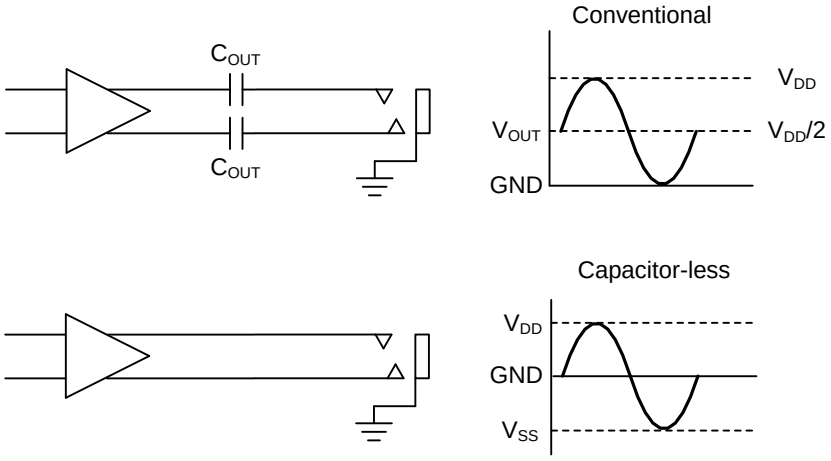


Figure3. Amplifier Application

Lineout Amplifier

The SY24112 can be used as an audio lineout driver capable of providing 2.0Vrms into 47kΩ loads with the single supply of 3.3V.

Modes of Operation

The SY24112 supports two modes of operation. When the EN pin is driven to low, the device will be in low power mode with the LDO and the charge pump powered down, the audio channels disabled and the outputs pulled to the ground. When the EN pin is driven to high, the device will enter active mode with the LDO and the charge pump powered up and the audio channels enabled. The transition from inactive to active state and active to inactive state is done softly through the anti-pop process to avoid the audible artifacts.

Gain Setting

The gain of the SY24112 is programmed by the Gain Control pin as Table 1.

Number	HP_G1	HP_G2	HP_G3	HP_G4	dB
1	0	0	0	0	0
2	0	0	0	1	5
3	0	0	1	0	6
4	0	0	1	1	7
5	0	1	0	0	8
6	0	1	0	1	9
7	0	1	1	0	10
8	0	1	1	1	11
9	1	0	0	0	12
10	1	0	0	1	13
11	1	0	1	0	14
12	1	0	1	1	15
13	1	1	0	0	16
14	1	1	0	1	17
15	1	1	1	0	18
16	1	1	1	1	19

Table1. Gain Set Table

Input-blocking Capacitor

The input capacitor C_{IN} is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. The input resistance R_{IN} of the SY24112 remains a constant value 20kΩ with the change of the gain. In this case, C_{IN} and R_{IN} will compose a high-pass filter with the cutoff frequency determined in the following equation:

$$f_c(\text{highpass}) = \frac{1}{2\pi R_{IN} C_{IN}}$$

The value of C_{IN} is important to consider carefully because it directly affects the low frequency THD performance and the pop noise of the circuit.

LDO Output Capacitor

The SY24112 uses the LDO to generate the positive voltage PVDD to supply the amplifier. The LDO needs an output capacitor to be stable and reduces the output voltage ripple. Using a low-ESR ceramic capacitor greater than 2.2μF is recommended.

Charge Pump Flying Capacitor

The SY24112 uses the charge pump to generate the negative voltage PVSS to supply the amplifier. The charge pump flying capacitor C_{FLY} serves to transfer the charge during the generation of the negative supply voltage as Figure 4. It affects the load transient of the charge pump. If the capacitor's value is too small, it will increase the charge pump's output resistance and degrade the performance of the headphone amplifier. It is recommended to use the low ESR ceramic capacitor with a typical value of 1μF.

Charge Pump Output Capacitor

The charge pump needs an output capacitor to filter the negative output current pulse flowing into PVSS pin and reduce the output voltage ripple. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow the maximum charge to transfer. Using a low ESR ceramic capacitor greater than 2.2μF is recommended.

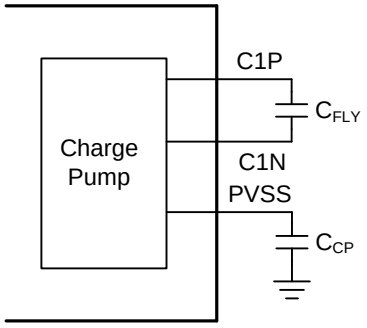


Figure4. Charge Pump Connection

Power Supply Decoupling Capacitor

The SY24112 is a direct path amplifier that requires adequate power-supply decoupling to ensure that the noise and the THD+N are low. A good low ESR ceramic capacitor, typically 10μF, placed as close as possible to the device SVDD pin works best.

Under Voltage Protection

If the voltage on the SVDD pin falls below the under voltage threshold 1.85V, the amplifier will be disabled and the internal logic will be reset. The operation will resume when SVDD rises above the UVLO threshold with 0.15V hysteresis.

Short Circuit Protection

The SY24112 has the protection for short circuit caused by a short from output port to VDD or GND. The current limiting block prevents the output current too high to damage the device.

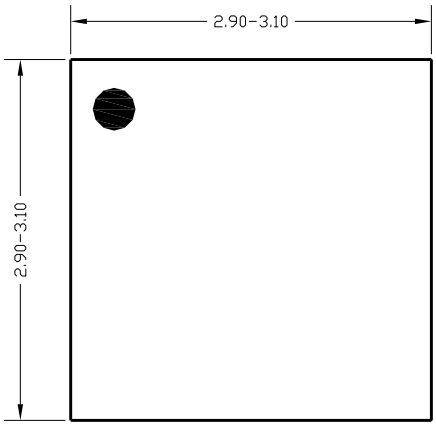
Thermal Protection

The thermal protection on the SY24112 will prevent damage to the device when the internal die temperature exceeds 155°C. Once the die temperature exceeds the thermal set point, the device will enter the shutdown state and the outputs will be disabled. This is not a latched fault. The thermal fault will be cleared once the temperature of the die is reduced by 30°C.

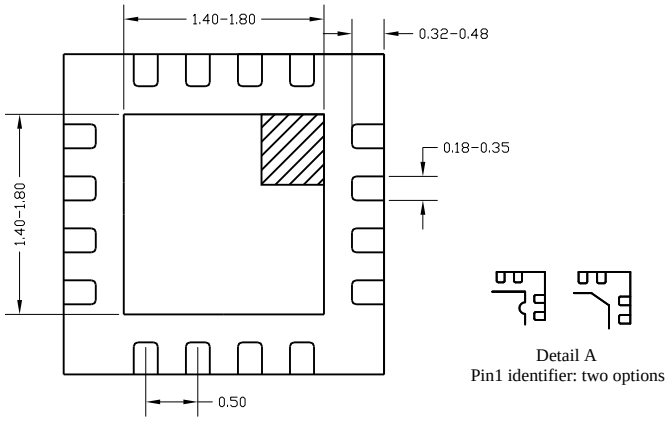
PCB Layout

1) All the components should be placed close to the SY24112. The decoupling capacitors should be placed by the power pin to decouple the power rail noise.
2) The input traces should be short and symmetric.
3) The output traces should be short, wide, and symmetric.
4) The power traces width should be greater than 50mil.
5) The ground traces are recommended to be routed as a star ground to minimize the interference.
6) The QFN thermal PAD should be soldered on the PCB.

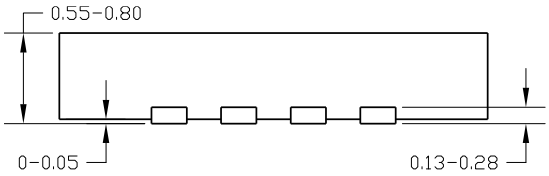
QFN3×3-16 Package Outline & PCB Layout



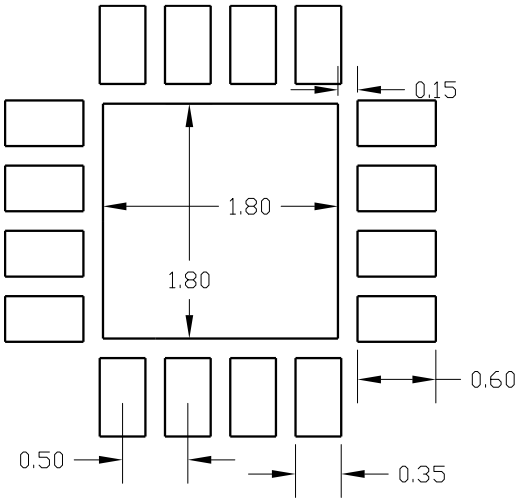
Top View



Bottom View



Front View

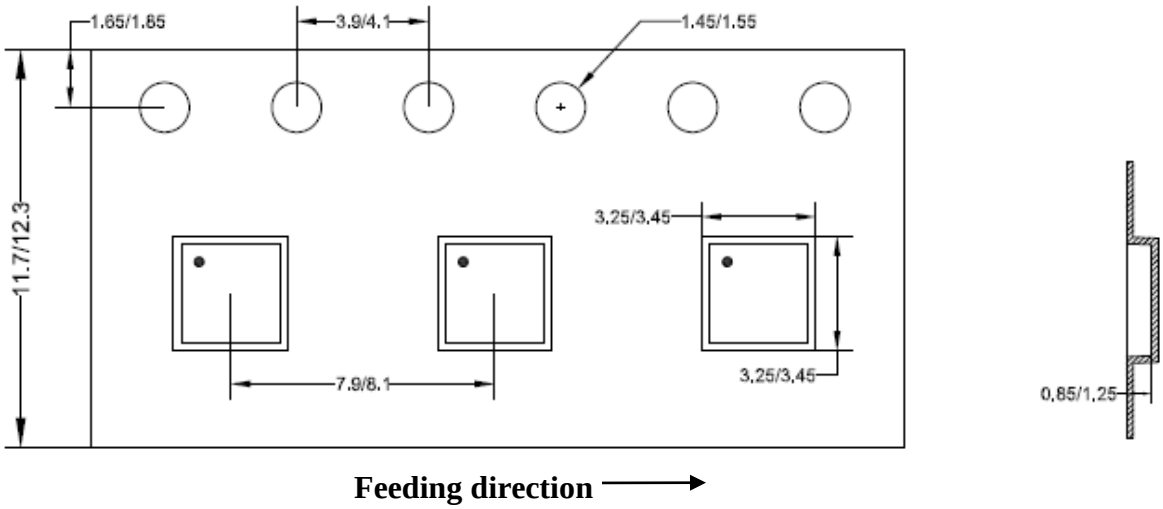


PCB layout (Recommended)

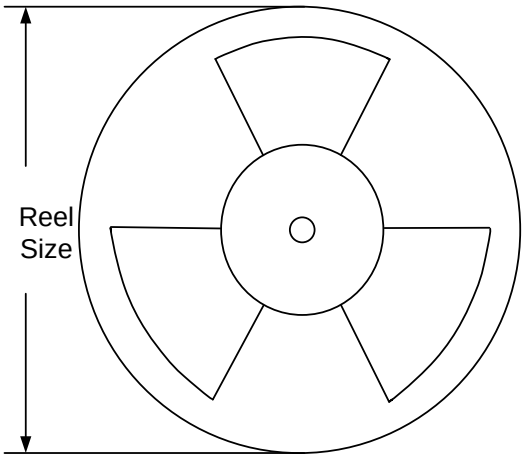
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. QFN3×3-16 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description
Rev 0.9	Oct 22, 2018	Initial Release
Rev 1.0	Oct 22, 2019	Production Release

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