General Description

The SY24104 is an analog Class-D audio power amplifier. It has filterless operation control strategy which eliminates the LC filter for each channel to reduce the size of final product and the cost of mass production. It has high conversion efficiency for driving two bridge-tied stereo speakers with no need for an external heat sink when playing music. The spread spectrum operation mode is achieved internally to improve the EMI performance. The amplifier gain of SY24104 in audible bandwidth is selectable by the external pin. Fully short protection at output side against shorts to GND, V_{DD} and out-to-out is achieved with auto recovery capability.

Ordering Information

SY24104 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY24104QCC	QFN4×4-24	----

Features

- 2×7W into 8Ω BTL Loads @1% THD+N from a 12V Supply
- 2×4W into 8Ω BTL Loads @10% THD+N from an 8V Supply
- 2×2.3W into 8Ω BTL Loads @10% THD+N from a 6V Supply
- Operates from 5.5V to 16V
- Filterless/Filter Operation
- Spread-Spectrum Modulation for Good EMI Performance
- High PSRR
- High Efficiency Class-D Operation Eliminates Need for Heat Sinks
- Four Fixed-gain Controlled: 20dB, 26dB, 32dB and 36dB
- Internal Oscillator (No External Components Required)
- Thermal and Short-Circuit Protection with Auto Recovery
- Comprehensive Click and Pop Suppression
- Space-saving Surface Mount QFN4×4-24 Package

Applications

- Flat Panel Display TVs, DLP®TVs, CRT TVs
- Powered Speakers
- Music Instruments
- Boom Box
- DVD Players, Game Machines

Typical Application

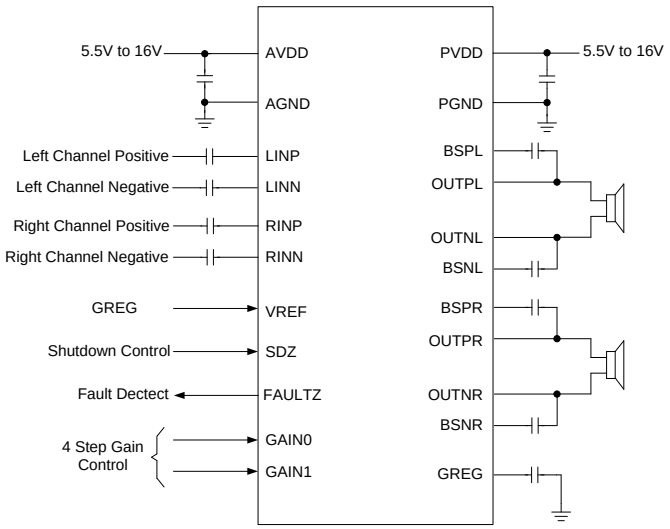
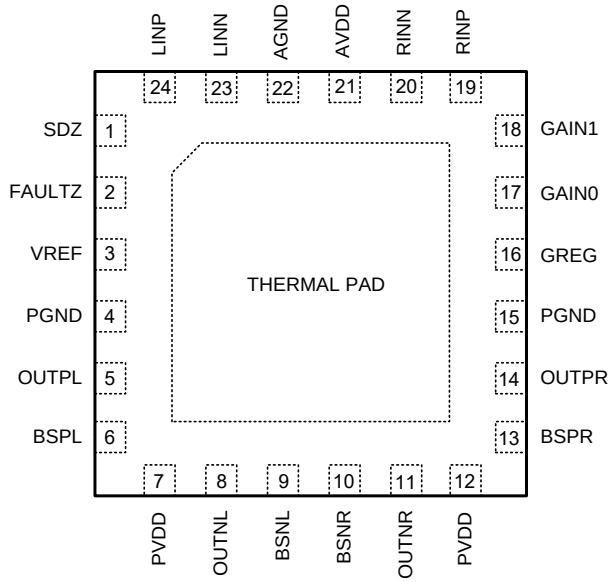


Figure1. Typical Application Circuit

Pinout (top view)



Top mark: **BDP*xyz*** (Device code: BDP, ***x=year code, y=week code, z= lot number code***)

Name	Number	Description
SDZ	1	Shutdown signal for IC (low=disabled, high=operational). TTL logic levels with compliance to AVDD.
FAULTZ	2	Open drain output used to display short circuit. Voltage compliant to AVDD. Short circuit faults can be set to auto-recovery by connecting this pin to SDZ pin.
VREF	3	Internal Reference Pin. Connect to GREG directly.
PGND	4	Power ground.
OUTPL	5	Class-D H-bridge positive output for left channel.
BSPL	6	Bootstrap I/O for left positive channel.
PVDD	7	Power supply.
OUTNL	8	Class-D H-bridge negative output for left channel.
BSNL	9	Bootstrap I/O for left negative channel.
BSNR	10	Bootstrap I/O for right negative channel.
OUTNR	11	Class-D H-bridge negative output for right channel.
PVDD	12	Power supply.
BSPR	13	Bootstrap I/O for right positive channel.
OUTPR	14	Class-D H-bridge positive output for right channel.
PGND	15	Power ground.
GREG	16	Gate drive supply. Nominal voltage is 3.4V.
GAIN0	17	Gain select least-significant bit. TTL logic levels with compliance to AVDD.
GAIN1	18	Gain select most-significant bit. TTL logic levels with compliance to AVDD.
RINP	19	Positive audio input for right channel. Biased at 1.7V.
RINN	20	Negative audio input for right channel. Biased at 1.7V.
AVDD	21	Analog power supply. Not internally connected to PVDD.
AGND	22	Analog ground.
LINN	23	Negative audio input for left channel. Biased at 1.7V.
LINP	24	Positive audio input for left channel. Biased at 1.7V.
Thermal Pad	25	Connect to GND for best system performance. If not connected to GND, leave floating.

Function Block

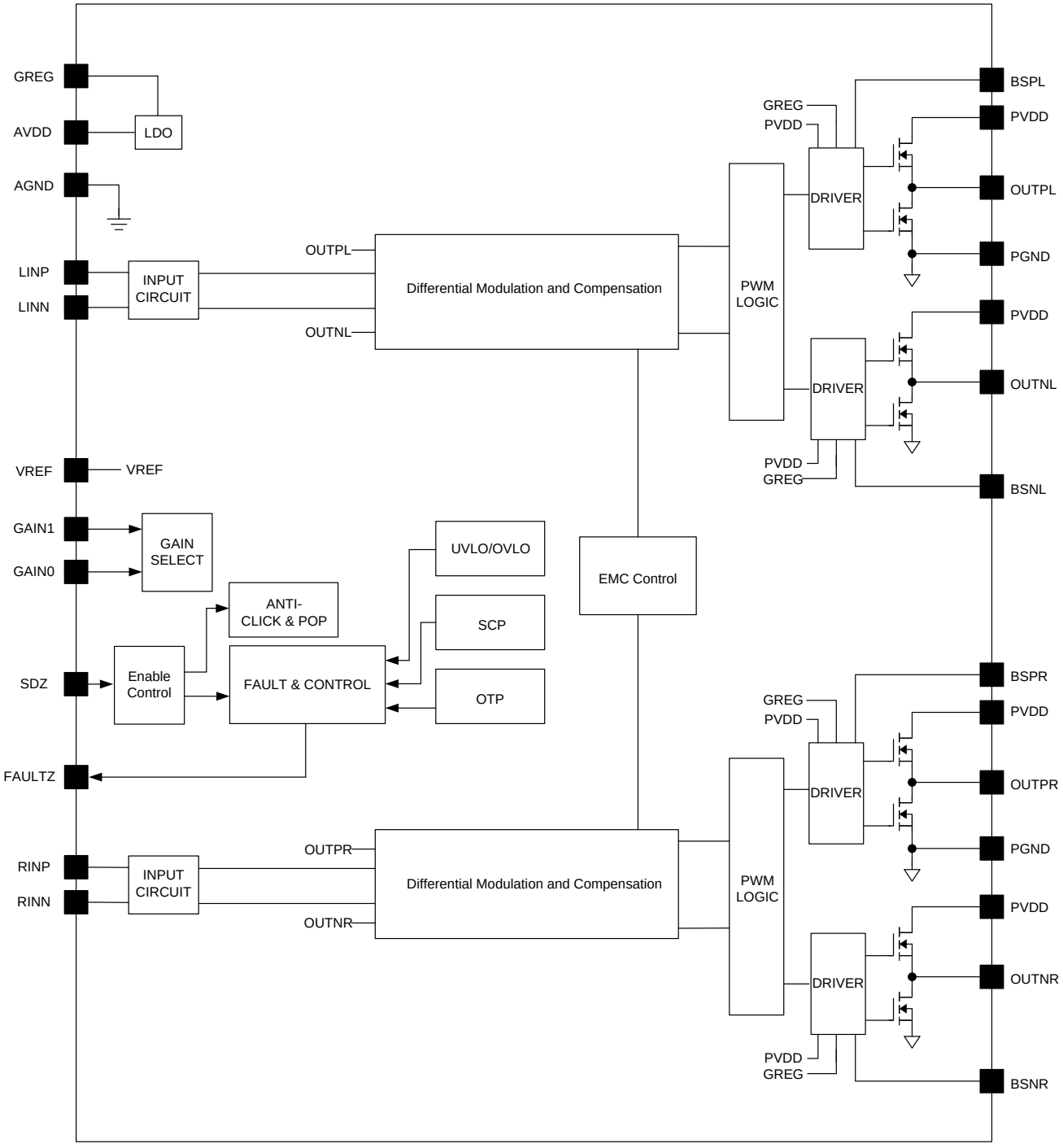


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

AVDD, PVDD (Note 2) ---------- -0.3V to 18V
RIN, LIN---------- -0.3V to 3.6V
SDZ, GAIN1, GAIN0 ---------- -0.3V to (AVDD+0.3)V
VREF---------- -0.3V to (GREG+0.3)V
Minimum Load Resistance Output Configuration ---------- 6Ω
Junction Temperature Range ---------- -40°C to 150°C
Storage Temperature Range ---------- -40°C to 125°C
Package Thermal Resistance
θ_{JA} (Note 3) ---------- 70°C/W
θ_{JC} ---------- 35°C/W

Recommended Operating Conditions

Supply Voltage Range ---------- 5.5V to 16V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(T_A =25°C, V_{DD}=12V, R_L=8Ω, Gain=26dB, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Characteristics						
AVDD, PVDD	V_{DD}		5.5		16	V
Quiescent Supply Current	I_Q	SDZ=1, no load or filter (Note 4)		10.7		mA
		SDZ=0, no load or filter		62	82	μA
High-level Input Voltage	V_{IH}	SDZ, GAIN1, GAIN0	2.05			V
Low-level Input Voltage	V_{IL}	SDZ, GAIN1, GAIN0			0.65	V
Low-level Output Voltage (Note 4)	V_{OL}	FAULTZ, $R_{PULL-UP}$=100kΩ, PVDD=16V		0.63		V
High-level Input Current	I_{IH}	GAIN1, GAIN0, V_I= 2V	-0.1		0.1	μA
		SDZ, V_I= 2V	1	3	4	μA
Drain-source On-state Resistance	$R_{DS(ON)}$			300		mΩ
Gain	G	GAIN0=0, GAIN1=0, No Load	19	20	21	dB
		GAIN0=1, GAIN1=0, No Load	25	26	27	
		GAIN0=0, GAIN1=1, No Load	31	32	33	
		GAIN0=1, GAIN1=1, No Load	35	36	37	
Turn-on Time (Note 4)	t_{ON}	SDZ=1		24		ms
Turn-off Time (Note 4)	t_{OFF}	SDZ=0		1		μs
Output Offset Voltage	$\|V_{OS}\|$	V_I=0V, Measured Differentially at VDD=6V		1.5	15	mV
Gate Drive Supply	GREG	SDZ=1, V_I=0V	3.2	3.4	3.6	V
PWM Frequency (Note 4)	f_{PWM}			350		kHz
AC Characteristics (Note 4)						
Output Integrated Noise	V_n	20Hz to 22kHz, A-weighted filter, Gain=20dB		70		μV
Signal to Noise Ratio	SNR	Max output at THD+N<1%, V_{DD}=6V,f=1kHz,Gain=20dB,		94		dB

		A-weighted				
		Max output at THD+N<1%, V_{DD}=8V,f=1kHz,Gain=20dB, A-weighted		97		
		Max output at THD+N<1%, V_{DD}=12V,f=1kHz,Gain=20dB, A-weighted		100.5		
Total Harmonic Distortion +Noise	THD+N	V_{DD}=6V, f=1kHz, Po=0.5W		0.05		%
		V_{DD}=6V, f=1kHz, Po=1W		0.055		
		V_{DD}=8V, f=1kHz, Po=1W		0.05		
		V_{DD}=8V, f=1kHz, Po=1.6W		0.055		
		V_{DD}=12V, f=1kHz, Po=1W		0.05		
		V_{DD}=12V, f=1kHz, Po=3.5W		0.05		
Output Power	P_O	V_{DD}=6V, f=1kHz, 1% THD+N		1.85		W
		V_{DD}=6V, f=1kHz, 10% THD+N		2.3		
		V_{DD}=8V, f=1kHz, 1% THD+N		3.25		
		V_{DD}=8V, f=1kHz, 10% THD+N		4		
		V_{DD}=12V, f=1kHz, 1% THD+N		7		
Crosstalk		Vo=1Vrms, f=1kHz, Gain=20dB		-90		dB
Power Supply Rejection Ratio	PSRR	200mV_{PP} ripple, f=1kHz , Gain=20dB		-60		dB
Protection						
V_{DD} Under Voltage Lockout Voltage	V_{UVLO_RISE}	V_{DD} Rising		5.25	5.5	V
	V_{UVLO_FALL}	V_{DD} Falling	4.75	5		V
V_{DD} Over Voltage Lockout Voltage	V_{OVLO_RISE}	V_{DD} Rising		21	22	V
	V_{OVLO_FALL}	V_{DD} Falling	16.9	17.7		V
Short Circuit Protection Current Limit(Note 4)	I_{SC}			4		A
Thermal Shutdown Temperature(Note 4)	T_{SD}			135		°C
Thermal Shutdown Hysteresis(Note 4)	T_{HYS}			30		°C

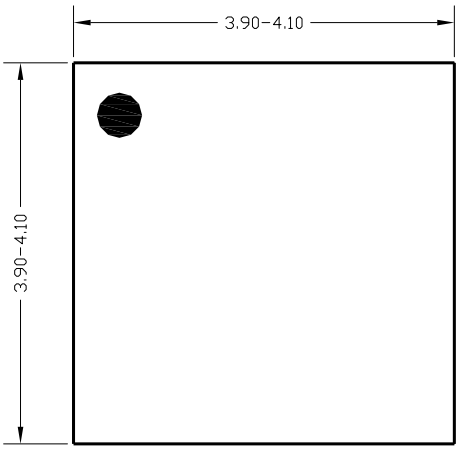
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: DC voltage rating could be derated a little according to the possible switching spike on switching node if the snubber is not appropriate enough.

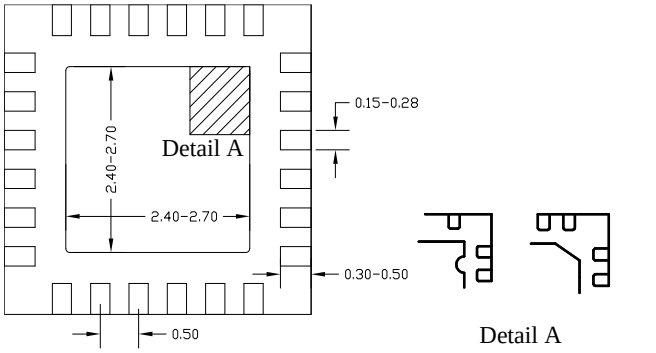
Note 3: θ_{JA} is measured in the natural convection at T_A=25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4: Typical value tested on demonstration board is guaranteed by design.

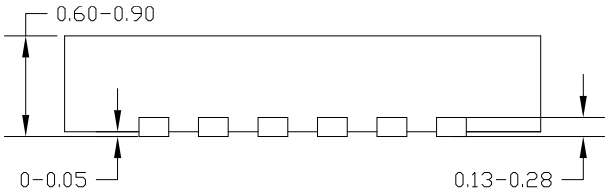
QFN4×4-24 Package Outline & PCB Layout



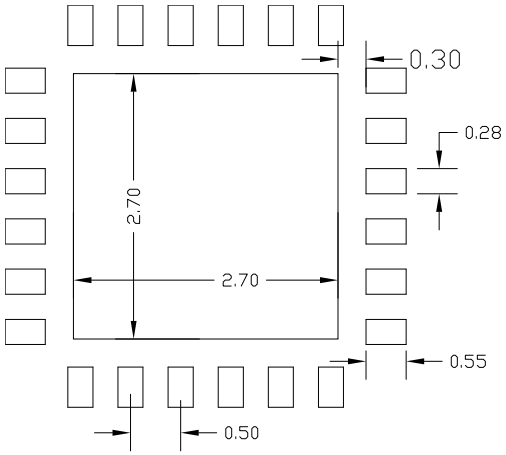
Top View



Bottom View



Side View



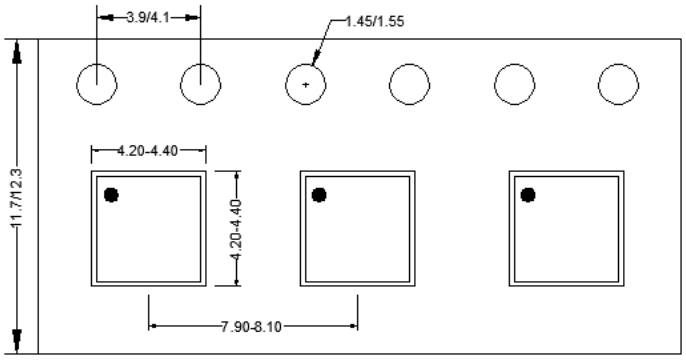
PCB Layout (Recommended)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

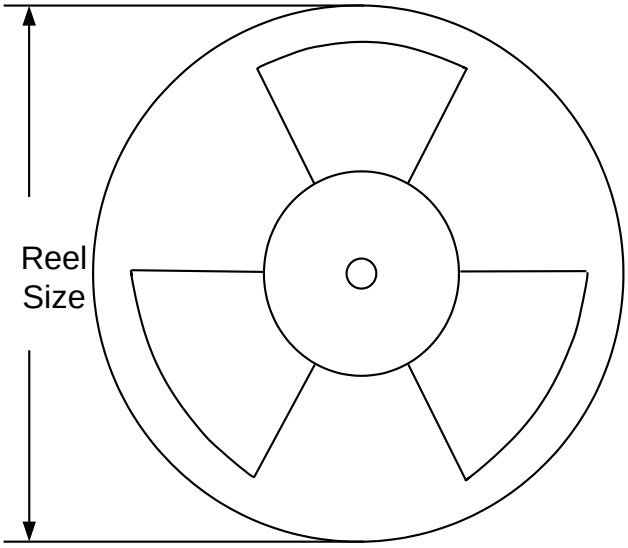
1. Taping orientation

QFN4×4



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.11, 2022	Revision 1.0	Production Release
Mar.11, 2021	Revision 0.9A	Change the pin3 from PLIMIT to VREF and delete the description of PLIMIT.
Nov. 2, 2017	Revision 0.9	Initial Release

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