SY21061F

High Efficiency, 300kHz, 36V Input, 1.2A Asynchronous Step Down Regulator

General Description

The SY21061F is a high efficiency 300kHz, adaptive constant OFF time controlled asynchronous step-down DC/DC regulator capable of delivering 1.2A output current respectively. The SY21061F can operate over a wide input voltage range from 9V to 36V and integrates the main switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with 300kHz switching frequency.

Features

- 9-36V Input Voltage Range
- Low $R_{DS(ON)}$ for Internal N-channel Power FET: 180 mΩ
- 300kHz Switching Frequency
- Adaptive Constant OFF Time Control
- Internal Soft-start Limits the Inrush Current
- 2% 0.81V Reference
- RoHS Compliant and Halogen Free
- Compact Package: SOT23-6

Ordering Information

SY21061 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21061FABC	SOT23-6	--

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Applications

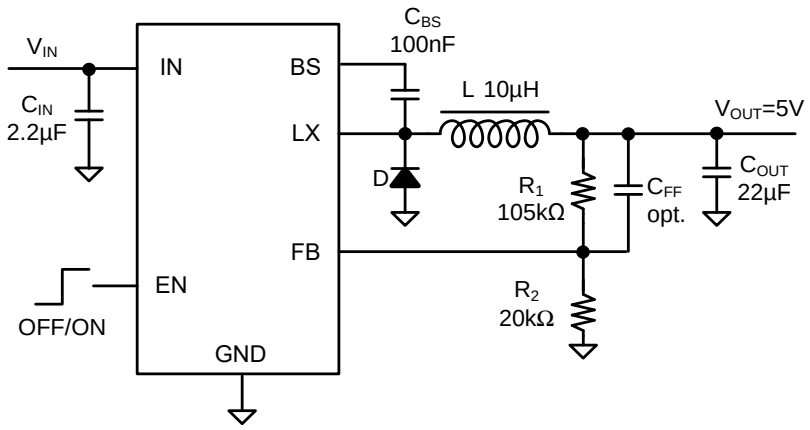
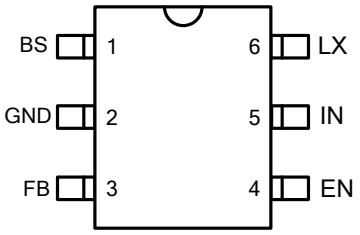


Figure1. Schematic Diagram

Pinout (top view)



(SOT23-6)

Top Mark: qR*xyz* (Device code: qR, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Decouple this pin to the LX pin with a 0.1μF ceramic capacitor.
GND	2	Ground pin.
FB	3	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.81\times(1+R_1/R_2)$
EN	4	Enable control. Pull high or leave this pin floating to turn on the IC, pull low to turn off the IC.
IN	5	Input pin. Decouple this pin to the GND pin with at least a 2.2μF ceramic capacitor.
LX	6	Inductor pin. Connect this pin to the switching node of the inductor.

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 40V
EN Voltage---------- -0.3V to V_{IN}+0.6V
FB, BS-LX Voltage---------- -0.3V to 3.6V
LX Voltage ---------- -0.7V to VIN + 0.6V
Power Dissipation, P_D @ T_A = 25°C, SOT23-6---------- 0.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 170°C/W
θ_{JC} ---------- 130°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX voltage in 20ns Duration ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 9V to 36V
Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 5V, L=10μH, C_{OUT} =22μF, T_A = 25°C, I_{OUT} = 0.5A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		9		36	V
Input UVLO Threshold	V_{UVLO}	Rising	7.5	8	8.5	V
Input UVLO Threshold		Falling	5.5	6	6.5	V
Input UVLO Hysteresis	V_{UVLO_HYS}			2		V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		160		μA
Shutdown Current	I_{SHDN}	EN=0			10	μA
Feedback Reference Voltage	V_{REF}		0.794	0.81	0.826	V
FB Input Current	I_{FB}	V_{FB}=3V	-50		50	nA
Power FET RON	$R_{DS(ON)1}$			180		mΩ
Power FET Current Limit	I_{LIM}	V_{FB}=V_{REF}×98%	1.5		2.2	A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Minimum OFF Time	t_{OFF}				100	ns
Minimum ON Time	t_{OFF}				100	ns
Soft-start Time	t_{SS}			650		μs
Oscillator Frequency	f_{OSC}		240	300	360	kHz
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Recovery Hysteresis	T_{HYS}			50		°C

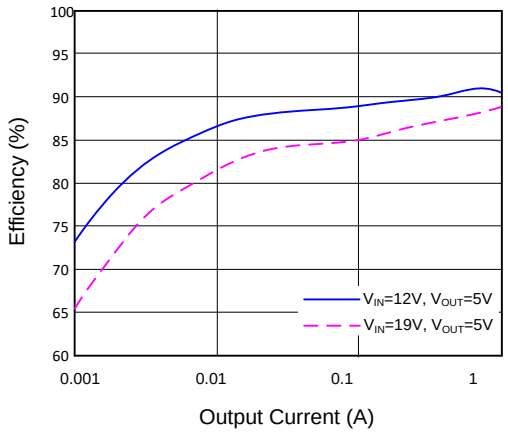
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

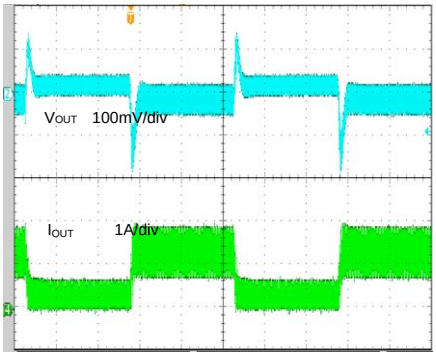
Typical Performance Characteristics

Efficiency vs Output Current



Load Transient Response

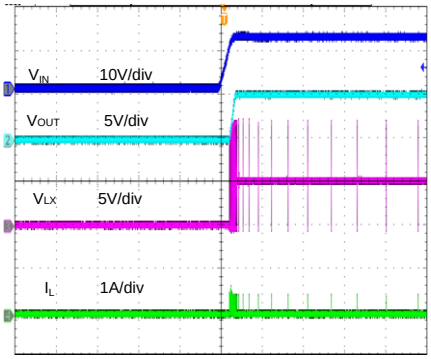
(V_{IN}=12V,V_{OUT}=5V I_{OUT}=0.12~1.2A)



Time (200μs/div)

Startup from V_{IN}

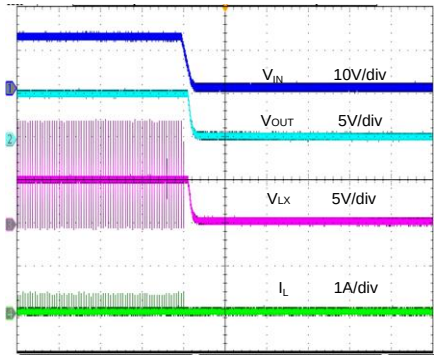
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (4ms/div)

Shutdown from V_{IN}

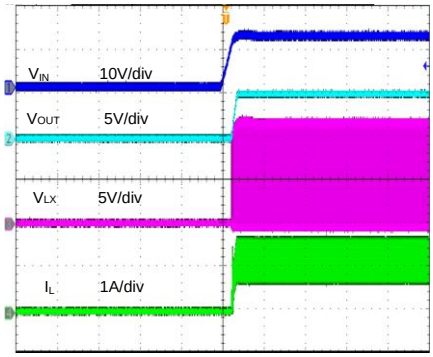
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (100ms/div)

Startup from V_{IN}

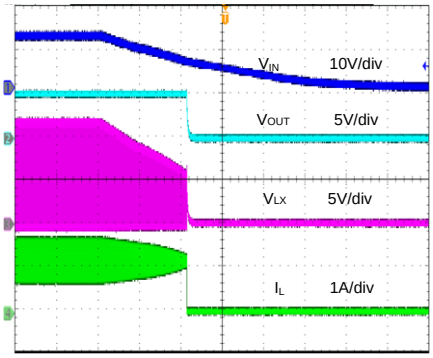
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.2A)



Time (4ms/div)

Shutdown from V_{IN}

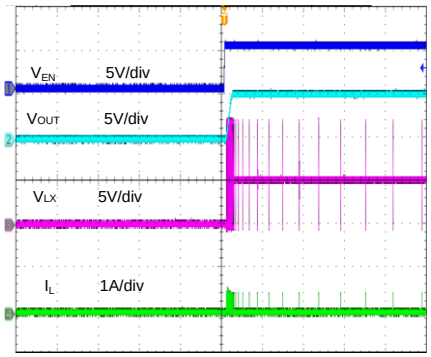
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.2A)



Time (4ms/div)

Startup from Enable

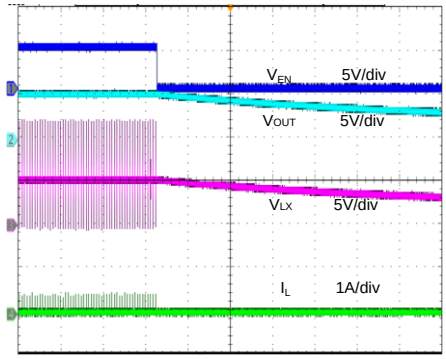
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (4ms/div)

Shutdown from Enable

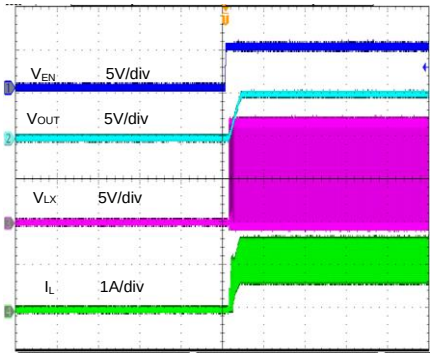
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (100ms/div)

Startup from Enable

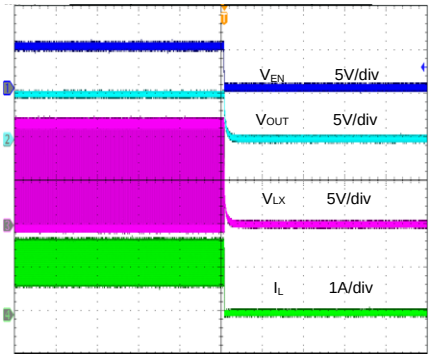
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.2A)



Time (2ms/div)

Shutdown from Enable

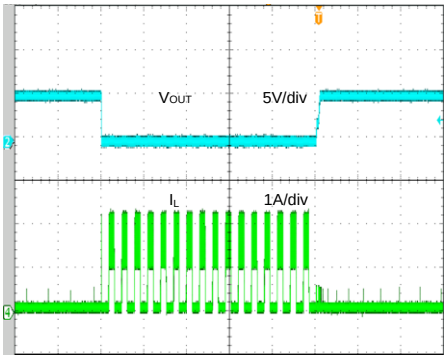
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.2A)



Time (2ms/div)

Short Circuit Protection

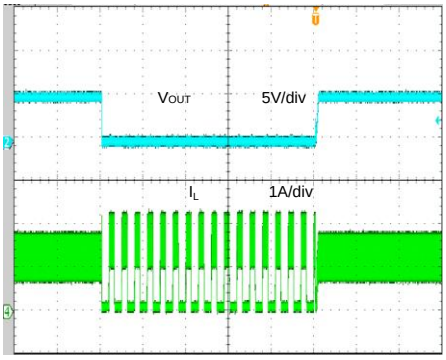
(V_{IN}=12V, V_{OUT}=5V I_{OUT}=0A~short)



Time (10ms/div)

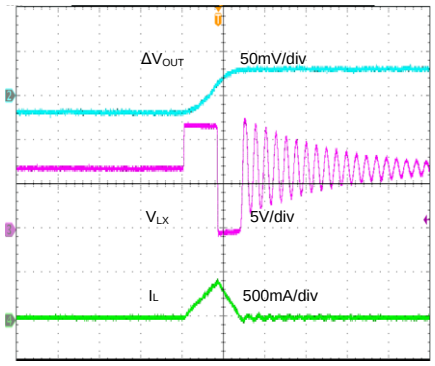
Short Circuit Protection

(V_{IN}=12V, V_{OUT}=5V I_{OUT}=1.2A~short)



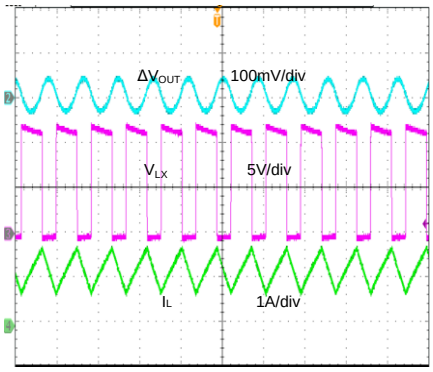
Time (10ms/div)

Output Voltage Ripple
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (1μs/div)

Output Voltage Ripple
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1.2A)



Time (4μs/div)

Operation

The SY21061F is an asynchronous Buck regulator that integrates the PWM control, a main switch on the same die. With ultra low $R_{DS(ON)}$ power switch and proprietary PWM control, this regulator can achieve high efficiency and fast transient response. High switch frequency minimizes the external inductor and capacitor size, thus minimizes the PCB area and the cost. The SY21061F also features cycle by cycle current limit, output short circuit protection and thermal shutdown protection.

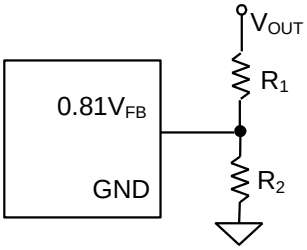
Applications Information

Because of the high integration in the SY21061F, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L, the rectifier diode D and the feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 5V, R_1=105kΩ is chosen, then using the following equation, R_2 can be calculated to be 20kΩ:

$$R_2 = \frac{0.81V}{V_{OUT}-0.81V} R_1$$



Input Capacitor C_{IN}:

The ripple current through the input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor should be placed really close to the IN pin and the negative end of the rectifier. A low ESR ceramic capacitor is recommended with greater than 2.2μF capacitance.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with greater than 22μF capacitance.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1-V_{OUT}/V_{IN,\,MAX})}{f_{SW} \times I_{OUT,\,MAX} \times 40\%}$$

Where f_{SW} is the switching frequency and $I_{OUT,\,MAX}$ is the maximum load current.

The SY21061F is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

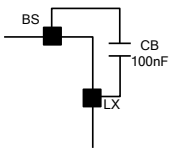
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{OUT,\,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

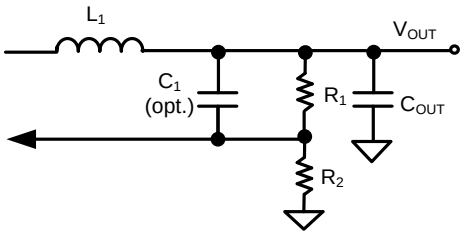


Rectifier Diode

Because of high switching speed of the SY21061F, a Schottky diode with low forward voltage and fast switching speed is desirable for the application. The voltage rating of the diode must be higher than the maximum output voltage. The diode's average and peak current rating should exceed the average output current and peak current.

Load Transient Considerations:

The SY21061F integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic capacitor in parallel with R_1 may further speed up the load transient response and is it is recommended for high step load applications.



Layout Design:

The layout design of the SY21061F is relatively simple. For the best efficiency and minimum noise problem, the following components should be placed close to the IC: C_{IN}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) The loop area formed by IN, LX, C_{IN} and the rectifier must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source, it is desirable to add a pull-down 1MΩ resistor between the EN and the GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

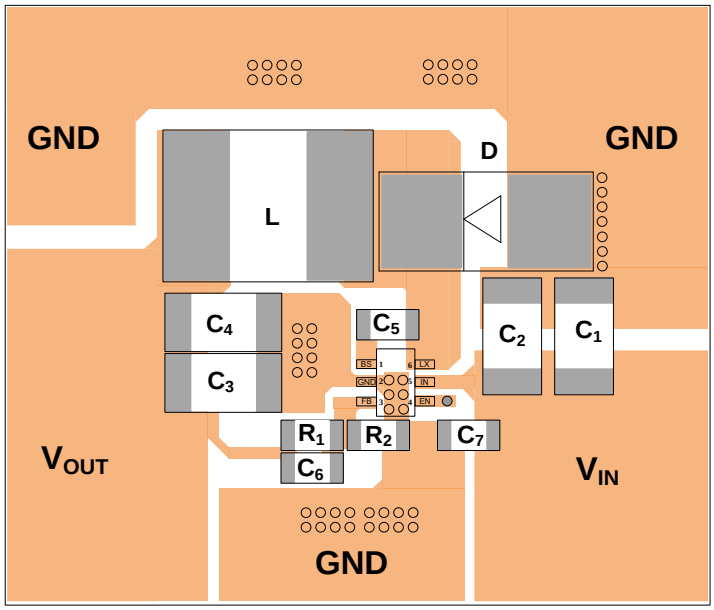
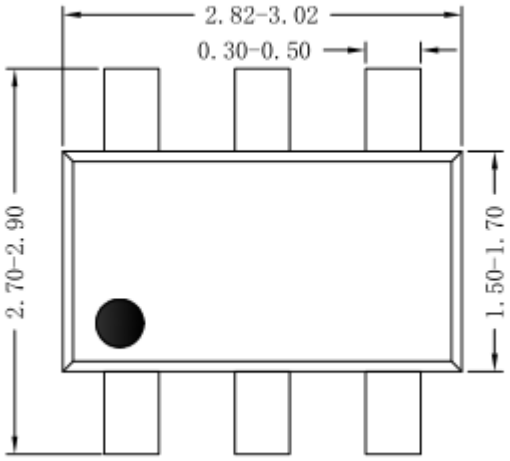
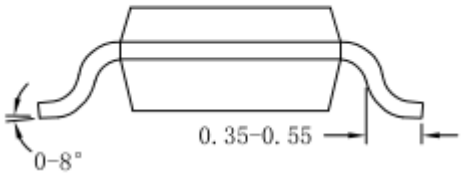


Figure3. PCB Layout Suggestion

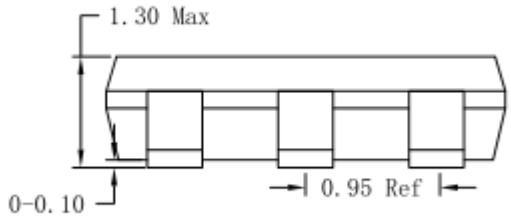
SOT23-6 Package Outline & PCB Layout Design



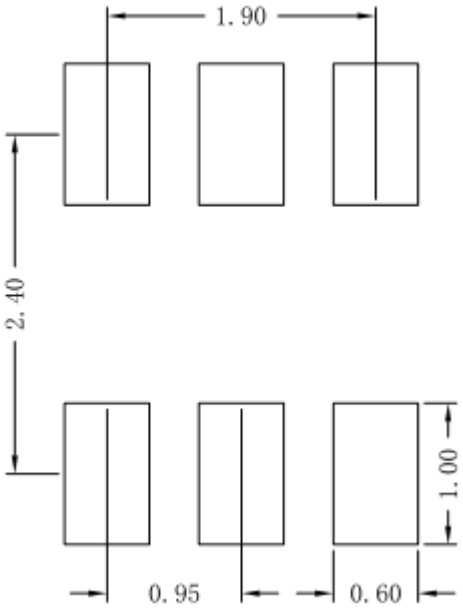
Top View



Side View



Side View

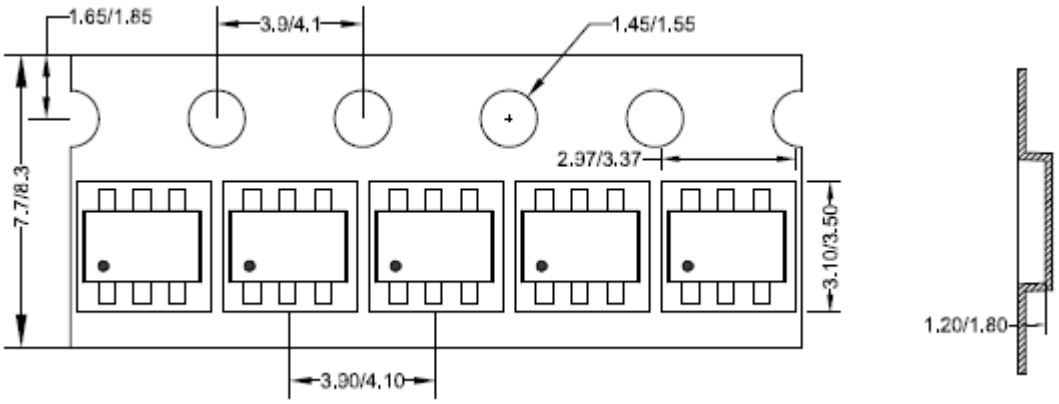


Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

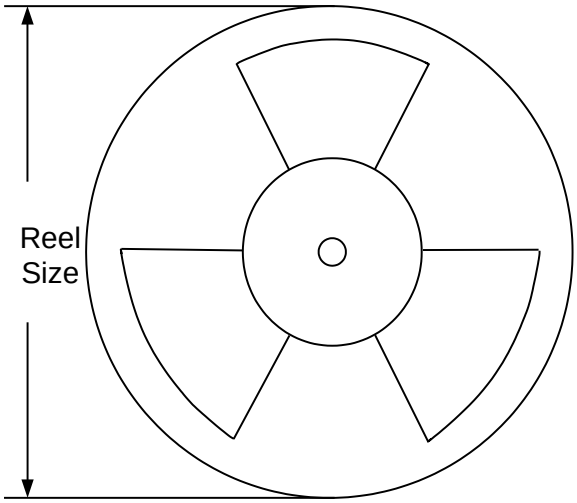
Taping & Reel Specification

1. Taping orientation for package



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

3. Others: NA

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