SY21612B

High Efficiency, 28V Input Single Inductor Synchronous Step Up/Down Regulator

General Description

The SY21612B is a high voltage Buck-Boost converter for USB power delivery applications. With user-selectable source mode and sink mode, it features bidirectional power delivery. In source mode, the output voltage V_{VBUS} is 5V, 9V, 10V, 12V, 15V, 20V selectable. In sink mode, the output voltage V_{BAT} is adjustable with an external resistor divider.

The device operates over a wide input voltage range from 4V to 28V and the maximum average inductor current is limited to a typical value of 10A. The four integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

The SY21612B integrates an I^2C compatible interface for mode selecting, output voltage setting, frequency setting, protection setting, and etc.

The device is available in compact QFN4×4-32 package.

Applications:

- Docking Station
- Laptop
- High-end Power Bank
- Monitor
- Car Charger
- USB PD

Features:

- Bidirectional Power Delivery: Source Mode and Sink Mode
- 4V to 28V Input Voltage Range
- Low $R_{DS(ON)}$ for Internal Switches: 25mΩ
- Internal Soft-start
- 8-bit ADC for Output Voltage, Input Voltage and VBUS Output Current Detection
- Fully Protected for Output Over Current, Short-circuit and Over-temperature
- I^2C Compatible Interface
  - Support Interrupt for Status Feedback
  - Selectable Switching Frequency: 250kHz, 500kHz, 750kHz, 1MHz
  - Selectable VBUS Output Voltage: 5V, 9V, 10V, 12V, 15V, 20V
  - Selectable Inductor Current Limit and VBUS Output Current Limit

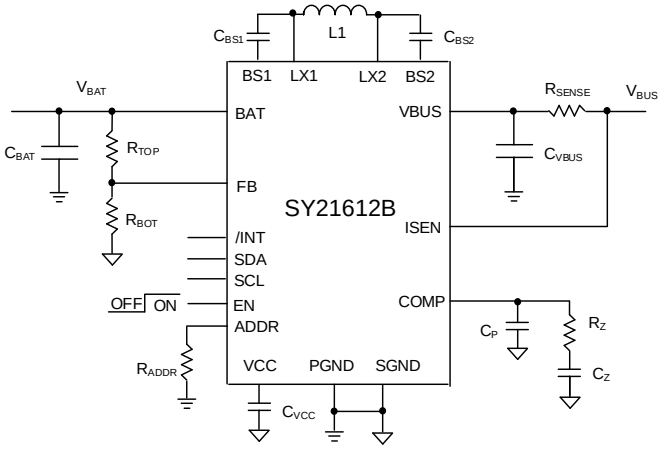


Figure1. Typical Schematic Diagram

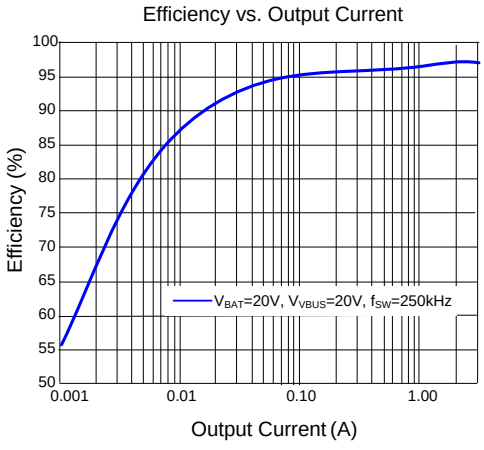


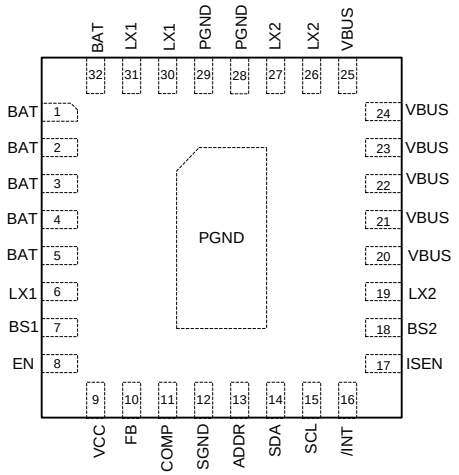
Figure2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21612BQFC	QFN4×4-32 RoHS Compliant and Halogen Free	BSZ*xyz*

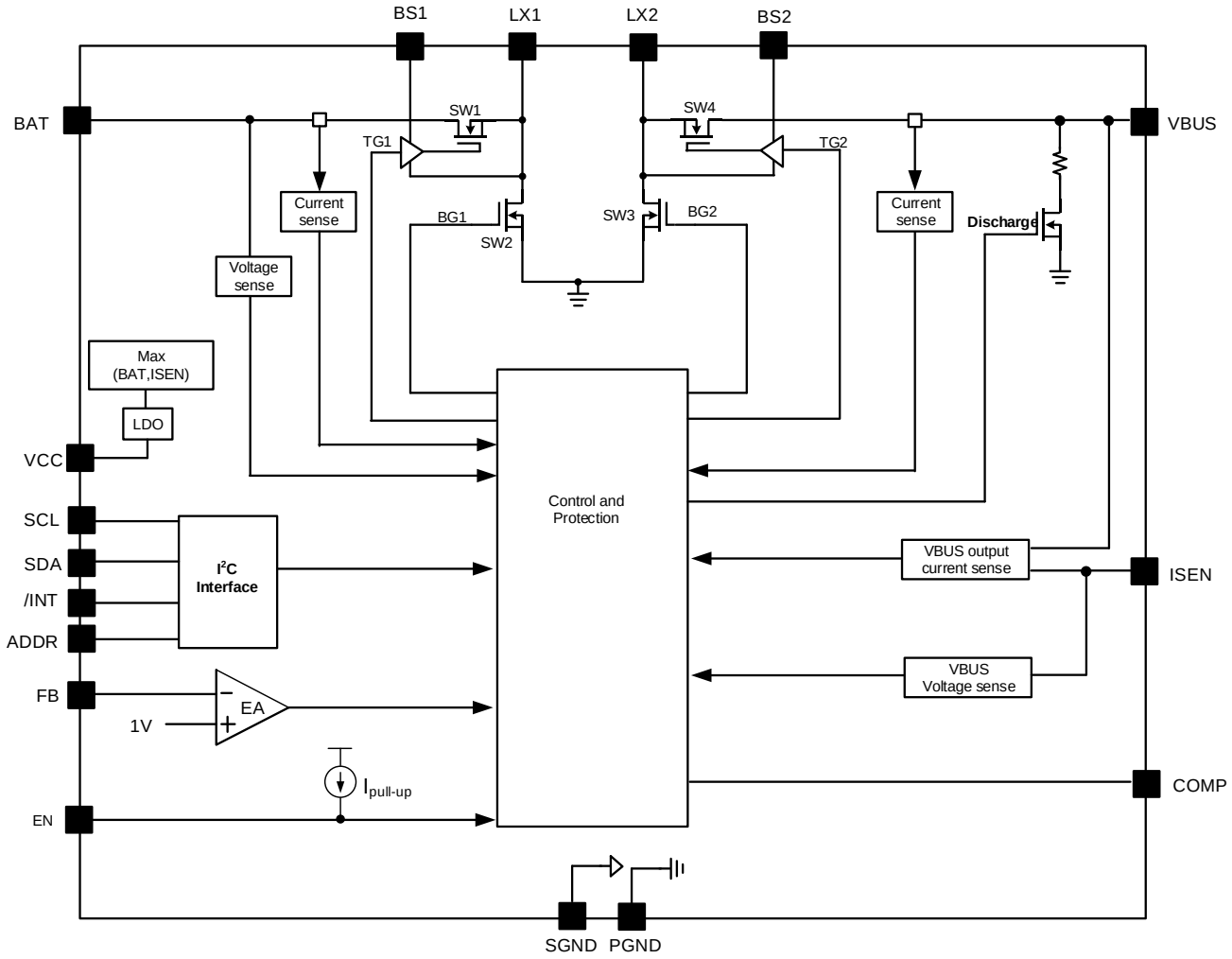
x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin Number	Description
BAT	1,2,3,4,5,32	Power input/output pin, decouple this pin to PGND with at least a 10μF ceramic capacitor. This pin is the power input in source mode and the power output in sink mode.
LX1	6,30,31	Switching node 1.
BS1	7	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS1 and the LX1 pin. Do not connect a resistor in series with the capacitor.
EN	8	IC enable control pin, logic high enable. This pin is internally pulled high by 400nA pull-up current.
VCC	9	3.3V LDO output, power supply for internal driver and control circuits. Decouple this pin to SGND with a minimum of 4.7μF ceramic capacitor.
FB	10	Sink mode output feedback pin. Connect this pin to the center point of the output resistor divider to adjust the V_{BAT} output voltage: $V_{BAT}=1V\times(R_{TOP}+R_{BOT})/R_{BOT}$.
COMP	11	Compensation pin. Connect the RC network between this pin and ground.
SGND	12	Signal ground.
ADDR	13	The device address set pin. Ground this pin to select 0x70. Connect this pin to GND with an external resistor to select 0x71(50kΩ<R_{ADDR}<100kΩ) or 0x72(400kΩ<R_{ADDR}<500kΩ). Float this pin to select 0x73.
SDA	14	I^2C interface serial data pin. Logic level input/output.
SCL	15	I^2C interface serial clock pin. Logic level input.
/INT	16	The /INT pin is an open-drain output. When an interrupt event happens, the /INT pin is internally pulled low to inform the host about fault condition. After the host reads the interrupt register, the /INT pin is externally pulled high. A 10kΩ pull-up resistor is recommended.
ISEN	17	Current sense pin. Connect a 10mΩ resistor R_{SENSE} between VBUS and ISEN to detect source mode output current.
BS2	18	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS2 and the LX2 pin. Do not connect a resistor in series with the capacitor.
LX2	19,26,27	Switching node 2.
PGND	28,29, Exposed Pad	Power ground.
VBUS	20,21,22,23, 24,25	Power input/output pin, decouple this pin to PGND with at least a 10μF ceramic capacitor. This pin is the power output in source mode and the power input in sink mode.

Block Diagram



Absolute Maximum Ratings (1)	Min	Max	Unit
BAT, LX1, LX2, VBUS, ISEN, EN, SDA, SCL, FB, COMP	-0.3	30	V
BS-LX, VCC, ADDR, /INT	-0.3	4	
LX, 50ns Duration	-5	31	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10sec.)		260	
Storage Temperature	-65	150	

Thermal Information (2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		28	°C/W
θ_{JC} Junction-to-case Thermal Resistance		2.8	
P_D Power Dissipation T_A=25°C		4	W

Recommended Operating Conditions (3)	Min	Max	Unit
BAT, VBUS	4	28	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics (V_{BAT} = 12V, V_{VBUS}=12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BAT Voltage Range	V_{BAT}		4		28	V
VBUS Voltage Range	V_{BUS}		4		28	V
LDO Voltage	VCC	I_{LDO}=50mA	3.12	3.3	3.37	V
LDO Current Limit	I_{LMT_LDO}			100		mA
LDO Dropout Voltage	$V_{DROPOUT}$	I_{LDO}=50mA		250		mV
Quiescent Current	I_Q	No switching		310	410	μA
Shutdown Current	I_{SD}	IC is disabled		9.6	15.5	μA
Feedback Reference Voltage	V_{REF}	Sink mode	0.97	1	1.03	V
FB Input Current	I_{FB}		-50		50	nA
VBUS Voltage Set-point	$V_{BUS,SET}$	Source mode, VBUS voltage setting register 0x01[5:3]='101'	11.82	12	12.18	V
VBUS OVP Threshold	$V_{BUS,OVP}$	VBUS OVP point 0x02[4:3]='10'		120		% $V_{BUS,SET}$
Internal Power MOSFET $R_{DS(ON)}$	$R_{DS(ON)}$			25		mΩ
Inductor Average Current Limit	I_{AVG}	0x03[7:6]='00'		6		A
		0x03[7:6]='10'		8		A
		0x03[7:6]='11'		10		A
Inductor Peak Current Limit	I_{PK}	0x03[7:6]='00'	6.8	8.8	11.1	A
		0x03[7:6]='10'	8.2	10.4	12.5	A
		0x03[7:6]='11'	10.2	13.2	15.8	A
VBUS/BAT Input UVLO Threshold	V_{UVLO}		3.3		3.7	V
UVLO Hysteresis	V_{HYS}			0.2		V
EN Logic High Threshold	V_{ENH}		1.5			V
EN Logic Low Threshold	V_{ENL}				0.5	V
VBUS Output Current Limit Voltage Threshold	$V_{BUS.ILIM}$	0x02[7:5]='000'	9	18	27	mV
		0x02[7:5]='001'	14	23	32	mV
		0x02[7:5]='010'	19	28	37	mV
		0x02[7:5]='011'	24	33	41	mV
		0x02[7:5]='100'	28	37	46	mV
		0x02[7:5]='101'	38	47	55	mV
		0x02[7:5]='110'	47	56	65	mV
		0x02[7:5]='111'	62	66	71	mV
Oscillator Frequency	f_{OSC}	0x01[7:6]='01'	425	500	575	kHz
Min On Time	t_{ON_MIN}			150		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Soft-start Time	t_{ss}	Source mode, V_{VBUS}=5V		1.5		ms
ADC Control						
ADC Resolution				8		Bits
ADC Voltage Sense Accuracy		V_{BAT}=23V	-5		5	%
ADC Current Sense Accuracy		V_{VBUS}-V_{ISEN}=71mV	-15		15	%
V_{BAT} Full Scale Range			0		25	V
V_{BUS} Full Scale Range			0		25	V
Sense Current Full Scale Range			0		71	mV
I²C COMPATIBLE INTERFACE						
Maximum Operating Frequency				400		kHz
SDA and SCL Input Logic Threshold	Logic_L				0.8	V
	Logic_H		2			V
SDA Output Low Voltage		3mA sink current			0.4	V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Function Description

I²C Compatible Interface

The SY21612B integrates an I²C compatible interface. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 400kHz ("Fast-Mode") and uses standard I²C commands. The SY21612B always operates as a slave device, and is addressed using a 7-bits slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

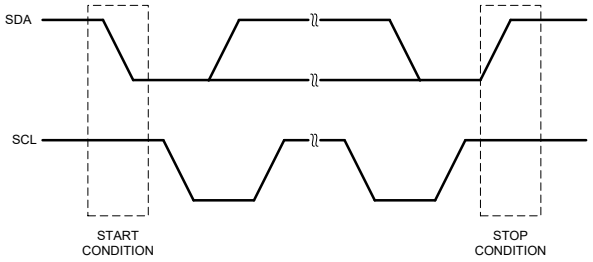
I²C Device Address

When communicating with multiple devices using the I²C interface, each device must have its own unique address so the host can distinguish among the devices. The most significant 4-bits of the device address are '1110'. The 5th, 6th and 7th-bit device address is selected by the ADDR pin.

ADDR	Device Address
ADDR short to GND	1110000
50kΩ<R_{ADDR}<100kΩ	1110001
400kΩ<R_{ADDR}<500kΩ	1110010
Floating or connect to VCC	1110011

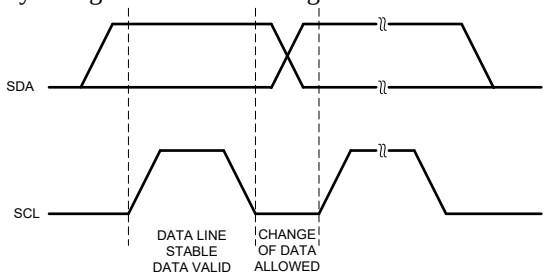
START and STOP Conditions

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.



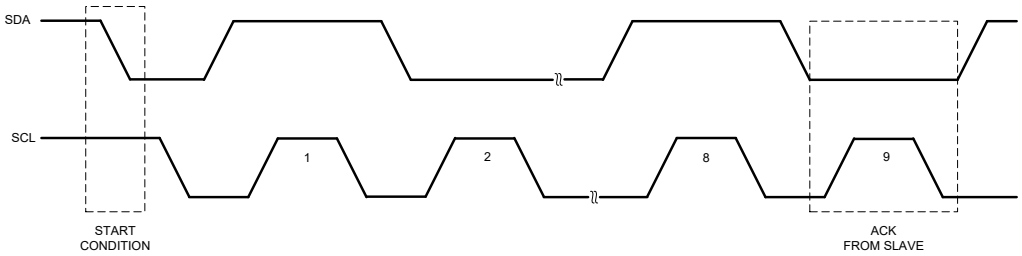
Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an $R/\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

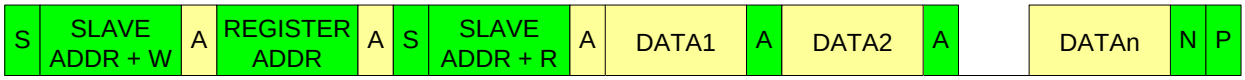


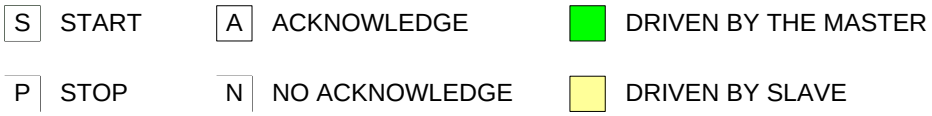
Data Transactions

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address followed by the R/W bit. The R/W bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the slave acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the slave which register the master will write or read. Once the slave receives a register address byte, it responds with acknowledge. If a STOP condition is detected after the register address byte is received, the SY21612B takes no further action but storing the register address byte. The register address byte auto increases when multiple date bytes are transited.

Write

Random Read





Register Map

Address	Data	Note
00	Control Register 1	R/W
01	Control Register 2	R/W
02	Protection setting 1	R/W
03	Protection setting 2	R/W
04	State Register	R
05	/INT Register	Read then Clear
06	BAT Voltage Value Register	R
07	VBUS Voltage Value Register	
08	VBUS Output Current Sense Voltage Register	

Control Register1 (0x00)

Name	# of Bits	Access	Default	Description
Regulator Enable	7	R/W	0	0:Disable 1:Enable
Low Battery Voltage Setting	6	R/W	0	000:10.2V[12V Car Battery] 001:10.7V[12V Car Battery] 010:11.2V [12V Car Battery] 011:11.7V [12V Car battery] 100: 22.0V [24V Car Battery] 101: 22.5V [24V Car Battery] 110: 23V [24V Car Battery] 111:23.5V [24V Car Battery]
	5	R/W	0	
	4	R/W	0	
ADC ON/OFF	3	R/W	0	0:Inactive; 1:Active
ADC Mode Select	2	R/W	0	0: Single detect mode; 1: Auto detect mode
VBUS Discharge Control	1	R/W	0	0: Active discharge when regulator is disabled 1: Inactive discharge when regulator is disabled
Reserved	0	R/W	0	

Control Register2 (0x01)

Name	# of Bits	Access	Default	Description
Switching Frequency	7	R/W	1	00: 250KHz 01: 500KHz 10: 750KHz 11: 1MHz
	6	R/W	1	
VBUS Voltage Setting	5	R/W	0	000:5V 001:5V 010:5V 011:9V 100:10V 101:12V 110:15V 111: 20V If 0x00[7]='0', this bit is reset to '0' and cannot be overwritten
	4	R/W	0	
	3	R/W	0	
VBUS Voltage Adjust	2	R/W	0	000: -2.5% 001: -1.25% 010: ±0% 011: +1.25% 100:+2.5% 101: +3.75% 110:+5% 111:+6.25%
	1	R/W	1	
	0	R/W	0	

Protection setting 1 (0x02)

Name	# of Bits	Access	Default	Description
VBUS Output Current Limit Voltage Threshold (Source mode)	7:5	R/W	011	000: 18mV 001: 23mV 010: 28mV 011: 33mV 100: 37mV 101: 47mV 110: 56mV 111: 66mV
VBUS OVP Threshold	4	R/W	1	00:110% $V_{BUS,SET}$ 01:115% $V_{BUS,SET}$ 10:120% $V_{BUS,SET}$ 11:125% $V_{BUS,SET}$
	3	R/W	0	
VBUS UVP Threshold	2	R/W	1	00:50% $V_{BUS,SET}$ 01:60% $V_{BUS,SET}$ 10:70% $V_{BUS,SET}$ 11:80% $V_{BUS,SET}$
	1	R/W	0	
Reserved	0	R/W	0	

Protection setting 2 (0x03)

Name	# of Bits	Access	Default	Description
Inductor Average Current Limit Setting	7	R/W	0	00: 6A 01: 6A 10: 8A 11: 10A
	6	R/W	0	
Inductor Average Current Limit Protection Mode	5	R/W	0	0: Latch off: 0x00[7] is reset to '0' 1: Auto recover: 0x01[5:3] is reset to '000'
VBUS Under Voltage Protection Mode	4	R/W	0	0: Latch off: 0x00[7] is reset to '0' 1: Auto recover: hiccup mode, 0x01[5:3] is reset to '000'
Over Temperature Protection Mode	3	R/W	0	0: Latch off: 0x00[7] is reset to '0' 1: Auto recover, 0x01[5:3] is reset to '000'
Bidirectional Mode	2	R/W	0	0: Source mode 1: Sink mode If 0x00[7]='0', this bit is reset to '0' and cannot be overwritten
Reserved	1	R/W	0	
Reserved	0	R/W	0	

State Register (0x04)

Name	# of Bits	Access	Description
Power Good State	7	R	0: Power is not in good range 1: Power good (feedback is 90%~120% Vref)
BAT/VBUS Voltage Relation	6	R	0:BAT voltage > VBUS voltage 1: BAT voltage < VBUS voltage
BAT Power State	5	R	0: Normal 1: Low BAT voltage
Reserved	4:0	R	

Interrupt Register (0x05)

Name	# of Bits	Access	Description
ADC Data Ready	7	Read then Clear	0: None 1: Data ready
VBUS Over Current Limit	6	Read then Clear	0: Normal 1:VBUS output current OCP
Inductor Current Protection	5	Read then Clear	0: Normal 1: Inductor OCP
VBUS UVP	4	Read then Clear	0: Normal 1:UVP
Over Temperature Protection	3	Read then Clear	0: Normal 1: OTP
Reserved	2:0	Read then Clear	

BAT Voltage Register (0x06)

Name	# of Bits	Access	Description
BAT Voltage Value	7:0	R	00000000: 0V 00000001: 0.098V …… 11111111: 25V

VBUS Voltage Register (0x07)

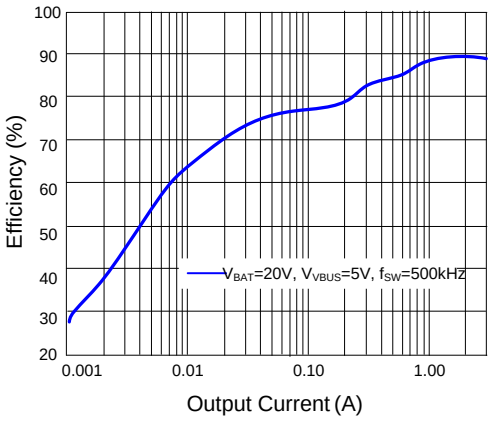
Name	# of Bits	Access	Description
VBUS Voltage Value	7:0	R	00000000: 0V 00000001: 0.098V …… 11111111: 25V

VBUS Output Current Sense Voltage Register (0x08)

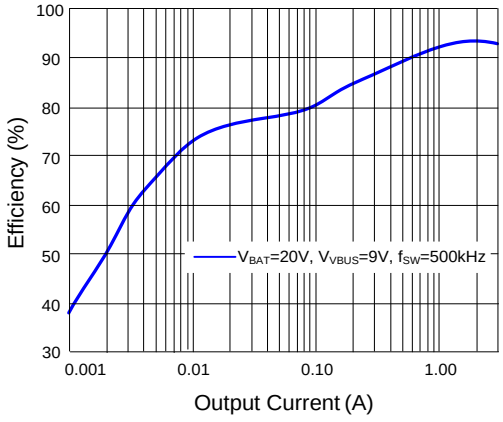
Name	# of Bits	Access	Description
VBUS Output Current Sense Voltage	7:0	R	00000000: 0mV 00000001: 0.278mV …… 11111111: 71mV

Typical Performance Characteristics

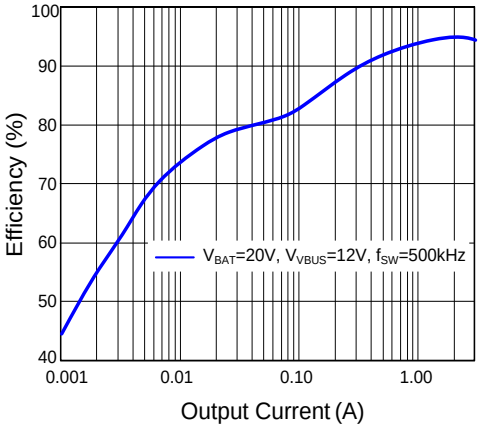
Efficiency vs. Output Current



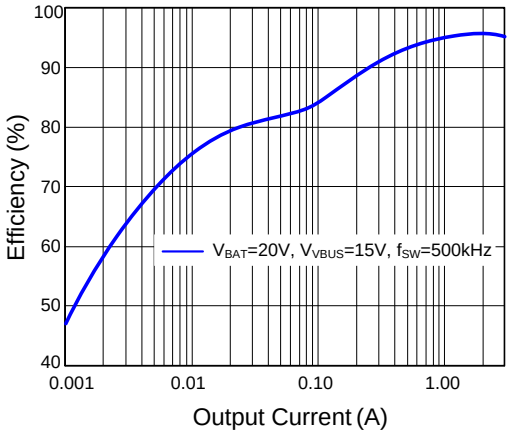
Efficiency vs. Output Current



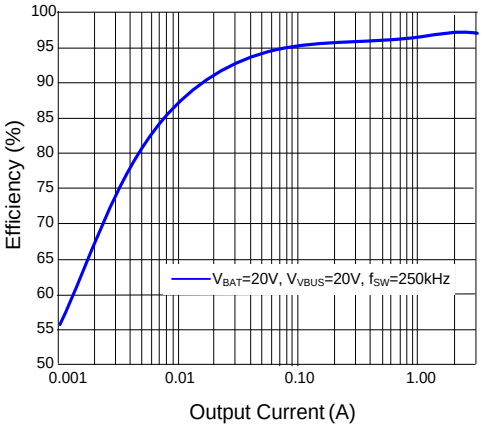
Efficiency vs. Output Current



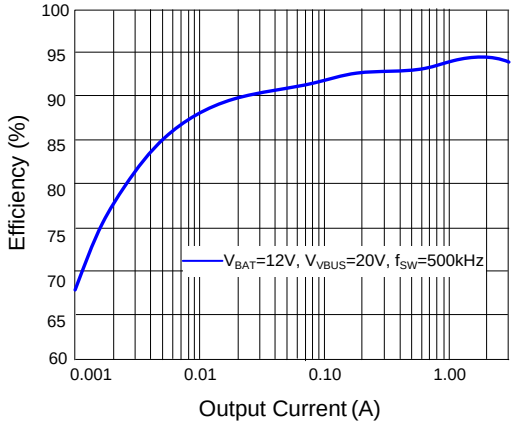
Efficiency vs. Output Current



Efficiency vs. Output Current

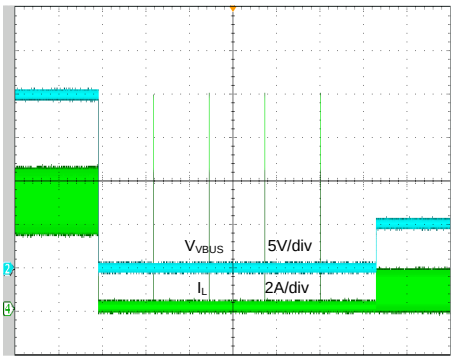


Efficiency vs. Output Current



Short Circuit Test (Auto Recover)

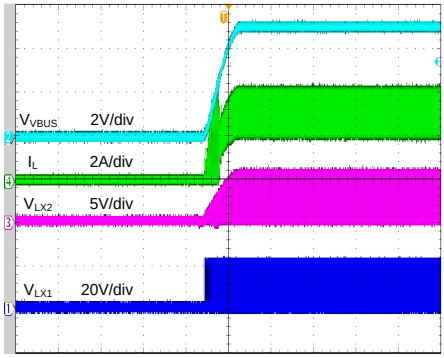
(V_{BAT}=20V,V_{VBUS}=20V,R_{LOAD}=6.7Ω)



Time (2s/div)

Regulator Enable

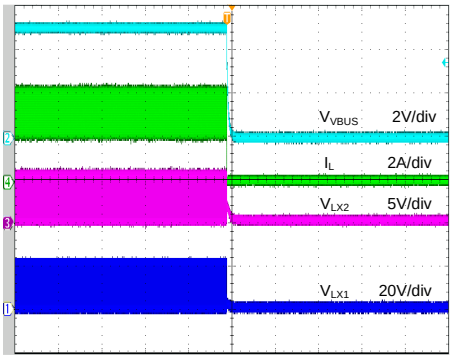
(V_{BAT}=20V,V_{VBUS}=5V,I_{LOAD}=3A)



Time (2ms/div)

Regulator Disable

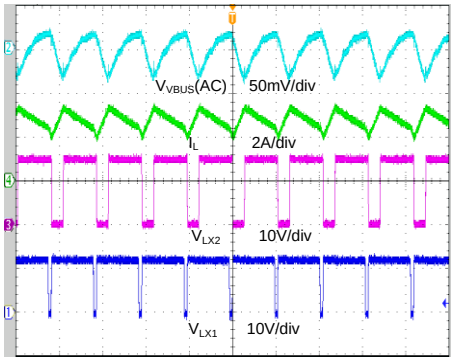
(V_{BAT}=20V,V_{VBUS}=5V,I_{LOAD}=3A)



Time (2ms/div)

Output Ripple

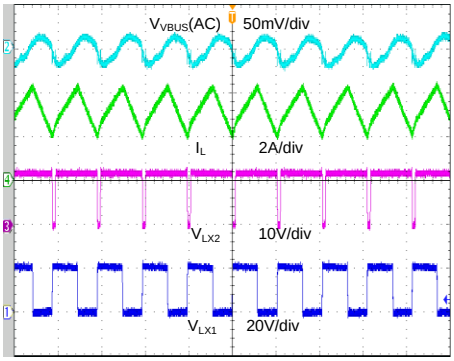
(V_{BAT}=12V,V_{VBUS}=15V,I_{LOAD}=2A)



Time (2μs/div)

Output Ripple

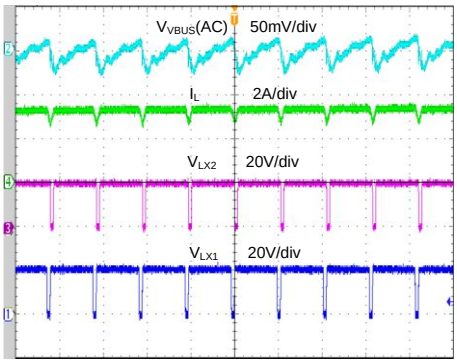
(V_{BAT}=20V,V_{VBUS}=12V,I_{LOAD}=3A)



Time (2μs/div)

Output Ripple

(V_{BAT}=20V,V_{VBUS}=20V,I_{LOAD}=3A)



Time (2μs/div)

Application Information

Input Under-voltage Lock-out

To prevent operation before all internal circuitry is ready and to ensure that the power and synchronous rectifier switches may be sufficiently enhanced, the IC incorporates input under-voltage lock-out (UVLO) protection. The device remains in a low current state and all switching is inhibited until V_{IN} exceeds V_{UVLO}, the input UVLO (rising) threshold. At that time, if EN is enabled, the device will start-up by initiating a soft-start ramp. If V_{IN} falls below V_{UVLO} less the UVLO hysteresis, switching will be suppressed again.

Bidirectional Buck-Boost Regulator Operation Mode

The SY21612B is a bidirectional device which can be operated under both source mode and sink mode. 0x03[2]='0' selects source mode while 0x03[2]='1' selects sink mode.

Under source mode, which is also the default mode, the BAT pin is connected to the power input and the VBUS pin is the power output. The output voltage V_{VBUS} is configured by 'VBUS Voltage Setting' register 0x01[5:3]. Once the 'Regulator Enable' bit is cleared (0x00[7]='0'), operation mode will be reset to source mode(0x03[2] is reset to '0' and cannot be overwritten).

Under sink mode, the VBUS pin is connected to the power input, the BAT pin is the power output and the FB pin is the feedback input. The output voltage V_{BAT} is programmed by external voltage divider (see Figure3) with the 1V internal voltage reference as given in equation (1).

$$V_{BAT}=1V\times\frac{R_{TOP}+R_{BOT}}{R_{BOT}} \qquad (1)$$

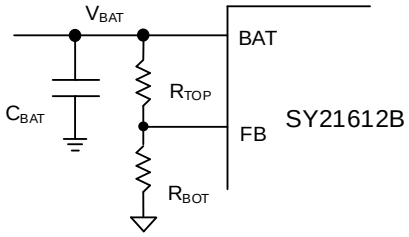


Figure3. Schematic of V_{BAT} under Sink Mode

Interrupt

When an interrupt event happens, the open-drain /INT pin is pulled low to inform the host. After the host reads the interrupt register, the /INT pin will be pulled high by an external pull-up resistor.

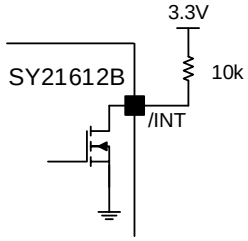


Figure4. Description of Interrupt Function

External Bootstrap Capacitor Connection

This device integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 100nF low ESR ceramic capacitor to be connected between BS1 and LX1, BS2 and LX2. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel power MOSFET switch. Do not connect a resistor in series with the bootstrap capacitor.

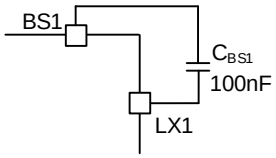


Figure5. External Bootstrap Capacitor Connection

VCC Linear Regulator

An internal 3.3V linear regulator (VCC) provides the power supply for the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a minimum of 1μF low ESR ceramic capacitor from VCC to SGND.

Under Voltage Protection

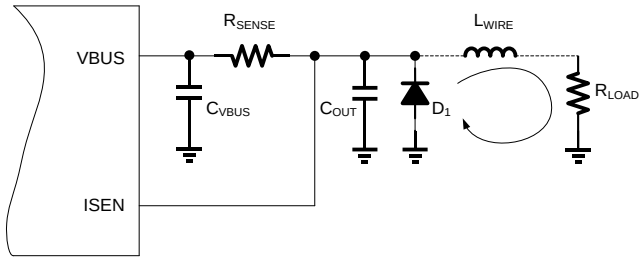
The SY21612B activates UVP (under voltage protection) function when output short occurs. There are two UVP protection modes. One is latch off operation by setting 0x03[4]='0', the other is auto recover operation with 0x03[4]='1'.

Latch off Operation: Once the output voltage is lower than UVP threshold for 1ms, the regulator will be disabled (0x00[7]='0').

Auto Recover Operation (Hiccup Mode): When output voltage is lower than UVP threshold for 1ms, the device will shut down for approximately 2.6s. The device will then restart with a complete soft-start cycle. If the short circuit condition remains another 'hiccup' cycle of shutdown and restart will continue indefinitely unless the OTP threshold is reached.

In applications where the wire length from the output of the SY21612B to the load is relative long, the parasitic inductance of the wire, L_{WIRE}, can't be neglected. If short circuit event happens on the load side, the energy stored in the L_{WIRE} will reversely charge the output capacitor, and cause high negative voltage on C_{OUT}. This may cause potential risk to the safe operating of the IC when negative voltage exceeds -0.7V. To avoid this happening, a Schottky diode in parallel with C_{OUT} can

be used as shown below. Same solution can be employed when the IC works under sink mode, and the BAT will be shorted.



Average Inductor Current Limit

When average inductor current is greater than the threshold, the internal control loop will regulate the average inductor current by decreasing duty cycle. Both latch off operation and auto recover operation are provided by the device: 0x03[5]='0' enters latch off operation, and 0x03[5]='1' enters auto recover operation.

Latch off Operation: When average inductor current exceeds a certain threshold for 1ms, the regulator will be disabled (0x00[7]='0').

Auto Recover Operation: The device will regulate the average inductor current to the setting value. The IC resumes normal operation when the fault condition is removed.

VBUS Output Current Limit

The SY21612B provides a function for VBUS output current limit by sensing the voltage drop between VBUS pin and ISEN pin (as shown in figure5). Once the voltage difference (V_{VBUS}-V_{ISEN}) exceeds the voltage threshold, which can be configured by register 0x02[7:5], the internal control loop will regulate the output current by decreasing duty cycle until UVP or OTP is triggered. Noticing that the effects of R_{PIN} and R_{WIRE} cannot be ignored, the actual limit current I_{LIMIT} can be calculated as given in Equation (2):

$$I_{LIMIT}=\frac{V_{VBUS}-V_{ISEN}}{R_{SENSE}+R_{PIN}+R_{WRIE}} \quad (2)$$

where $R_{PIN}\approx 1.65m\Omega$.

R_{WIRE} depends on PCB layout.

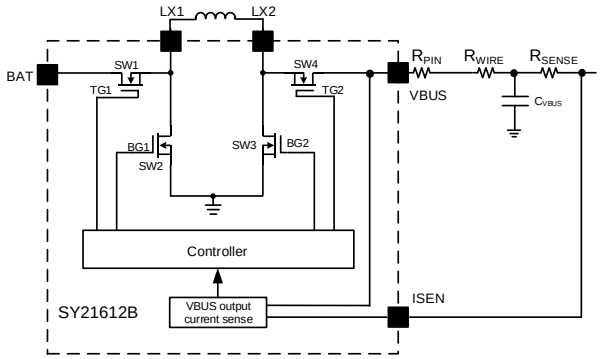


Figure6. Description of VBUS Output Current Limit

Note: The VBUS output current limit only functions under source mode, after finishing soft-start.

Over Temperature Protection

The device provides two protection modes for OTP (over temperature protection). If 0x03[5]='0', it selects latch off operation , and if 0x03[3]='1' , it is auto recover operation

Latch off Operation: The regulator will be disabled when the junction temperature exceeds 150°C.

Auto Recover Operation: The regulator stops switching when the junction temperature exceeds 150°C. Once the junction temperature falls below 135°C, the device will resume operation.

Device Enable

When the device is enabled, LDO is turned on, and then I^2C interface is fully functional. The device can be enabled when BAT voltage is above 3.5V and EN voltage is greater than 1.2V, or VBUS voltage exceeds 3.5V (see Figure6). To disable the device, the regulator should be disabled through I^2C first, and then the device will automatically discharge VBUS. After VBUS falls below 3.5 V, pulled EN low to totally disable the device.

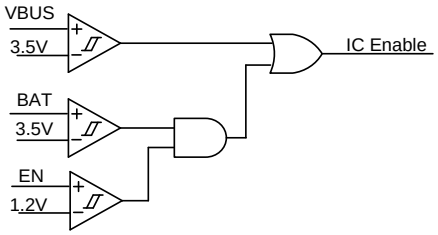


Figure7. Description of the IC Enable Function

Input Capacitor CIN

In the buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitor is calculated as:

$$I_{CIN\_RMS}=I_{OUT}\times\sqrt{D\times(1-D)} \quad (3)$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. For most applications, at least a 22µF low ESR ceramic capacitor is recommended.

Output Capacitor COUT

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For most applications, it is recommended to use more than 30µF capacitance with X5R or better grade ceramic capacitor. The capacitance derating with DC voltage must be considered.

Inductor Selection

For the Buck-Boost converter, the inductor must support buck applications with the maximum input voltage and boost applications with the minimum input voltage. The critical inductance values for buck mode is calculated with Equation (4):

$$L_{BUCK} = \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times \Delta I_L} \quad (4)$$

Where ΔI_L is the peak-to-peak inductor ripple current, and it is about 30% to 50% of the maximum output current.

The critical inductance for boost mode is calculated with Equation (5) and Equation (6):

$$L_{BOOST} = \frac{V_{IN,MIN} \times (V_{OUT} - V_{IN,MIN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (5)$$

$$I_{IN,MAX} = \frac{V_{OUT} \times I_{OUT}}{V_{IN,MIN} \times \eta} \quad (6)$$

Where η is the efficiency, and ΔI_L is the peak-to-peak inductor ripple current, it is about 30% to 50% of the maximum input current ($I_{IN,MAX}$). The recommended minimum inductor values are either L_{BUCK} or L_{BOOST} whichever is higher.

In addition to the inductance value, the inductor must support the peak current based on Equation (14) and Equation (15) to avoid saturation:

$$I_{PEAK-BUCK} = I_{OUT} + \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L} \quad (7)$$

$$I_{PEAK-BOOST} = \frac{V_{OUT} \times I_{OUT}}{V_{IN,MIN} \times \eta} + \frac{V_{IN,MIN} \times (V_{OUT} - V_{IN,MIN})}{2 \times V_{OUT} \times f_{SW} \times L} \quad (8)$$

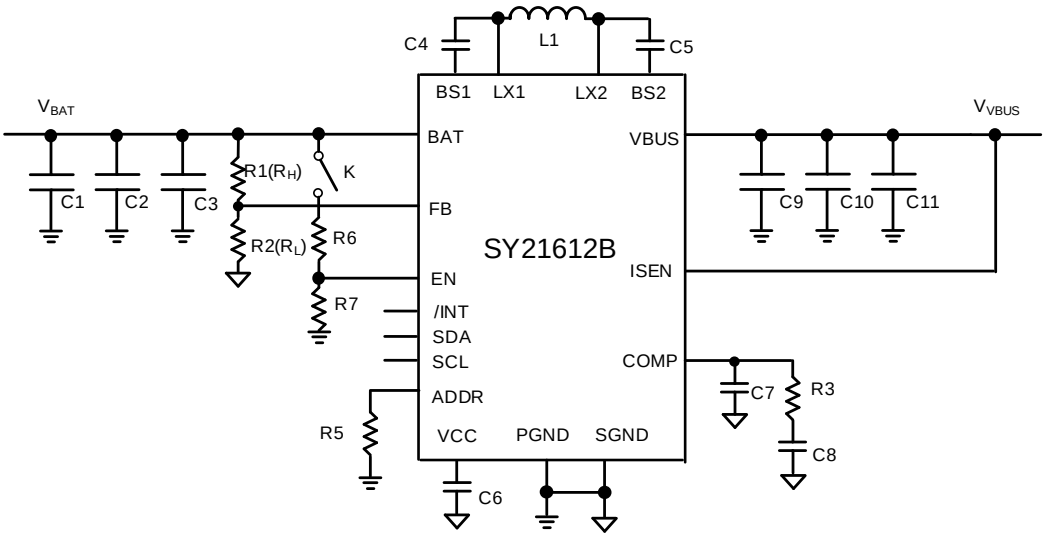
Choosing a larger inductance reduces the ripple current but also increase the size of the inductor and reduces the achievable bandwidth of the converter by moving the right half-plane zero to lower frequency. The appropriate balance should be chosen based on the application requirements

Loop compensation

The IC incorporates an average current mode control strategy. The average current mode control strategy has two feedback loops. The inner loop is voltage loop, which
compensation components will be adjusted automatically with frequency setting. The outer loop is current loop, which is compensated with external components. The external components designed for stability consideration, a fixed compensation network is recommended: 10k and 2.2nF in series from COMP pin to SGND, and a 4.7~10pF capacitor in parallel at same time.

Typical Design

Typical Schematic



Design Specifications

Mode	Input Voltage (V)	Output Voltage (V)	Maximum Output Current (A)
Source	4~28	5/7/9/12/15/20	3
Sink	4~28	4~20	3

BOM List

Designator	Description	Part Number	Manufacturer
Sink mode		SY21612BQFC	Silergy
C1,C2,C3,C9,C10,C11	10μF/50V/X5R,1206	C3216X5R1H106K	TDK
C4,C5	0.1μF/50V/X7R,0603	C1608X7R1H104K	TDK
C6	4.7μF/16V/X5R,0603	C1608X5R0J475K	TDK
C7	10pF/50V/C0G, 0603	C1608C0G1H100J	TDK
C8	2.2nF/50V	C1608C0G1H222J	TDK
R1	110k,1%,0603		
R2	10k,1%,0603		
R3	10k,1%,0603		
R4	0.01Ω,1%,1206		
R5	91k,1%,0603		
R6	10k,1%,0603		
R7	1MΩ,1%,0603		
L1	3.3μH	PCMB104T3R3MS	

Recommend Table for Typical Applications

V_{OUT}(V)	Fsw(Hz)	L	Cout
5	500k	2.2μH	3*22uF/50V, 1206, X5R
12	500k	3.3μH	3*22uF/50V, 1206, X5R
12	250k	4.7μH	3*22uF/50V, 1206, X5R
20	250k	6.8μH	3*22uF/50V, 1206, X5R

Layout Design suggestion

For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{BAT}, C_{VCC}, C_{BUS}, C_{BS}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) The decoupling capacitor of V_{BAT} must be placed close enough to the BAT pin and GND pin. The loop area formed by the input capacitors, BAT pin and GND pins must be minimized.

3) The decoupling capacitor of V_{BUS} also must be placed close enough to the VBUS pin and GND pin. The loop area formed by the output capacitors, VBUS pin and GND pins also must be minimized.

4) BS pin is sensitive. Bootstrap cap must be placed between BS and LX as close as possible.

5) To prevent the circulating currents in the ground plane from disrupting operation of the regulator, all small-signal grounds should return to GND by a separation way. This main includes the ground connection for the FB pin resistor and the feedback network when work in Sink mode.

If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode

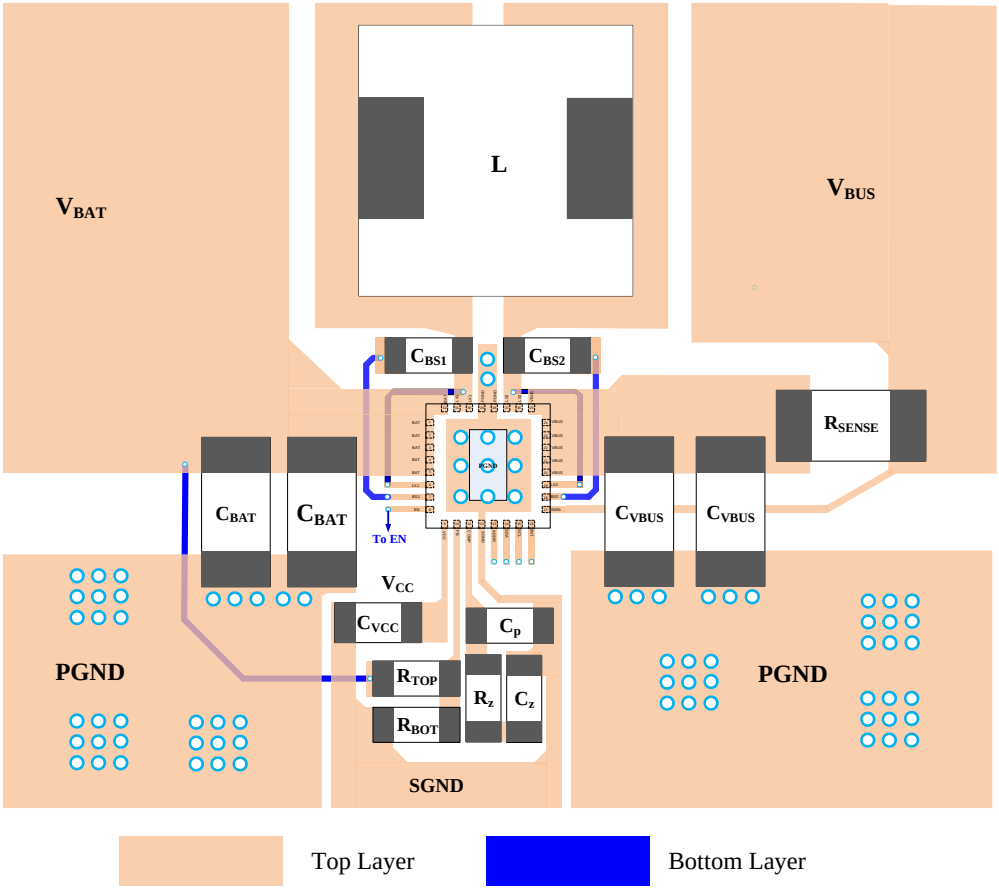
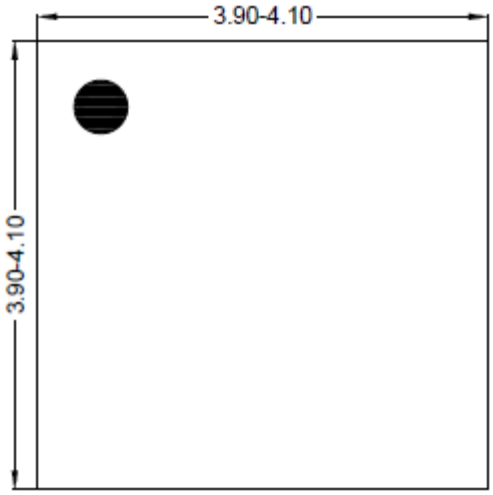
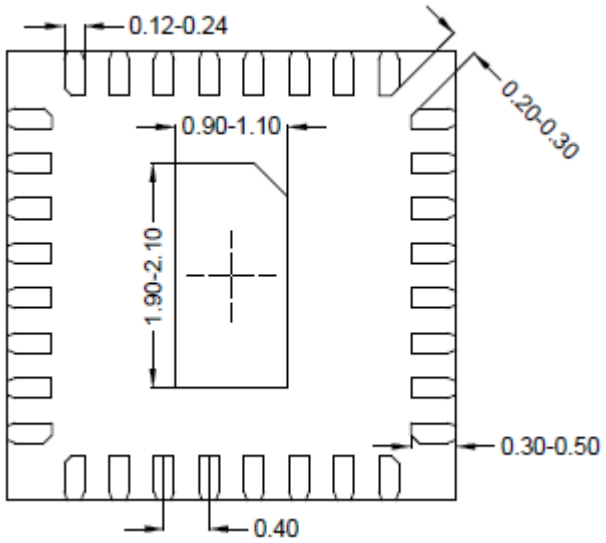


Figure8. PCB Layout Suggestion

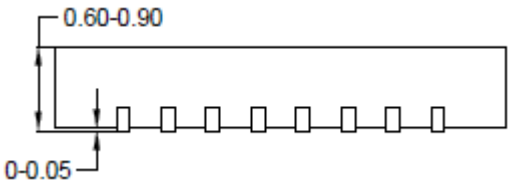
QFN4×4-32 Package Outline Drawing



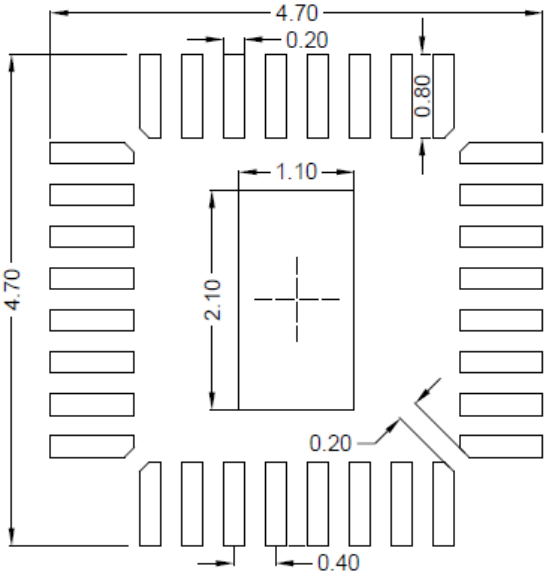
Top View



Bottom View



Side View



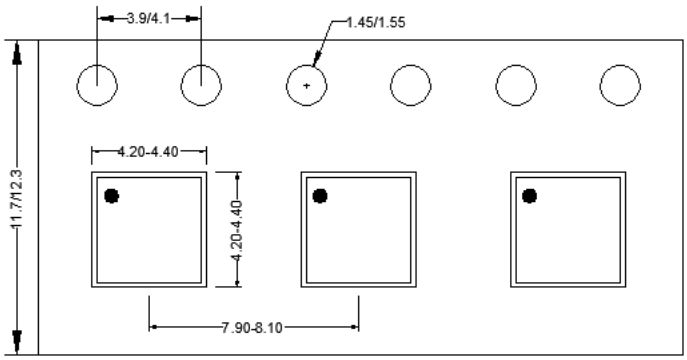
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

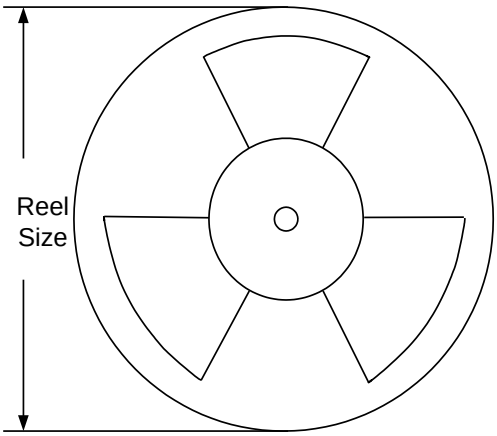
1. Taping orientation

QFN4×4



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN4×4	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 13, 2025	Revision 1.0A	Add the following description to the BS2/BS1 pin description (Page2) and the **External Bootstrap Capacitor Connection** application information (page 14): ---- Do not connect a resistor in series with the capacitor.
Mar.24, 2023	Revision 1.0	Upgrade the version code to Rev.1.0 for Production Release.
Apr.09, 2020	Revision 0.9	Initial Release

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