SY20745

SMBus Controlled 1-4 Cell Battery Charger Controller Supporting Boost Mode

General Description

The SY20745 is a high efficient, multi-cell battery charger controller supporting Boost mode. It allows the battery to discharge energy to the system when the system power demand is higher than the input capacity temporarily.

Three internal DACs are used as the reference of the charge voltage, the charge current, and the input current limit. They can be programmed by the system using SMBus.

The SY20745 can charge 1, 2, 3 and 4 cells battery pack and is available in QFN3.5x3.5-20 package to allow the small PCB footprint.

Ordering Information

SY20745 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20745RBC	QFN3.5x3.5-20	

Applications

- Notebook and Sub-notebook
- Battery Charger Cradle
- Portable Equipment with Rechargeable Battery
- Battery Back-up Systems

Features

- Input Voltage Range 4.5V to 25V
- SMBus Controlled Synchronous Buck Controller with 615kHz, 750kHz and 885kHz Programmable Switching Frequency
- SMBus Controls
  - Battery Charge Voltage (1.024V – 19.2V)
  - Battery Charge Current (128mA – 8.128A)
  - Adapter Input Current Limit (128mA – 8.064A)
- ±0.5% Battery Charge Voltage Accuracy
- ±3% Battery Charge Current Accuracy
- ±3% Adapter Input Current Limit Accuracy
- ±2% 20x Input Current or Charge Current Amplifier Output Accuracy
- Internal Charge Pumps for AC Blocking NFETs and BAT NFET
- Integrated Loop Compensation
- Internal Soft Start
- Programmable Adapter Detection and Indicator Support Air-line Adapter
- Support 1, 2, 3 and 4 Cells Battery Pack
- Support Boost Mode
- Battery LEARN Function and Programmable Battery Depletion Threshold
- Cycle-by-cycle Peak Current Limit
- Battery Over Voltage Protection and Short Protection
- Inductor and MOSFET Short Circuit Protection
- Thermal Shutdown with Hysteresis
- 0.65mA(0.8mA Max) Adapter Standby Quiescent Current
- 5μA Off-state Battery Discharge Current
- Package QFN 3.5x3.5-20

Typical Application

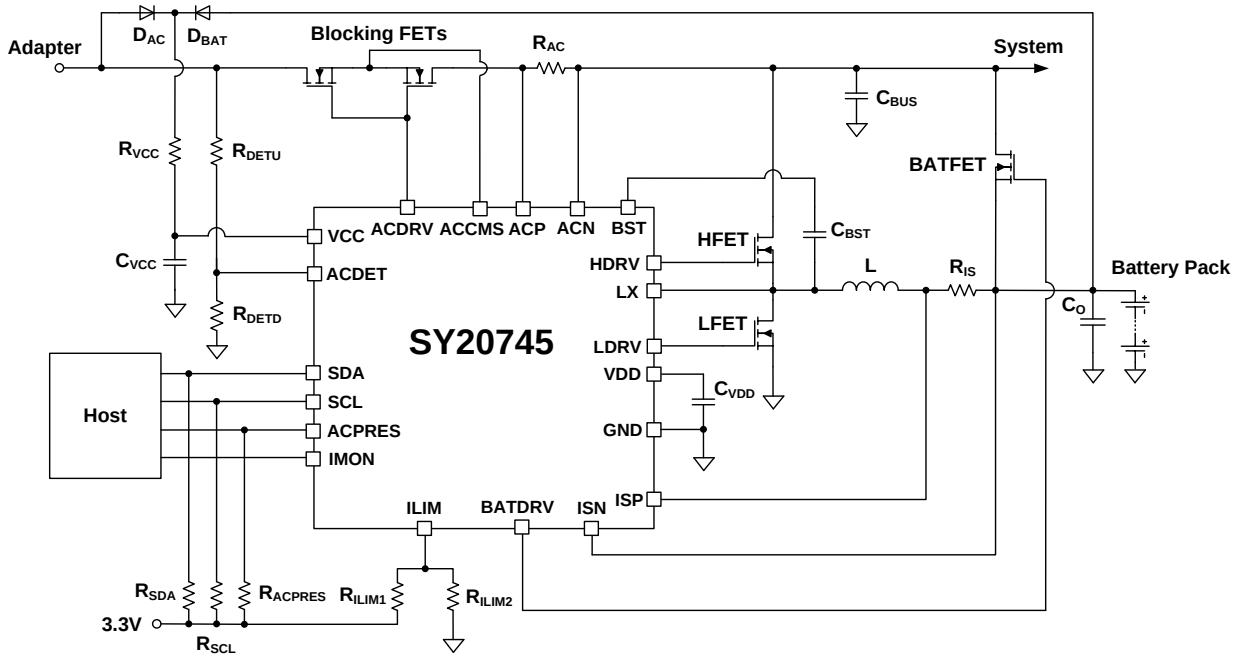


Figure1a. Schematic Diagram

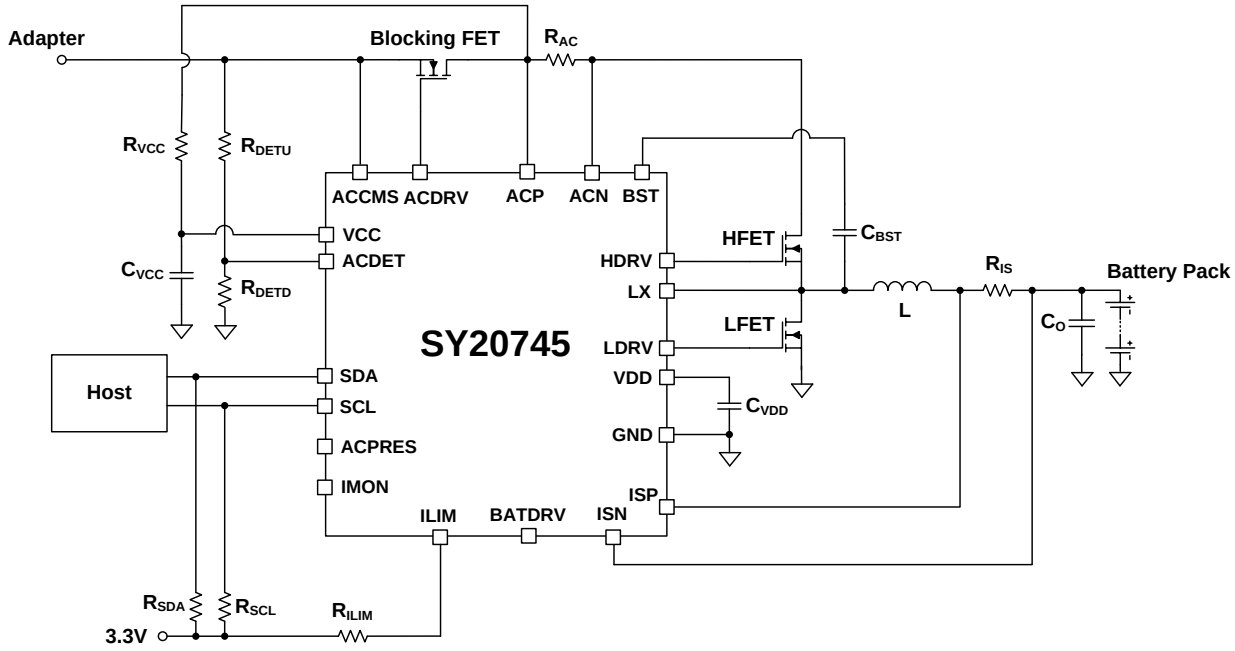
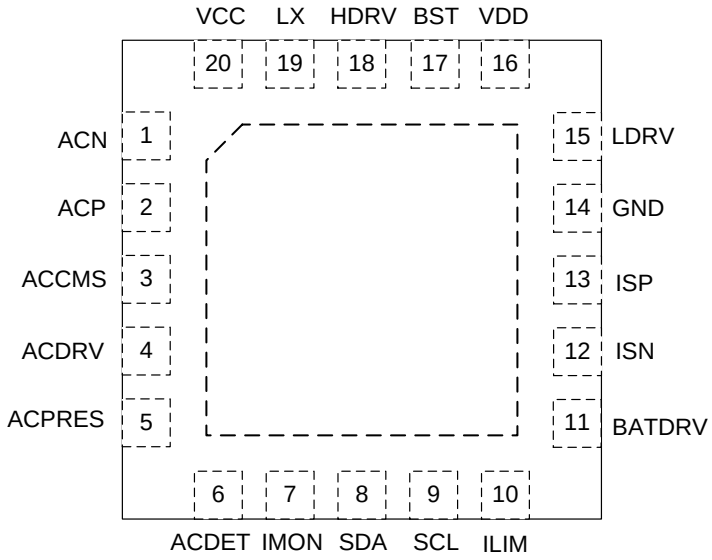


Figure1b. Schematic Diagram

Pinout (top view)



(QFN3.5x3.5-20)

Top Mark: AUS*xyz* (device code: **AUS**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
ACN	1	Adapter current sense negative input.
ACP	2	Adapter current sense positive input.
ACCMS	3	Common source connection for N-channel MOSFET switches.
ACDRV	4	N-channel blocking MOSFETs driver output.
ACPRES	5	AC adapter detection open-drain output. It's pulled high by an external pull-up resistor when the ACDET voltage is above 1.8V and the VCC voltage is above UVLO threshold. High ACPRES indicates a valid adapter (air mode or normal AC adapter) is present to start charge.
ACDET	6	Adapter detection input. Use the resistor divider from adapter output to set the detection voltage. When the ACDET voltage is above 0.6V and the VCC voltage is above UVLO threshold, the VDD will be present, ACPRES comparator and IMON will be active.
IMON	7	Buffered input or charge current output, selectable with SMBus command. The IMON voltage is 20 times of the differential voltage across the sense resistor.
SDA	8	SMBus data I/O. Open-drain output. Connect an external pull-up resistor according to the SMBus specification.
SCL	9	SMBus clock input. Connect an external pull-up resistor according to the SMBus specification.
ILIM	10	Charge current limit input. Minimum of the ILIM voltage and DAC limit voltage sets charge current limit. Setting the ILIM voltage above 1.6V will disable this control. Once the voltage on ILIM pin falls below 75mV, charge will be disabled. Charge will be enabled when the voltage on ILIM pin rises above 105mV.
BATDRV	11	Charge pump output to drive N-channel BAT MOSFET.
ISN	12	Battery charge current sense negative input.
ISP	13	Battery charge current sense positive input.
GND	14	IC ground.

LDRV	15	Low side MOSFET driver output.
VDD	16	LDO output for converter power MOSFETs driver. Connect a 1μF ceramic capacitor at least to GND.
BST	17	High side power MOSFET driver power supply.
HDRV	18	High side MOSFET driver output.
LX	19	Inductor connecting point.
VCC	20	IC power supply input. Add a 10Ω resistor and a 1μF capacitor to filter the inrush current and the high frequency noise.

Absolute Maximum Ratings (Note 1)

ACN, ACP, ACCMS, ACPRES, ISN, ISP, LX, VCC ---------- -0.3V to 30V
ACDRV, BATDRV, BST, HDRV---------- -0.3V to 36V
ACDET, IMON, SDA, SCL, ILIM, LDRV, VDD ---------- -0.3V to 6V
ACP-ACN, ISP-ISN ---------- -0.3V to 0.3V
ACDRV-ACCMS, BATDRV-ISN, BST-LX, BST-HDRV, HDRV-LX, VDD-LDRV---------- -0.3V to 6V
Package Thermal Resistance (Note 2)
QFN3.5×3.5-20, θ_{JA} ---------- 46.8°C/W
QFN3.5×3.5-20, θ_{JC} ---------- 56.9°C/W
Junction Temperature Range ---------- -40°C to 150°C
Operating Temperature Range ---------- -40°C to 100°C
Storage Temperature ---------- -65°C to 150°C
Lead Temperature (Soldering, 10s) ---------- 300°C

Recommended Operating Conditions (Note 3)

ACN, ACP, ACCMS, ACPRES, ISN, ISP, LX, VCC ---------- -0.3V to 25V
ACDRV, BATDRV, BST, HDRV---------- -0.3V to 30V
ACDET, IMON, SDA, SCL, ILIM, LDRV, VDD ---------- -0.3V to 5.5V
ACP-ACN, ISP-ISN, ---------- -0.2V to 0.2V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(T_A = 25℃, V_{VCC}=18V, V_{ISN}=12V, 10mΩ sense resistor between ACP and ACN, 10mΩ sense resistor between ISP and ISN, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Condition						
VCC Input Voltage Range	V_{VCC_RNG}		4.5		25	V
Regulation Range and Accuracy						
Charge Voltage Regulation Range	$V_{BAT\_REG\_RNG}$		1.024		19.2	V
Charge Voltage Regulation Accuracy	$V_{BAT\_REG\_ACC}$	ChargeVoltage() = 0x41A0	16.716	16.8	16.884	V
			-0.5%		0.5%	
		ChargeVoltage() = 0x3130	12.529	12.592	12.655	V
			-0.5%		0.5%	
		ChargeVoltage() = 0x20D0	8.35	8.4	8.45	V
			-0.6%		0.6%	
		ChargeVoltage() = 0x1060	4.163	4.192	4.221	V
			-0.7%		0.7%	
Charge Current Regulation Range	$I_{CHG\_REG\_RNG}$	$V_{ISP-ISN}$, 10mΩ sense resistor	0		8128	mA
Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$	ChargeCurrent() = 0x1000	3973	4096	4219	mA
			-3%		3%	
		ChargeCurrent() = 0x0800	1946	2048	2150	mA
			-5%		5%	
		ChargeCurrent() = 0x0200	430	512	594	mA
			-16%		16%	
		ChargeCurrent() = 0x0100	204.8	256	307.2	mA
			-20%		20%	
		ChargeCurrent() = 0x00C0	147.8	192	236.2	mA
			-23%		23%	
		ChargeCurrent() = 0x0080	64	128	192	mA
			-50%		50%	
Input Current Limit Regulation Range	$I_{AC\_REG\_RNG}$	$V_{ACP-ACN}$, 10mΩ sense resistor	0		8064	mA

Input Current Limit Regulation Accuracy	$I_{AC\_REG\_ACC}$	InputCurrent() = 0x1000	3973	4096	4219	mA
			-3%		3%	
		InputCurrent() = 0x0800	1946	2048	2150	mA
			-5%		5%	
		InputCurrent() = 0x0400	870	1024	1178	mA
			-15%		15%	
		InputCurrent() = 0x0200	384	512	640	mA
			-25%		25%	
Current Sense Amplifier						
Current Sense Amplifier Output Voltage Range	V_{IMON_RNG}		0		3.3	V
Current Sense Amplifier Output Current Range	I_{IMON_RNG}		0		1	mA
Current Sense Amplifier Gain	A_{IMON}	$V_{IMON}/(V_{ISP}-V_{ISN})$ or $(V_{ACP}-V_{ACN})$		20		V/V
Current Sense Amplifier Gain Accuracy	V_{IMON_ACC}	$V_{ACP}-V_{ACN}$ or $V_{ISP}-V_{ISN}$=40.96mV	-2%		2%	
		$V_{ACP}-V_{ACN}$ or $V_{ISP}-V_{ISN}$=20.48mV	-4%		4%	
		$V_{ACP}-V_{ACN}$ or $V_{ISP}-V_{ISN}$=10.24mV	-15%		15%	
		$V_{ACP}-V_{ACN}$ or $V_{ISP}-V_{ISN}$=5.12mV	-20%		20%	
		$V_{ACP}-V_{ACN}$ or $V_{ISP}-V_{ISN}$=2.56mV	-33%		33%	
		$V_{ACP}-V_{ACN}$ or $V_{ISP}-V_{ISN}$=1.28mV	-50%		50%	
Buffer Capacitance Load	C_{IMON}		0		100	pF
Comparator						
VCC UVLO Comparator	V_{UVLO}	V_{VCC} rising	3.5	3.75	4	V
VCC UVLO Hysteresis	ΔV_{UVLO}	V_{VCC} falling		340		mV
ACPRES Rising Threshold	V_{ACPRES}	V_{VCC} >V_{UVLO}, V_{ACDET} rising	1.78	1.80	1.82	V
ACPRES Falling Hysteresis	V_{ACPRES_HYS}	V_{VCC} >V_{UVLO}, V_{ACDET} falling	35	50	75	mV
ACPRES Rising Deglitch Time	t_{ACPRES_DEG}	V_{VCC} >V_{UVLO}, V_{ACDET} rising above 2.4V, First time or ChargeOption() bit [15]=0	110	160	210	ms
		V_{VCC} >V_{UVLO},V_{ACDET} rising above 2.4V, Not first time and ChargeOption() bit [15]=1	0.9	1.3	1.7	s
		V_{VCC} >V_{UVLO},V_{ACDET} rising above 1.8V and less than 2.4V, air mode	0.6	1.0	1.7	s
WAKEUP Detect Rising	V_{WAKE_RISE}	V_{VCC}> V_{UVLO}, V_{ACDET} rising		0.6	0.8	V

Threshold						
WAKEUP Detect Falling Threshold	V_{WAKE_FALL}	V_{VCC}> V_{UVLO}, V_{ACDET} falling	0.3	0.5		V
AC Over Voltage ACDET Rising Threshold	V_{ACOV}	V_{ACDET} rising	3.05	3.15	3.25	V
AC Over Voltage ACDET Falling Hysteresis	V_{ACOV_HYS}	V_{ACDET} falling	50	75	100	mV
VCC to ISN Comparator	V_{VCC_ISN}	V_{VCC}-V_{ISN} falling threshold	70	125	200	mV
VCC to ISN Comparator Hysteresis	$V_{VCC\_ISN\_HYS}$	V_{VCC}-V_{ISN} rising hysteresis	100	150	200	mV
ACN to ISN Comparator	V_{ACN_ISN}	V_{ACN}-V_{ISN} falling threshold	120	200	280	mV
ACN to ISN Comparator Hysteresis	$V_{ACN\_ISN\_HYS}$	V_{ACN}-V_{ISN} rising hysteresis	40	80	120	mV
HFET_SC ACP to LX Comparator Rising Threshold	V_{HFET_SC}	ChargeOption() bit [8] = 1	450	750	1200	mV
		ChargeOption() bit [8] = 0, Disable function				
LFET_SC LX to GND Comparator Rising Threshold	V_{LFET_SC}	ChargeOption() bit [7] = 0, Buck Mode	100	125	150	mV
		ChargeOption() bit [7] = 0, Boost Mode	120	150	180	
		ChargeOption() bit [7] = 1, Buck Mode	200	250	300	
		ChargeOption() bit [7] = 1, Boost Mode	240	300	360	
Cycle-by-cycle Peak Current Limit during Buck Mode, ISP to ISN Comparator Rising Threshold	V_{PK_CHARGE}	ChargeCurrent() = 0x0xxxH	45	55	65	mV
		ChargeCurrent() = 0x1000H–0x17C0H	70	85	100	
		ChargeCurrent() = 0x1800H–0x1FC0H	90	105	120	
Fast DPM Comparator Threshold	I_{DPM}	Stop charging and enter Boost mode threshold with respect to input current limit	103%	107%	111%	I_{AC_REG}
ACOC Comparator Rising Threshold	I_{ACOC}	ChargeOption() bit [1] = 1	300%	333%	366%	I_{AC_REG}
Min ACOC Clamped Threshold	I_{ACOC_MIN}	I_{ACOC}=333%×I_{AC_REG}	4	4.5	5	A
Max ACOC Clamped Threshold	I_{ACOC_MAX}	I_{ACOC}=333%×I_{AC_REG}	13.5	15	16.5	A
ACOC Deglitch Time	t_{ACOC_DEG}	Voltage across input sense resistor rising to disable charge	2.3	4.2	6.6	ms
BAT OV Rising Threshold	V_{BATOV_RISE}	V_{ISN} rising	103%	104%	106%	V_{BAT_REG}

BAT OV Falling Threshold	V_{BATOV_FALL}	V_{ISN} falling		102%		V_{BAT_REG}
Battery Depletion ISN Falling Threshold	V_{BATDEP}	ChargeOption() bit [12:11] = 00	55.53%	59.19%	63.5%	V_{BAT_REG}
		ChargeOption() bit [12:11] = 01	58.68%	62.65%	67.5%	
		ChargeOption() bit [12:11] = 10	62.17%	66.55%	71.5%	
		ChargeOption() bit [12:11] = 11	66.06%	70.97%	77%	
Battery Depletion ISN Rising Hysteresis	V_{BATDEP_HYS}	ChargeOption() bit [12:11] = 00	225	305	400	mV
		ChargeOption() bit [12:11] = 01	240	325	430	
		ChargeOption() bit [12:11] = 10	255	345	450	
		ChargeOption() bit [12:11] = 11	280	370	490	
Battery Depletion ISN Rising Deglitch Time	t_{BATDEP_DEG}			600		ms
BAT UV Falling Threshold	V_{BATUV}	V_{ISN} falling	2.4	2.5	2.6	V
BAT UV Rising Hysteresis	V_{BATUV_HYS}	V_{ISN} rising		200		mV
ILIM Falling Threshold to Disable Charge	V_{ILIM_DIS}	V_{ILIM} falling	60	75	90	mV
ILIM Rising Threshold To Enable Charge	V_{ILIM_EN}	V_{ILIM} rising	90	105	120	mV
Thermal Shutdown Rising Threshold	T_{SD}	Temperature rising		150		ºC
Thermal Shutdown Falling Hysteresis	T_{SD_HYS}	Temperature falling		20		ºC
Driver Capability						
VDD LDO Voltage	V_{VDD}	V_{VCC}>6V,V_{ACDET}>0.6V	5	5.5	6	V
VDD Current Capacity	I_{VDD}	V_{VCC}>6V,V_{ACDET}>0.6V	55			mA
High Side Driver Turn-on Resistance	R_{H_ON}	V_{BST}-V_{LX}=5.2V		3		Ω
High Side Driver Turn-off Resistance	R_{H_OFF}			0.5		Ω
Low Side Driver Turn-on Resistance	R_{L_ON}	V_{VDD}=5.5V		4		Ω
Low Side Driver Turn-off Resistance	R_{L_OFF}			0.5		Ω
Dead Time from HDRV Low to LDRV High	t_{DEAD_LD}			20		ns
Dead Time from LDRV Low to HDRV High	t_{DEAD_HD}			20		ns
ACDRV Driver Voltage	V_{ACPUMP}	V_{ACDRV}-V_{ACCMS} when V_{VCC}>6V		6		V
ACDRV Driver Source Current	I_{ACDRV_SOURCE}		30	60		µA

ACDRV Driver Sink Current	I_{ACDRV_SINK}		1.75			mA
BATDRV Driver Voltage	$V_{BATPUMP}$	V_{BATDRV}-V_{ISN} when V_{VCC}>6V		6		V
BATDRV Driver Source Current	I_{BATDRV_SOURCE}		40	60		µA
BATDRV Driver Sink Current	I_{BATDRV_SINK}			1		mA
PWM Oscillator						
PWM Switching Frequency	F_{SW}	ChargeOption() bit [9] = 0 (Default)	600	750	900	kHz
PWM Increase Frequency	F_{SW+}	ChargeOption() bit [10:9] = 11	665	885	1100	kHz
PWM Decrease Frequency	F_{SW-}	ChargeOption() bit [10:9] = 01	465	615	765	kHz
Logic I/O						
SCL/SDA Input Low Threshold	V_{IN_LO}				0.8	V
SCL/SDA Input High Threshold	V_{IN_HI}		2.1			V
SDA/ACPRES Output Saturation Voltage	V_{OUT_LO}	5mA drain current			0.5	V
SDA/ACPRES Leakage Current	I_{OUT_LEAK}	V=7V	-1		1	µA
Time						
Soft Start Current Step	I_{STEP}	10mΩ current sensing resistor		64		mA
Soft Start Current Step Time	t_{STEP}			240		µs
Quiescent Current						
Battery Current when BATFET OFF	$I_{BAT\_BATFET\_OFF}$	V_{ISN}=16.8V, VCC disconnect from battery, BATFET charge pump off, BATFET turns off			5	µA
Battery Current when BATFET ON	$I_{BAT\_BATFET\_ON}$	V_{ISN} =16.8V, VCC connect from battery, BATFET charge pump on, BATFET turns on			25	µA
Standby Quiescent Current	$I_{STANDBY}$	Adapter present, V_{VCC}>V_{UVLO}, V_{ACDET}>0.6V, charge disabled		0.65	0.8	mA
Adapter Current when No Switching	I_{AC_NOSW}	Adapter present, V_{VCC}>V_{UVLO}, 2.4V<V_{ACDET}<3.15V, charge enabled, no switching		1.5	3	mA
Adapter Current when Switching	I_{AC_SW}	Adapter present, V_{VCC}>V_{UVLO}, 2.4V<V_{ACDET}<3.15V, charge enabled, switching, MOSFET SiS412DN		10		mA

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

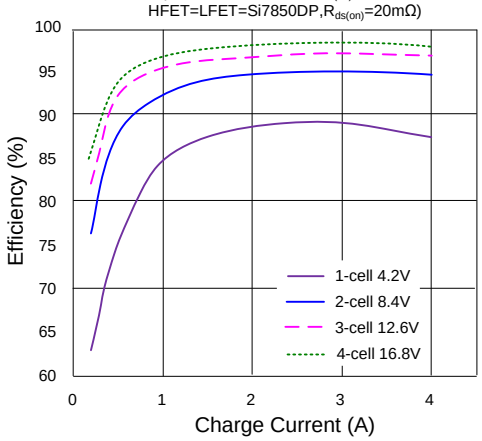
SMBus Timing Specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SMBus Frequency	$F_{S(CLK)}$		10		100	kHz
SCL/SDA Rise Time	t_{RISE}				1	µs
SCL/SDA Fall Time	t_{FALL}				300	ns
SCL Pulse Width High	$t_{W(HIGH)}$		4		50	µs
SCL Pulse Width Low	$t_{W(LOW)}$		4.7			µs
Setup Time for START Condition	$t_{SET(START)}$		4.7			µs
START Condition Hold Time after which First Clock Pulse is Generated	$t_{HOLD(START)}$		4			µs
Data Setup Time	$t_{SET(DAT)}$		250			ns
Data Hold Time	$t_{HOLD(DAT)}$		300			ns
Setup Time for STOP Condition	$t_{SET(STOP)}$		4			us
Bus Free Time between START and STOP Condition	$t_{FREE(BUS)}$		4.7			us
SMBus Bus Release Timeout	$t_{TIMEOUT}$			30		ms
Deglitch for Watchdog Reset Signal	t_{BOOT}		10			ms
Watchdog Timeout Period	$t_{WATCHDOG}$	ChargeOption() bit [14:13] = 11	140	175	210	s
		ChargeOption() bit [14:13] = 10	70	88	105	s
		ChargeOption() bit [14:13] = 01	35	44	53	s

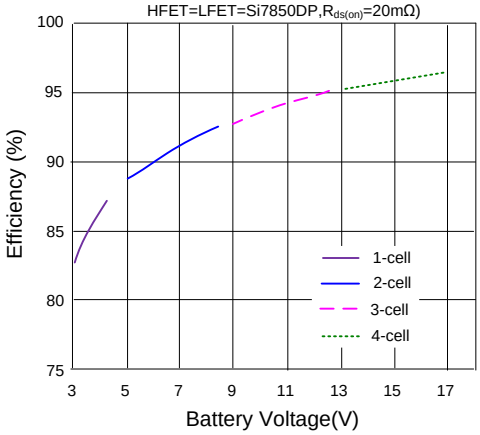
Typical Performance Characteristics

T_A=25°C, V_{IN}=19V, I_{CHG}=4A, 2cell battery, L=4.7μH, unless otherwise specified.

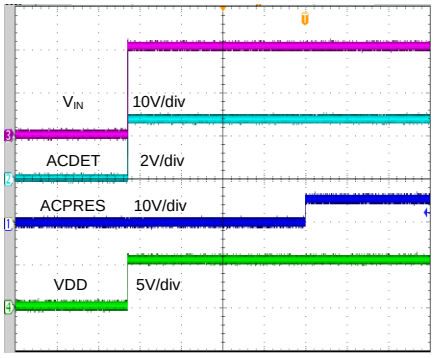
Efficiency vs. Charge Current(CV Mode)



Efficiency vs. Battery Voltage(CC Mode)

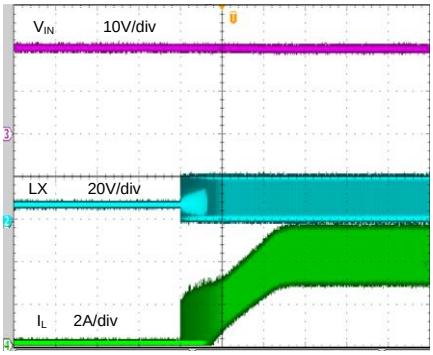


Control Timing



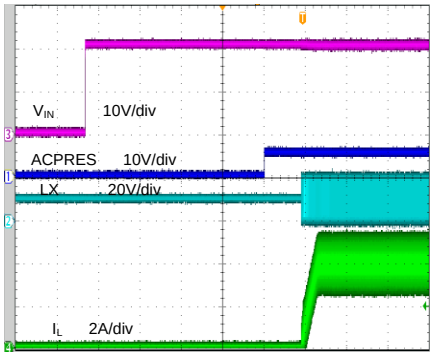
Time(40.0ms/div)

Current Soft Start



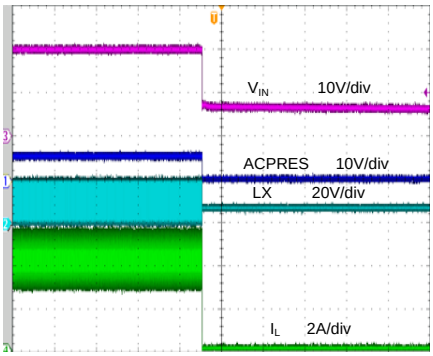
Time(4.00ms/div)

Insert Adapter



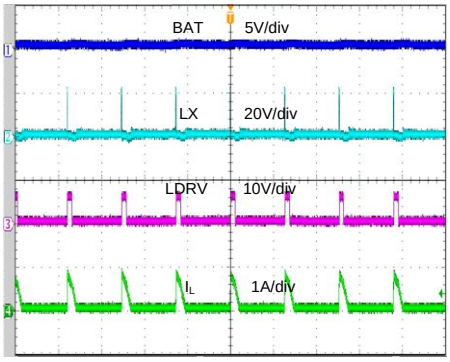
Time(40.0ms/div)

Remove Adapter



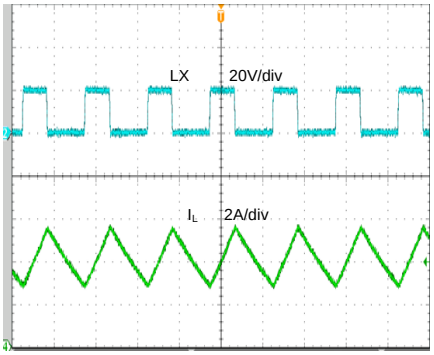
Time(40.0ms/div)

Battery Short



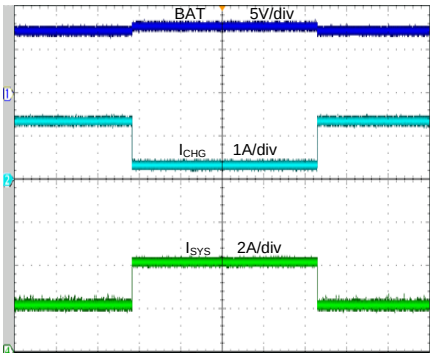
Time (20.0μs/div)

Constant Current Charge State



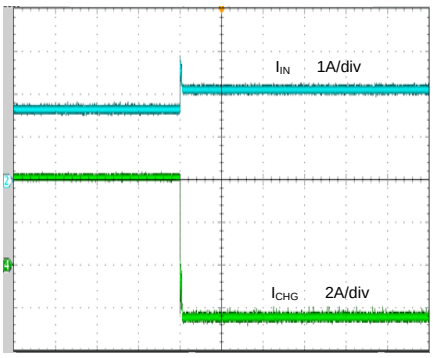
Time(1.00μs/div)

System Load Transient(Input DPM)



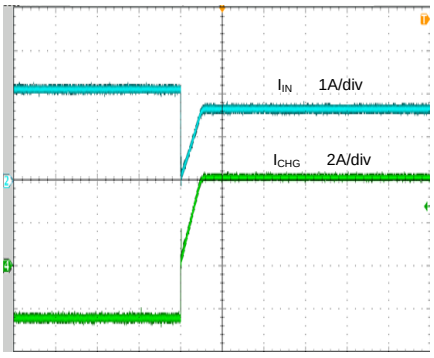
Time(400ms/div)

Buck to Boost Mode



Time(100ms/div)

Boost to Buck Mode



Time(20ms/div)

General Function Description

The SY20745 is a high efficient, multi-cell battery charger controller supporting Boost mode. It allows the battery to discharge energy to the system when the system power demand is higher than the input capacity temporarily.

Three internal DACs are used as the reference of the charge voltage, the charge current, and the adapter input current limit. They can be programmed by system using SMBus.

Adapter Detect and Power up (ACPRES)

Pin ACDET detects the input voltage from the adapter or other DC source. The divider resistors should program the input voltage higher than the maximum battery voltage and lower than the maximum allowed adapter voltage.

ACPRES can be pulled to the external rail by the pull-up resistor after ACPRES deglitch time under the following conditions:

- V_{VCC}>V_{UVLO}, ensure the control circuits operate well;
- V_{ACDET}>1.8V, the input voltage is within operation range;

The ACPRES rising deglitch time is 160ms for the first time after POR no matter what the charge option register value is. After one time the voltage on ACDET pin drops below 1.8V but above 0.6V, the next ACPRES rising deglitch time will be forced to 1.3s.

Battery Charge Voltage, Battery Charge Current, and Adapter Input Current Limit Regulation

The battery charge voltage regulation is set by an 11-bit DAC register, programmed by the host microcontroller through the SMBus interface.

The battery charge current regulation is set by a 7-bit DAC register. It is sensed by a resistor connected between the ISP and ISN pins. For a 10mΩ sense resistor, the maximum current is 8.128A. A larger resistor gives lower maximum current and higher regulation accuracy.

The adapter input current limit is set by a 6-bit DAC register, sensed by the resistor between the ACP and ACN pins. For a 10mΩ sense resistor, the maximum current is 8.064A. A high accuracy amplifier provides an analog output voltage of 20X ACP-ACN at the IMON pin that can be used by the host system to monitor the adapter input current. If the adapter current rises to the limit, the battery charge current will be reduced so that the charger will not reduce the current available to the system.

Dynamic Power Management (DPM, ACOC)

When the input current rises to adapter input current limit due to system load, the charge current will be decreased by the input current limit loop. It can prevent adapter overload.

The ACOC function can be enabled by charge option register. If the input current has increased to the ACOC set point for 4.2ms (t_{ACOC_DEG}), ACFETs will latch off. The latch status can't be cleared until adapter is removed.

Boost Mode

SY20745 supports Boost mode. The system draws the battery power through Boost converter when the adapter is fully loaded. During Boost mode, battery energy is delivered to system when system power demand is temporarily higher than adapter maximum power level so that adapter will not overload. After POR, the charge option register bit[3] is 0 which disable Boost mode. To enable it, the charge option register bit[3] must be written to 1 by the host.

When input current is higher than the FAST_DPM comparator threshold, if Boost mode is enabled, the IC will allow battery to discharge and the converter will change from Buck to Boost. During Boost mode the adapter current is regulated at input current limit level so that adapter will not overload. The battery discharge current depends on system current requirement and adapter input current limit register setting value. The SMBus timer can be enabled to prevent converter running at Boost mode for too long time.

Cycle-by-cycle Peak Current Limit

The SY20745 uses cycle-by-cycle peak current limit mode to prevent the switch from over current. The IC senses the voltage drop of resistor or switch as the current information. The peak current limit values of Buck and Boost are different.

MOSFET Short Circuit Protection (HFET_SC, LFET_SC)

When the MOSFET or inductor is shorten, the high voltage drop across the $R_{DS(ON)}$ will trigger the HFET_SC or LFET_SC. When the counter receives the short circuit signal over 7 times within 90s, the IC will latch off the converter. Recycle the AC input will release the latch off status.

Battery Over Voltage Protection (BATOV)

The converter will not switch when battery voltage exceeds 104% of the regulation voltage set point. Switching resumes when it is below 102%.

Battery Short Protection (BATUV)

A comparator monitors output battery voltage. If the voltage falls below 2.5V (V_{BATUV}), the battery short status will be detected. The peak current will be clamped to a low value and the IC will decrease the switching frequency. The charge current will return to the set point when the battery voltage rises above 2.7V (V_{BATUV}+V_{BATUV_HYS}).

Thermal Shutdown Protection (T_{SD})

When the junction temperature exceeds 150°C, the IC will shut down. Once the temperature drops below 130°C, switching will resume.

Charge Timeout

A timer will terminate charging if the charger does not receive a charge voltage or charge current command within 175s. If a timeout occurs, either charge voltage or charge current command must be sent to reenable charging.

Battery LEARN

A Battery LEARN cycle can be activated via SMBus command in the SY20745. Battery LEARN mode allows the battery to discharge in order to calibrate the battery gas gauge over a complete discharge/charge cycle. When entering into battery LEARN mode, the IC will turn off the converter and ACFETs first, and then will turn on BATFET to support the discharge mode. When exiting battery LEARN mode, the IC will recovery to normal mode if all conditions are ready.

SMBus Interface

The System Management Bus

The System Management Bus (SMBus) is a 2 wire BUS that supports bidirectional communications. The protocol is described briefly here. More detail is available from www.smbus.org.

General SMBus Architecture

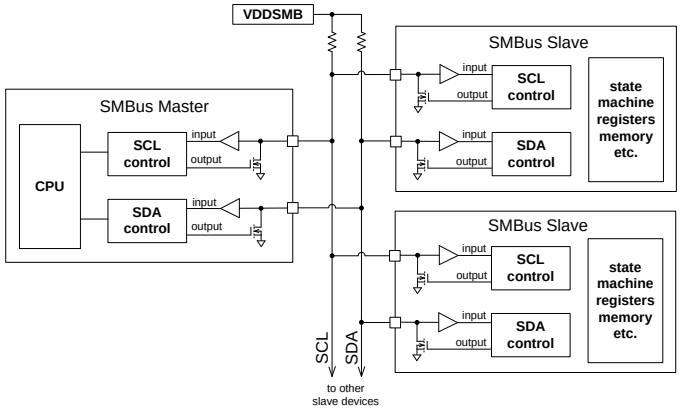


Figure2. SMBus Architecture

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure3.

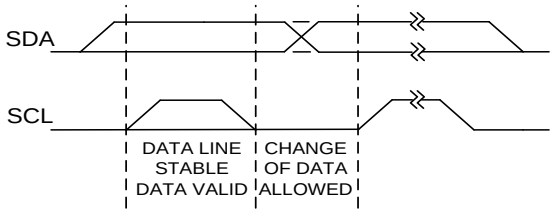


Figure3. Data Validity

START and STOP Conditions

As shown in Figure4, START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

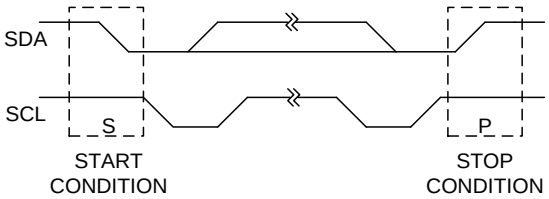


Figure4. Start and Stop Waveforms

Acknowledge

Each address and data transmission uses 9 clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7 slave address bits and a R/W bit during the next 8 clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data as described below.

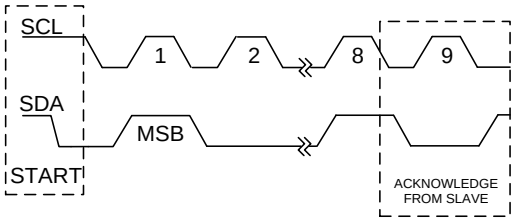


Figure5. Acknowledge On the SMBus

SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a START condition, followed by 7-bits of slave address (0001001 for the SY20745) followed by the R/W bit. The R/W bit is 0 for a write or 1 for a read. If any slave devices on the SMBus recognize their address, they will acknowledge by pulling the serial data (SDA) line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a not acknowledge condition. Once the control byte is sent, and the SY20745 acknowledges it, the 2nd byte sent by the master must be a register address byte such as 0x14 for the charge current register. The register address byte tells the SY20745 which register the master will write or read. See Table 1 for details of the registers. Once the SY20745 receives a register address byte it responds with acknowledgement.

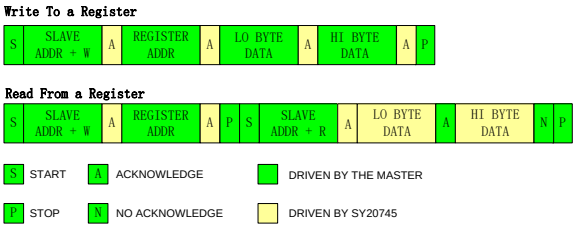


Figure6. SMBus/SY20745 Read and Write Protocol

Byte Format

Every byte put on the SDA line must be eight bits long and must be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB) and the least significant bit last (LSB).

SY20745 and SMBus

The SY20745 receives control inputs from the SMBus interface. The serial interface complies with the SMBus protocols as documented in the system management BUS specification V1.1, which can be downloaded from www.smbus.org. The SY20745 uses the SMBus Read-Word and Write-Word protocols (Figure 6) to communicate with the smart battery. The SY20745 is a SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001X. Read address = 0b00010011 and Write address = 0b00010010.

In addition, the SY20745 has two identification (ID) registers: a 16-bit device ID register and a 16-bit manufacturer ID register.

The data (SDA) and clock (SCL) pins have schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications. The SY20745 is controlled by the data written to the registers described in Table 1.

SMBus communication is enabled with the following conditions:

- V_{VCC} is above V_{UVLO} ;
- V_{ACDET} is above 0.6V.

Battery Charger Registers

The SY20745 supports four battery charger registers that use either write-word or read-word protocols, as summarized in Table 1. Manufacturer ID and Device ID are “read only” registers and can be used for identifying SY20745. On SY20745, Manufacturer ID always returns 0x0053 (ASCII code for “SI” for Silergy) and Device ID always returns 0x0002.

Table1. Battery Charger Register Summary

Register Address	Register Name	Read/Write	Description	POR State
0x12	ChargeOption()	Read or Write	16-Bit Charge Option Control	0xF902
0x14	ChargeCurrent()	Read or Write	7-Bit Charge Current Setting	0x0000
0x15	ChargeVoltage()	Read or Write	11-Bit Charge Voltage Setting	0x0000
0x3F	InputCurrent()	Read or Write	6-Bit Input Current Limit Setting	0x1000
0xFE	ManufactureID()	Read Only	Manufacture ID	0x0053
0xFF	DeviceID()	Read Only	Device ID	0x0002

Enabling and Disabling Charge

After applying power to the SY20745, the internal registers contain their POR values (see Table 1). The POR values for charge current and charge voltage are 0x0000. These values disable charge. To enable charge, the charge current register must be written with a number larger than 0x007F and the charge voltage register must be written with a number larger than 0x03FF. Charge can be disabled by writing 0x0000 to either of the two registers.

Charge Option Control

Charge option is set by writing a valid 16-bit number to the charge option register.

Table2. Charge Option (Register 0x12)

Bit	Bit Name	Description
0	Charge Inhibit	0: Enable Charge (POR default) 1: Inhibit Charge
1	ACOC Threshold Adjust	Set this bit 1 to limit the Input current when it is out of regulation. The maximum input current limit is 15A typical with10mΩ sense resistor. 0: Function is disabled 1: 3.33 x of input current regulation limit (POR default)
2	Boost Mode Indication (Read Only)	0: Not in Boost mode (POR default) 1: In Boost mode.
3	Boost Mode Enable	0: Disable Boost mode (POR default) 1: Enable Boost mode
4	AC Adapter Indication (Read Only)	0: AC adapter is not present (V_{ACDET}<2.4V) (POR default) 1: AC adapter is present (V_{ACDET}>2.4V)
5	IMON Selection	0: IMON is the 20x input current amplifier output (POR default) 1: IMON is the 20x charge current amplifier output
6	Battery LEARN Enable	0: Disable LEARN (POR default) 1: Enable LEARN
7	LFET_SC Comparator Threshold Adjust	Short circuit protection low side MOSFET voltage drop comparator threshold. This is also used for cycle-by-cycle current limit protection threshold during Boost mode. 0: 125mV (POR default) 1: 250mV

Bit	Bit Name	Description
8	HFET_SC Comparator Threshold Adjust	Short circuit protection high side MOSFET voltage drop comparator threshold. 0: Function is disabled. 1: 750mV (POR default).
9	EMI Switching Frequency Enable	0: Disable adjust PWM switching frequency (POR default). 1: Enable adjust PWM switching frequency
10	EMI Switching Frequency Adjust	Default frequency:750kHz 0: Reduce PWM switching frequency by 18% (POR default). 1: Increase PWM switching frequency by 18%.
11	BAT Depletion Comparator Threshold Adjust [12:11]	See bit [12].
12	BAT Depletion Comparator Threshold Adjust [12:11]	Bit [12:11] is used for LEARN function and battery over discharge protection during Boost mode. During LEARN cycle, when IC detects battery voltage is below depletion voltage threshold, the IC will turn off BATFET and turn on blocking FETs to power the system from AC adapter instead of the battery. During Boost mode, when the IC detects battery voltage is below depletion voltage threshold, the IC will stop Boost mode. Set charge voltage register value to 0V will disable this function. 00: Falling Threshold = 59.19% of voltage regulation limit (~2.486V/cell) 01: Falling Threshold = 62.65% of voltage regulation limit (~2.631V/cell) 10: Falling Threshold = 66.55% of voltage regulation limit (~2.795V/cell) 11: Falling Threshold = 70.97% of voltage regulation limit (~2.981V/cell) (POR default)
14:13	WATCHDOG Timer Adjust	Set maximum delay between consecutive SMBus Write charge voltage or charge current command. The charge will be suspended if the IC does not receive write charge voltage or write charge current command within the watchdog time period and watchdog timer is enabled. The charge will be resumed after receive write charge voltage or write charge current command when watchdog timer expires and charge suspends. During Boost mode, the timer is fixed to 175s if it is enabled. 00: Disable Watchdog Timer. 01: Enabled, 44 s. 10: Enabled, 88 s. 11: Enable Watchdog Timer (175s) (POR default).
15	ACPRES Deglitch Time Adjust	Adjust ACPRES rising edge deglitch time. After POR, the first time the adapter plug in occurs, the deglitch time is always 160ms no matter if this bit is 0 or 1. This bit only sets the next ACPRES deglitch time after ACFET turns off at least one time. To change this option, the VCC voltage must above UVLO threshold and the ACDET voltage must above 0.6V to enable the IC SMBus communication. 0: ACPRES rising edge deglitch time is 160ms. 1: ACPRES rising edge deglitch time is 1.3s (POR default).

Setting Charge Voltage

Charge voltage is set by writing a valid 16-bit number to the charge voltage register. This 16-bit number translates to a 65.535V full-scale voltage. The SY20745 ignores the first 4 LSBs and uses the next 11 bits to set the voltage DAC. The charge voltage range of the SY20745 is 1.024V to 19.200V. All numbers requesting charge voltage below 1.024V or above 19.2V result in a voltage set point of zero, which terminates charging.

Upon initial power up or reset, the charge voltage and charge current registers are reset to 0 and the charger remains shut down until valid numbers are sent to the charge voltage and charge current registers. Use the Write-word protocol to write to the charge voltage register. The register address for charge voltage is 0x15. The 16-bit binary number formed by D15–D0 represents the charge voltage set point in mV. However, the resolution of the SY20745 is 16mV because the D0–D3 bits are ignored as shown in Table 3. The D15 bit is also ignored because it is not needed to span the 1.024V to 19.2V range. Table 3 shows the mapping between the charge voltage set point and the 16-bit number written to the charge voltage register. The charge voltage register can be read back to verify its contents.

Table3. Charge Voltage (Register 0x15)

Bit	Bit Name	Description
0		Not used.
1		Not used.
2		Not used.
3		Not used.
4	Charge Voltage, DACV 0	0 = Adds 0mV of charge voltage. 1 = Adds 16mV of charge voltage.
5	Charge Voltage, DACV 1	0 = Adds 0mV of charge voltage. 1 = Adds 32mV of charge voltage.
6	Charge Voltage, DACV 2	0 = Adds 0mV of charge voltage. 1 = Adds 64mV of charge voltage.
7	Charge Voltage, DACV 3	0 = Adds 0mV of charge voltage. 1 = Adds 128mV of charge voltage.
8	Charge Voltage, DACV 4	0 = Adds 0mV of charge voltage. 1 = Adds 256mV of charge voltage.
9	Charge Voltage, DACV 5	0 = Adds 0mV of charge voltage. 1 = Adds 512mV of charge voltage.
10	Charge Voltage, DACV 6	0 = Adds 0mV of charge voltage. 1 = Adds 1024mV of charge voltage.
11	Charge Voltage, DACV 7	0 = Adds 0mV of charge voltage. 1 = Adds 2048mV of charge voltage.
12	Charge Voltage, DACV 8	0 = Adds 0mV of charge voltage. 1 = Adds 4096mV of charge voltage.
13	Charge Voltage, DACV 9	0 = Adds 0mV of charge voltage. 1 = Adds 8192mV of charge voltage.
14	Charge Voltage, DACV 10	0 = Adds 0mV of charge voltage. 1 = Adds 16384mV of charge voltage, 19200mV max.
15		Not used.

Setting Charge Current

SY20745 has a 16-bit charge current register that sets the battery charge current. SY20745 controls the charge current by controlling the ISP-ISN voltage. The SY20745 ignores the first 6 LSBs and uses the next 7 bits to control the current DAC. The charge-current range of the SY20745 is 128mA to 8.128A (using a 10mΩ current-sense resistor). All numbers requesting charge current below 128mA or above 8.128A result in a current setting of 0mA and charging termination.

The default charge current setting at power on Reset (POR) is 0mA. To stop charging, set charge current to 0. Upon initial power up, the charge voltage and charge current registers are reset to 0 and the charger is disabled. To start the charger, write valid numbers to the charge voltage and charge current registers. The charge current register uses the Write-word protocol. The register code for charge current is 0x14 (0b00010100). Table 4 shows the mapping between the charge current set point and the 16-bit number written to the charge current register. The charge current register can be read back to verify its contents.

The ILIM voltage also can limit the battery charge current. The limited charge current is given by the equation $I_{CHG}=V_{ILIM}/(20xR_{IS})$ in Buck mode. The lower of the current set by ILIM and DAC is selected for internal charge current limit.

Table4. Charge Current (Register 0x14) (10mΩ Sense Resistor)

Bit	Bit Name	Description
0		Not used.
1		Not used.
2		Not used.
3		Not used.
4		Not used.
5		Not used.
6	Charge Current, DACICHG 0	0 = Adds 0mA of charge current. 1 = Adds 64mA of charge current.
7	Charge Current, DACICHG 1	0 = Adds 0mA of charge current. 1 = Adds 128mA of charge current.
8	Charge Current, DACICHG 2	0 = Adds 0mA of charge current. 1 = Adds 256mA of charge current.
9	Charge Current, DACICHG 3	0 = Adds 0mA of charge current. 1 = Adds 512mA of charge current.
10	Charge Current, DACICHG 4	0 = Adds 0mA of charge current. 1 = Adds 1024mA of charge current.
11	Charge Current, DACICHG 5	0 = Adds 0mA of charge current. 1 = Adds 2048mA of charge current.
12	Charge Current, DACICHG 6	0 = Adds 0mA of charge current. 1 = Adds 4096mA of charge current, 8128mA max.
13		Not used.
14		Not used.
15		Not used.

Setting Input Current Limit

The total power from an adapter is the sum of the power supplied to the system and the power into the charger and battery. When the input current exceeds the set input current limit, the SY20745 will decrease the charge current to provide priority to system load current. As the system load rises, the available charge current drops linearly to zero. Thereafter, all input current goes to system load and input current increases.

The internal amplifier compares the differential voltage between ACP and ACN to a scaled voltage set by the input current register. The total input current is the sum of the device supply current, the charger input current, and the system load current. The total input current can be estimated as follows:

$$I_{INPUT} = I_{SYSTEM} + \left[\left(I_{CHG} \times V_{BATTERY} \right) / (V_{IN} \times \eta) \right]$$

where η is the efficiency of the DC/DC converter (typically 85% to 95%). To set the input current limit use the SMBus to write a 16-bit input current register using the data format listed in Table 5. The input current register uses the Write-Word protocol. The register code for input current is 0x3F (0b00111111). The input current register can be read back to verify its contents.

The SY20745 ignores the first 6 LSBs and uses the next 6 bits to control the input current DAC. The input-current range of the SY20745 is from 128mA to 8.064A. All 16-bit numbers requesting input current below 128mA or above 8.064A will terminate charging. The default input current limit setting at POR is 4.096A. When choosing the current-sense resistor, carefully calculate its power rating. Take into account variations in the system's load current and the overall accuracy of the sense amplifier. Note that the voltage drop across this resistor contributes additional power loss, which reduces efficiency. System currents normally fluctuate as portions of the system are powered up or put to sleep. Without input current regulation, the input source must be able to deliver the maximum system current and the maximum charger-input current. By using the input current limit circuit, the output-current capability of the AC wall adapter can be lowered, reducing system cost.

Table5. Input Current Limit (Register 0x3F) (10mΩ Sense Resistor)

Bit	Bit Name	Description
0		Not used.
1		Not used.
2		Not used.
3		Not used.
4		Not used.
5		Not used.
6		Not used.
7	Input Current, DACIIN 0	0 = Adds 0mA of input current. 1 = Adds 128mA of input current.
8	Input Current, DACIIN 1	0 = Adds 0mA of input current. 1 = Adds 256mA of input current.
9	Input Current, DACIIN 2	0 = Adds 0mA of input current. 1 = Adds 512mA of input current.
10	Input Current, DACIIN 3	0 = Adds 0mA of input current. 1 = Adds 1024mA of input current.
11	Input Current, DACIIN 4	0 = Adds 0mA of input current. 1 = Adds 2048mA of input current.
12	Input Current, DACIIN 5	0 = Adds 0mA of input current. 1 = Adds 4096mA of input current, 8064mA max.

Bit	Bit Name	Description
13		Not used.
14		Not used.
15		Not used.

SY20745 Data Byte Order

Each register in SY20745 contains 16-bits or 2, 8 bit bytes. All data sent on the SMBus is in 8 bit bytes and 2 bytes must be written or read from each register in SY20745. The order in which these bytes are transmitted appears reversed from the way they are normally written. The LO byte is sent first and the HI byte is sent second. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is sent second.

Writing to the Internal Registers

In order to set the charge current, charge voltage or input current, valid 16-bit numbers must be written to SY20745's internal registers via the SMBus.

To write to a register in the SY20745, the master sends a control byte with the R/W bit set to 0, indicating a write. If it receives an Acknowledge from the SY20745 it sends a register address byte setting the register to be written (i.e. 0x14 for the charge current register). The SY20745 will respond with an Acknowledge. The master then sends the lower data byte to be written into the desired register. The SY20745 will respond with an Acknowledge. The master then sends the higher data byte to be written into the desired register. The SY20745 will respond with an Acknowledge. The master then issues a Stop condition, indicating to the SY20745 that the current transaction is complete. Once this transaction completes the SY20745 will begin operating at the new current or voltage.

SY20745 does not support writing more than one register per transaction.

Reading from the Internal Registers

The SY20745 has the ability to read from 6 internal registers. Prior to reading from an internal register, the master must first select the desired register by writing to it and sending the register address byte. This process begins by the master sending a control byte with the R/W bit set to 0, indicating a write. Once it receives an Acknowledge from the SY20745 it sends a register address byte representing the internal register it wants to read. The SY20745 will respond with an Acknowledge. The master must then respond with a Stop condition. After the Stop condition the master follows with a new Start condition, then sends a new control byte with the SY20745 slave address and the R/W bit set to 1, indicating a read. The SY20745 will Acknowledge then send the lower byte stored in that register. After receiving the byte, the master Acknowledges by holding SDA low during the 9th clock pulse. SY20745 then sends the higher byte stored in the register. After the second byte neither device holds SDA low (No Acknowledge).

SY20745 does not support reading more than one register per transaction.

Application Information

The following battery charger design refers to the "Schematic Diagram" (see Figure 1.). This section describes how to select the external components including the inductor, input and output capacitors, switching MOSFET.

Inductor Selection

The SY20745 has three selectable fixed switching frequencies. Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charge current

(I_{CHG}) plus half of the ripple current (I_{Ripple}):

$$I_{SAT} \geq I_{CHG} + \frac{1}{2} \times I_{Ripple}$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle (D = V_{OUT}/V_{IN}), switching frequency (f_{SW}) and inductance (L):

$$I_{Ripple} = \frac{V_{IN} \times D \times (1-D)}{f_{SW} \times L}$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charge voltage range is from 9V to 12.6V for 3-cell battery pack. For 20V adapter voltage, 10V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20-40%) maximum charge current as a trade-off between inductor size and efficiency for a practical design.

Output Capacitor Selection

The output capacitor in parallel with the battery is used for absorbing the high frequency switching ripple current and smooth the output voltage. The RMS value of the output ripple current I_{RMS} is calculated as follow.

$$I_{RMS} = \frac{V_{IN}}{2 \times \sqrt{3} \times L \times f_{SW}} \times D \times (1-D)$$

Where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for CCM mode which is typical operation for the battery charger. During the battery charge period, battery voltage varies from its initial battery voltage to the rated voltage. Take 20V adapter voltage and 3 cell battery for example, the duty cycle varies from 0.375 for the minimum battery voltage of 7.5V to 0.63 for the maximum battery voltage of 12.6V. The maximum RMS value of the output ripple current occurs at the duty cycle of 0.5 and is expressed as follow.

$$I_{RMS\_MAX} = \frac{V_{IN}}{8 \times \sqrt{3} \times L \times f_{SW}}$$

For V_{IN} = 25V, 3 cell battery, L = 3.3μH, and f_{SW}=750 kHz, the maximum RMS current is 0.729A. A typical 20μF ceramic capacitor is a good choice to absorb this current and also has very small size. Organic polymer capacitors have high capacitance with small size and have a significant equivalent series resistance (ESR). Although ESR adds to ripple voltage, it also creates a high frequency zero that helps the closed loop operation of Buck converter.

Input Capacitor Selection

The input capacitor absorbs input ripple current from the Buck converter, which is given by below equation.

$$I_{RMS} = I_{CHG} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet. Non-tantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents when the adapter is plugged into the battery charger. For notebook battery charger applications, it is recommended that ceramic capacitors or polymer capacitors from Sanyo be used due to their small size and reasonable cost.

Power MOSFET Selection

Two external NFETs are used for synchronous switching charger. The gate drivers are internally integrated into the sample with 5.5V of gate drive voltage. 30V or higher voltage rating MOSFETs are preferred for 19-20V input voltage.

Figure of merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss.

$$FOM = R_{ds(on)} \times Q_g$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{ds(on)}$ has higher cost with the same package size.

The high side NFET loss includes conduction loss and switching loss. It relates with duty cycle(D), charge current (I_{CHG}), MOSFET's on resistance ($R_{ds(on)}$), input voltage (V_{IN}), switching frequency (f_{sw}), turn on time (t_{on}) and turn off time (t_{off}):

$$P_{HFET} =$$

$$D \times I_{CHG}{}^2 \times R_{ds(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (t_r + t_f) \times f_{SW}$$

The first part represents conduction loss. Usually MOSFET $R_{ds(on)}$ increases by 50% with 100°C junction temperature rise. The second part represents switching loss. The MOSFET turn on time and turn off time are defined as:

$$t_r = \frac{Q_{SW}}{I_r}, \quad t_f = \frac{Q_{SW}}{I_f}$$

where Q_{sw} is the switching charge, I_r is the turn on gate driving current and I_f is the turn off gate driving current. If Q_{sw} is not given in the datasheet, it can be estimated by gate-to-drain charge (Q_{gd}) and gate-to-source charge (Q_{gs}):

$$Q_{SW} = Q_{gd} + \frac{1}{2} \times Q_{gs}$$

Gate driving current can be estimated by VDD voltage (V_{VDD}), MOSFET plateau voltage ($V_{plateau}$), total turn-on
gate resistance (R_g_on) and turn-off gate resistance (R_g_off) of the gate driver:

$$I_r = \frac{V_{VDD} - V_{Plateau}}{R_{g\_on}}, \quad I_f = \frac{V_{Plateau}}{R_{g\_off}}$$

The conduction loss of the low-side MOSFET is calculated with the following equation when it operates in synchronous CCM mode.

$$P_{LFET} = (1-D) \times I_{CHG}{}^2 \times R_{ds(on)}$$

Layout Design

The rise and fall time of switching node LX are important for switching loss. Proper layout can minimize high frequency current path loop. This is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Below is list for proper layout.

1. Place input capacitor as close as possible to switching MOSFET's supply and ground connections and use shortest copper trace connection. These parts should be placed on the same layer of PCB instead of on different layers and using vias to make this connection.

2. The IC should be placed close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of switching MOSFETs.

3. Place inductor input terminal to switching MOSFET's output terminal as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charge current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

4. The charge current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path. Place decoupling capacitor on these traces next to the IC

5. Place output capacitor next to the sensing resistor output and ground.

6. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.

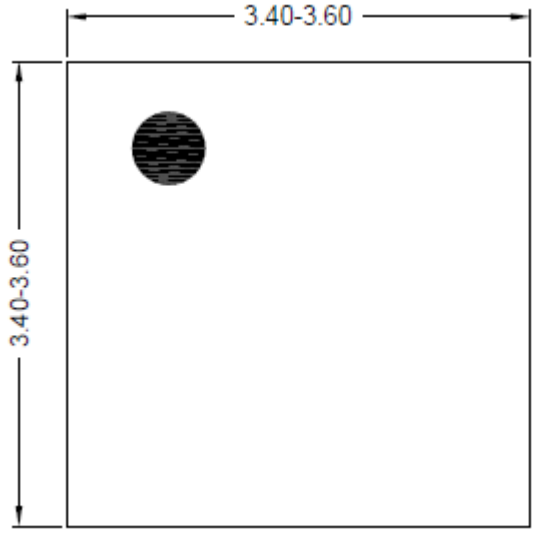
7. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling

8. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground (power pad should tie to analog ground in this case if possible).

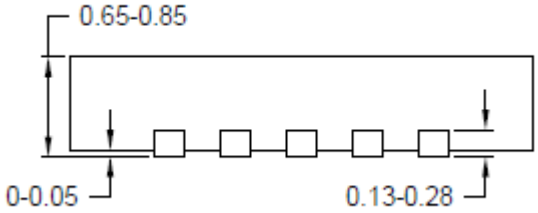
9. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible

10. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layer.

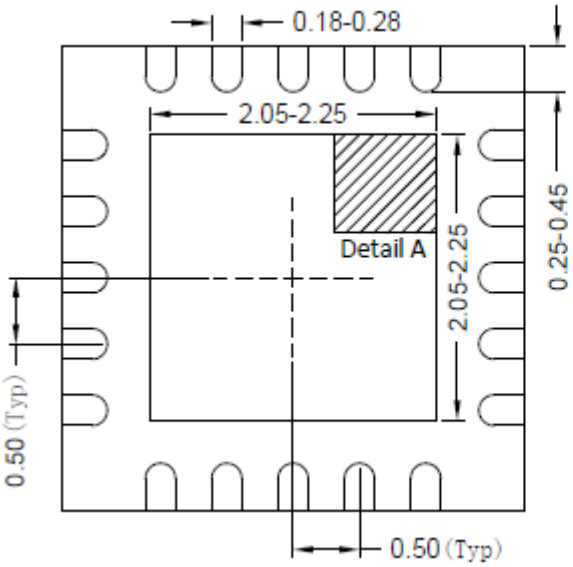
QFN3.5x3.5-20 Package Outline

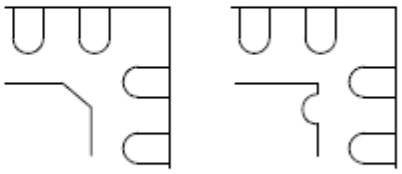


Top view



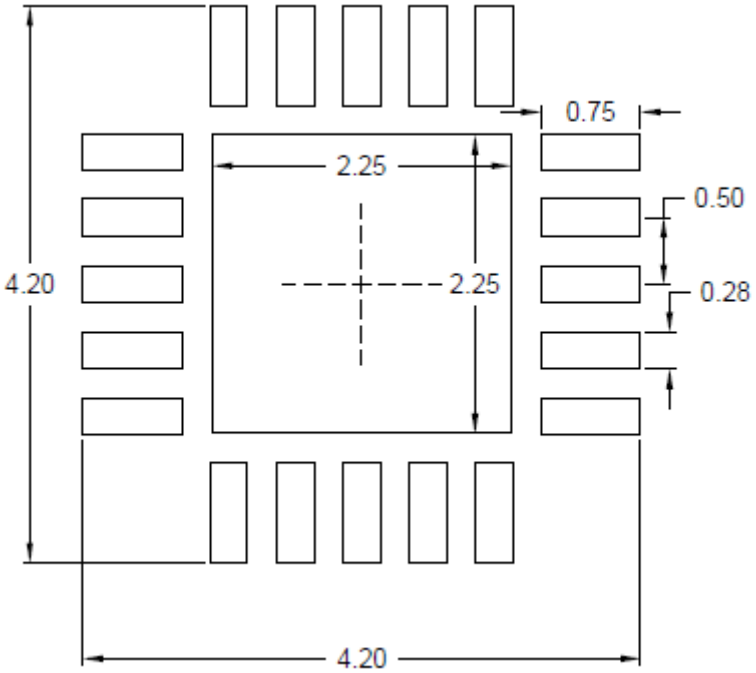
Side view





Detail A
Pin1 Identifier: two options

Bottom view



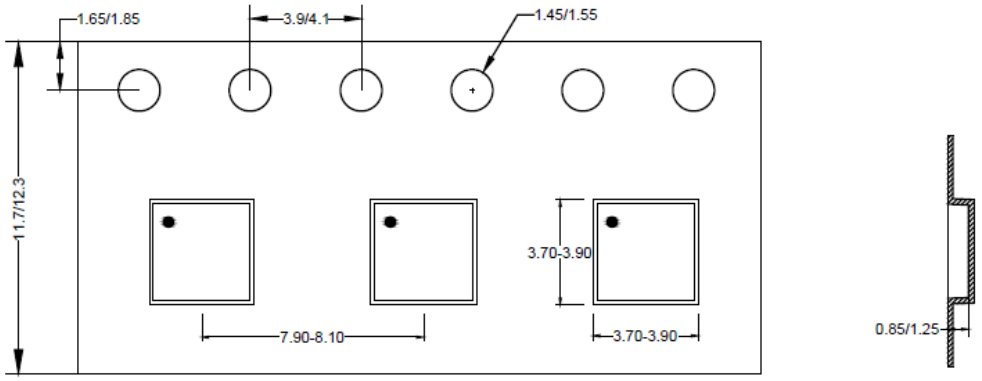
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

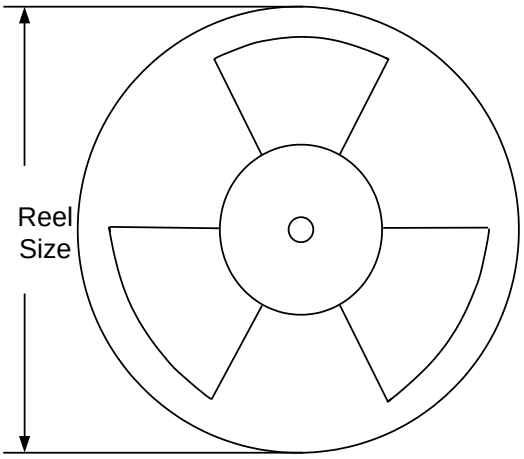
1. Taping orientation

QFN3.5x3.5



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3.5x3.5	12	8	13"	400	400	3000

3. Others: NA

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