SY20819E

Programmable High Current Protection Switch with -6V Reverse Voltage Protection

General Description

The SY20819E is an 18V, 5A protection switch with output voltage clamping. Extremely low $R_{DS(ON)}$ of the integrated protection N-channel MOSFETs helps to reduce the power loss during normal operation. The programmable soft-start time controls the slew rate of the output voltage during the start-up time.

The SY20819E can withstand a negative input voltage as low as -6V, protecting the load from being damaged by negative voltages.

Over-current and thermal limit protections are provided to enable reliable operation of the system.

The SY20819E is available in a compact QFN 2mm×2mm-9pin package.

Features

- Input Voltage Range: 2.95V to 6.5V with Surge Up to 18V
- 5A Output Current Capability
- Withstands -6V Input Voltage and Blocks the Power Path
- Extremely Low $R_{DS(ON)}$: 30mΩ at 3V V_{IN}
- Programmable Soft-Start Time
- Short Circuit Protection
- Selectable Clamping Output Voltage Threshold
- Power Good Indicator Pin for Operation Status
- FLG Indicator Pin for IN Status
- Thermal Shutdown Protection and Auto Recovery
- RoHS Compliant and Halogen Free
- Compact Package: QFN2×2-9

Applications

- SSD M.2 Form Factor
- SSD Dual Input Power Applications
- SSD Load Switch

Typical Application Circuit

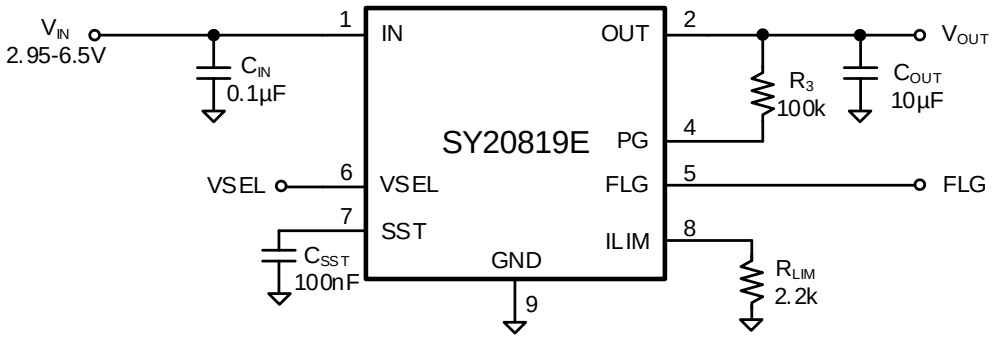


Figure 1. Schematic Diagram

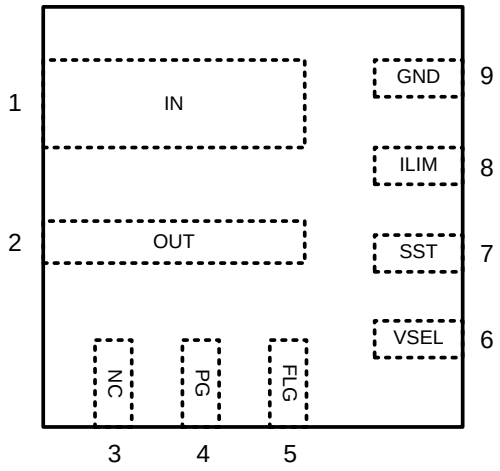
Ordering Information

Ordering Number	Package Type	Top Mark
SY20819ERYC	QFN2×2-9 RoHS Compliant and Halogen Free	**mF*xyz***

Device code: mF

***x=year code, y=week code, z= lot number code*)**

Pinout (Top View)



(QFN2×2-9)

Pin Name	Pin Number	Pin Description
IN	1	Power input pin. Decouple high frequency noise by connecting at least a 0.1μF MLCC capacitor to the ground.
OUT	2	Output voltage pin.
NC	3	No connection.
PG	4	Open-drain indicator pin. PG is high-impedance when the output voltage in the normal range. This pin cannot withstand negative voltage, do not connect IN power domain. Leave floating when not used.
FLG	5	Open-drain indicator pin. FLG is driven low when the input voltage is larger than UVLO. This pin cannot withstand negative voltage, do not connect IN power domain. Leave floating when not used.
VSEL	6	Output clamp voltage selection based on the input voltage. Pull the VSEL pin low by connecting a resistor to the ground in a 3.3V application or leave floating in a 5V application.

VSEL	VIN	Clamping Threshold		
		Min	Typ.	Max
LOW	3.3V	3.6V	3.8V	4V
Floating	5V	5.4V	5.7V	6V

SST	7	Soft-start time program pin. Connect a capacitor to the ground to program the soft-start time.
ILIM	8	Input current limit program pin. Connect a resistor between this pin and GND to program the input current limit.
GND	9	Ground pin.

Block Diagram

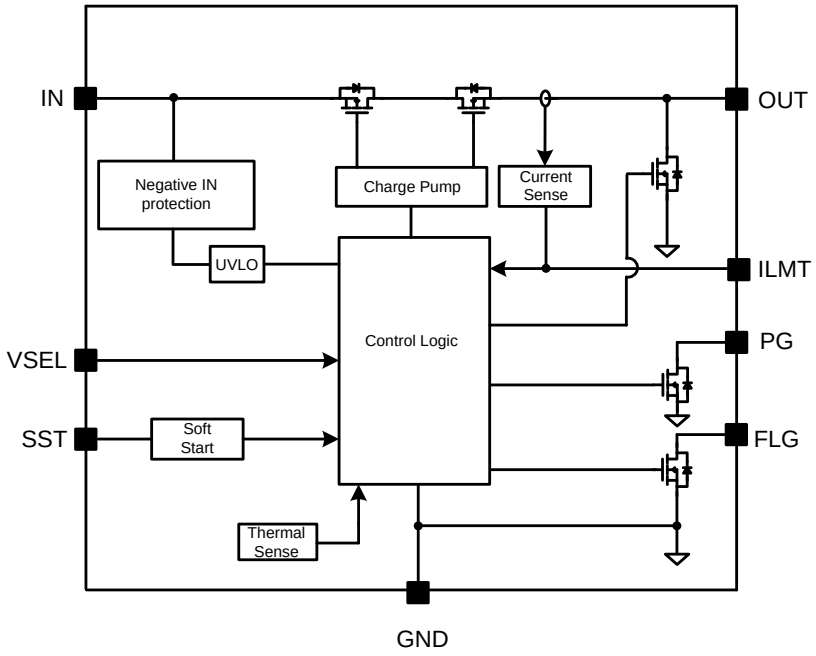


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-6	18	V
VSEL, PG, FLG	-0.3	18	
OUT	-0.3	7	
SST, ILIM	-0.3	3.6	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	35.5	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	14.3	
P_D Power Dissipation T_A = 25°C	2.8	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.95	6.5	V
VSEL, PG, FLG, OUT	0	6.5	
SST, ILIM	0	3.3	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 2.95V to 6.5V, C_{IN}=0.1μF, C_{OUT}=1μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Voltage Range	V_{IN}			2.95		6.5	V
Input UVLO Threshold	V_{UVLO}	VSEL=Low	Rising	2.7		2.9	V
			Falling	2.65		2.85	V
		VSEL=Floating	Rising	3.4		3.8	V
			Falling	3.25		3.75	V
Quiescent Current	I_Q	V_{IN}=5V, Null load			50	85	μA
Negative Current	I_{NEG}	V_{IN}=-6V, Flow from GND to IN			62	100	μA
Clamping Output Voltage	V_{CLP}	VSEL=LOW		3.6	3.8	4.0	V
		Leave VSEL floating		5.4	5.7	6.0	V
VSEL High Threshold	V_{SEL_HI}			1			V
VSEL Low Threshold	V_{SEL_LO}					0.4	V
Resistance of Power Path	R_{PWPT}	V_{IN}=3V, I_{OUT}=200mA, from IN to OUT			30	45	mΩ
		-40°C ≤ T_A ≤ 85°C				55	mΩ
Soft-start Time Program Range	t_{SST}	C_{SST}=100nF, T_A = 25°C		16.1	23	29.9	ms
Current Limit Accuracy	I_{LIM}	V_{IN}=5V, VSEL=floating (Note 5), R_{ILIM}=2.2kΩ		4.5	5	5.5	A
PG Low Voltage	V_{PGL}	I_{SINK}=1mA				0.2	V
PG Leakage Current	V_{PGLK}	V_{PG}=3.3V, PG high impedance				1	μA
PG Assert Delay Time	t_{PG}	V_{IN}=3.3V, C_{SST}=100nF, R_{LOAD}=0.82Ω, measure time from 90% of V_{IN} to PG pull high (Note 6)			25		ms
PG De-assert Delay Time	t_{PG-OFF}	V_{IN} from 3.3V to 5V within 1μs, VSEL=Low, V_{IN}=3.8V to PG pull down (Note 6)			15		μs
FLG Assert Delay Time	t_{FLG}	V_{IN} from 2.5V to 3.3V within 1μs, VSEL=Low, V_{IN}>UVLO to FLG pull low (Note 6)			40		μs
UVLO Delay Time	t_{UV_DLY}	V_{IN} from 3.3V to 2.5V within 40μs, VSEL=Low, V_{IN}<UVLO to Power FET turned off (Note 6)			25		μs
Turn On Delay Time	t_{ON_DLY}	V_{IN} from 0V to 5V by 100μs, C_{SST}=Null, C_{OUT}=10μF, null load, measure from V_{IN} over UVLO to V_{OUT} reach 10% of V_{IN} (Note 6)			500		μs
Output Voltage Clamp Delay Time	t_{CLMP_DLY}	V_{IN} from 3V to 5V within 1μs, VSEL=Low, C_{OUT}=10μF, R_L=10Ω, measure time from V_{OUT} over 3.8V to peak voltage (Note 6)			660		ns
FLG Low Voltage	V_{FAL}	I_{SINK}=1mA				0.2	V
FLG Leakage Current	V_{FALK}	V_{PG}=3.3V, FLG high impedance				1	μA
Discharge Resistance	R_{DSG}	V_{IN}=2.0V, V_{OUT}=0.1V			35	50	Ω
Thermal Shutdown Temperature	T_{SD}				150		°C
Thermal Shutdown Hysteresis	T_{HYS}				20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a Silergy test board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4. Recommended Soft-Start Time Program Table

Recommended formulas for C_{SST} and soft-start time calculations. Use the following formula if there is no external C_{SST}:

$$t_{SS} = t_{SS\_DLT}$$

When longer soft-start time is required, the capacitor can be calculated using the following equation:

$$t_{SS} = \frac{0.85 \times C_{SST}}{I_{INT}},\ t_{SS} > t_{SS\_DLT}$$

Where:

- t_{SS_DLT} is the internally fixed default soft-start time of 0.6ms (typ.) without using an external capacitor
- I_{INT} is the internal current source with a value of 3.7μA (typ.).

The soft-start time programming table and tolerances are shown below:

C_{SST}(nF)	Min(ms)	Typ(ms)	Max(ms)
None	0.384	0.6	1.61
3.3	0.531	0.758	1.61
4.7	0.756	1.08	1.404
10	1.61	2.3	2.99
47	7.56	10.8	14.04
100	16.1	23	29.9

Note 5. Recommended Current Limit Program Table:

Current Limit Resistance (kΩ)	11	5.5	4.4	3.7	3.1	2.8	2.4	2.2
Current Limit (A)	1.0	2.0	2.5	3.0	3.5	4.0	4.5	5.0

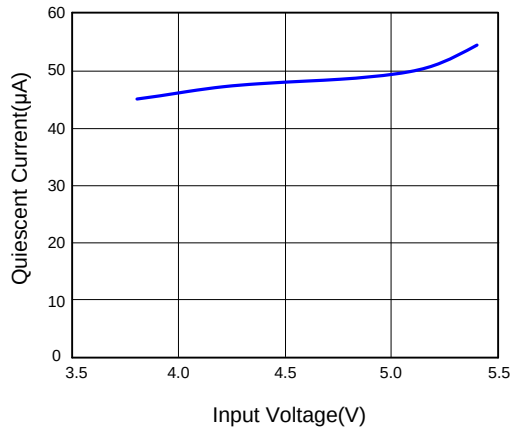
Recommended formula for R_{LIM} and current limit calculation:

$$R_{LIM} = \frac{11k}{I_{LIM}}(\Omega)$$

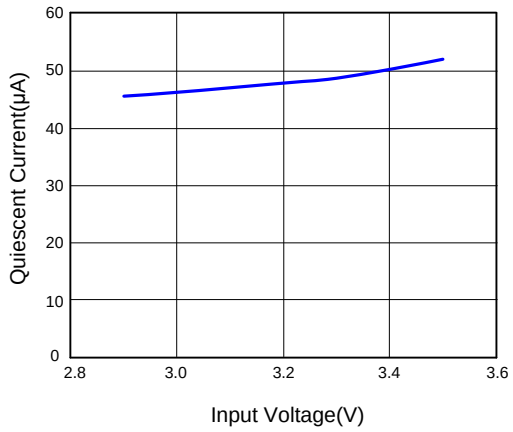
Note 6: Guaranteed by design.

Typical Performance Characteristics

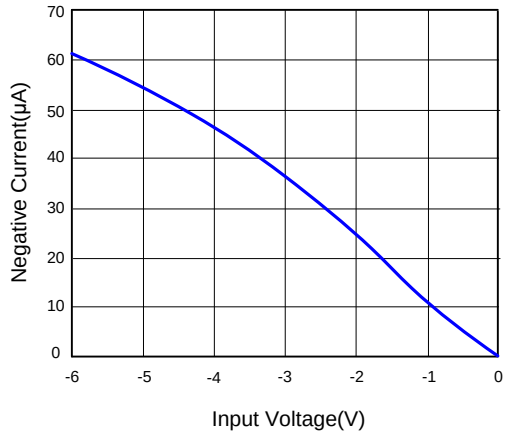
Quiescent Current vs. Input Voltage
(VSEL= Floating, C_{IN}=0.1μF,C_{OUT}=10μF)



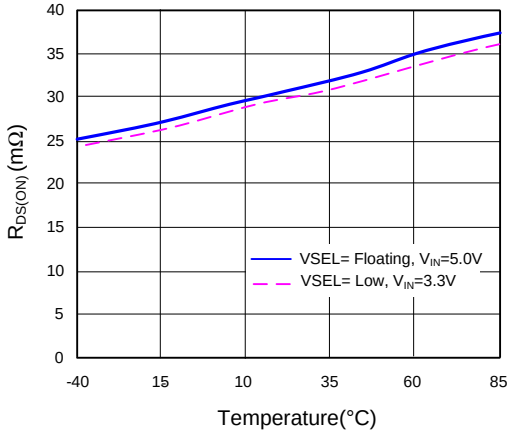
Quiescent Current vs. Input Voltage
(VSEL=Low, C_{IN}=0.1μF,C_{OUT}=10μF)



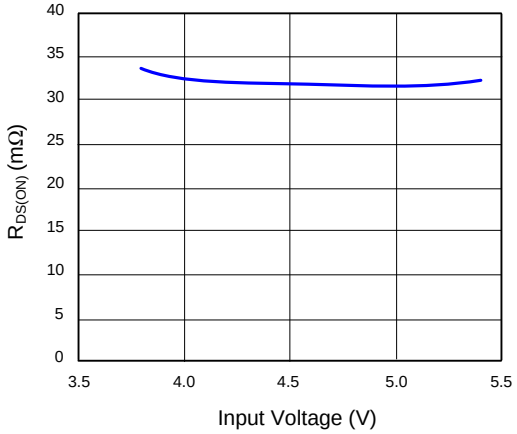
Negative Current vs. Input Voltage



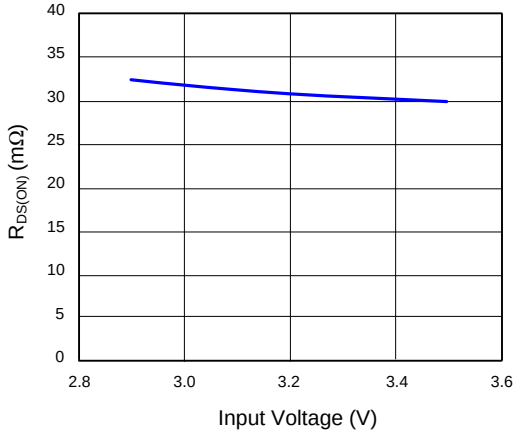
$R_{DS(ON)}$ vs. Temperature



$R_{DS(ON)}$ vs. Input Voltage
(VSEL= Floating, C_{IN}=0.1μF,C_{OUT}=10μF,I_{OUT}=1A)

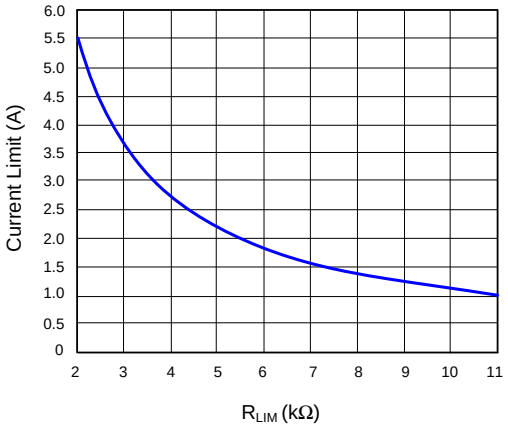


$R_{DS(ON)}$ vs. Input Voltage
(VSEL=Low, C_{IN}=0.1μF,C_{OUT}=10μF,I_{OUT}=1A)



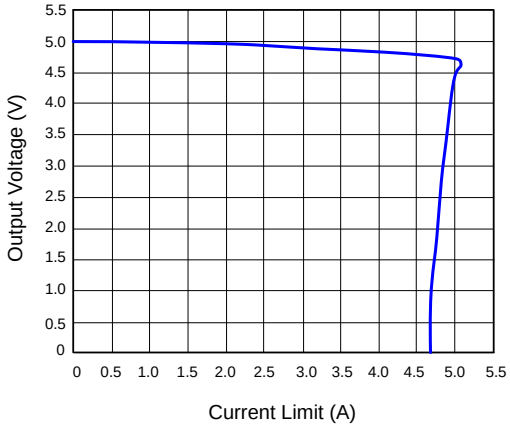
Current Limit vs. R_{LIM}

(VSEL=Floating, V_{IN}=5V)



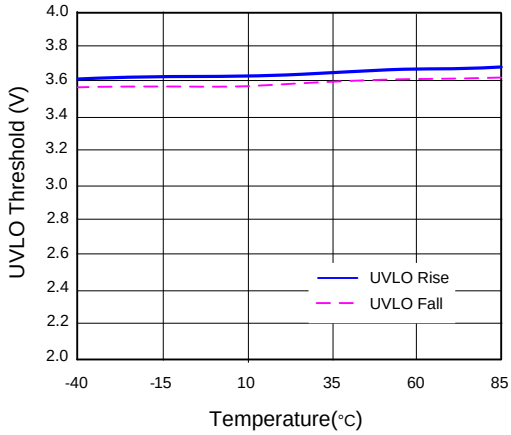
Current Limit vs. Output Voltage

(V_{IN}=5V, C_{IN}=0.1μF, C_{OUT}=10μF, R_{LIM}=2.2kΩ)



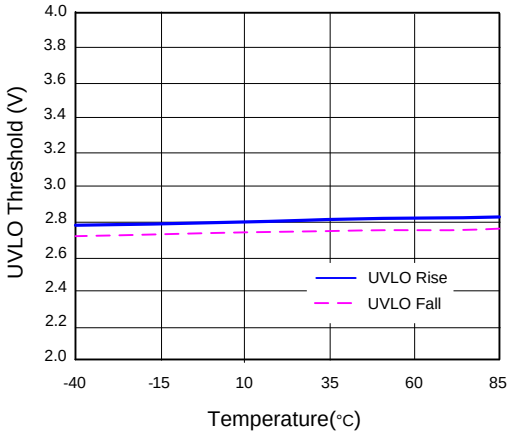
UVLO Threshold vs. Temperature

(VSEL= Floating, C_{IN}=0.1μF,C_{OUT}=10μF)

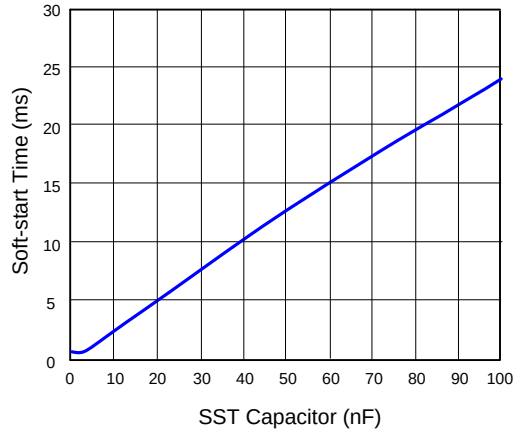


UVLO Threshold vs. Temperature

(VSEL= Low, C_{IN}=0.1μF,C_{OUT}=10μF)

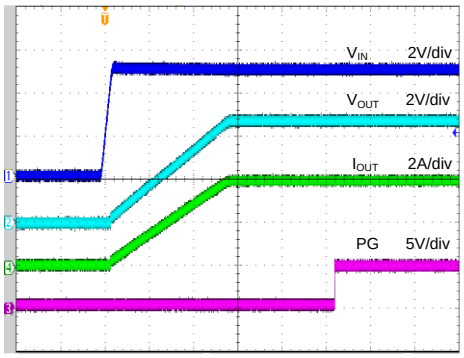


Soft-start Time vs. SST Capacitor



Startup from V_{IN}

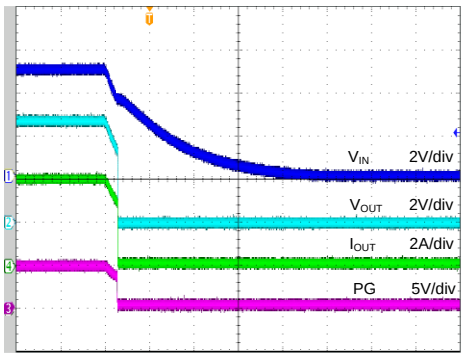
(V_{IN}=5V,VSEL=Floating, C_{IN}=0.1uF, C_{OUT}=10uF, R_{ILIM}=2.2kΩ, C_{SST}=100nF, R_L=1.25Ω)



Time (10ms/div)

Shutdown from V_{IN}

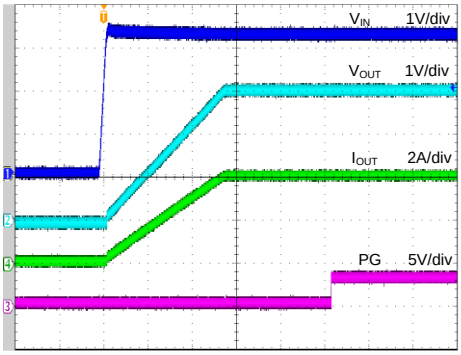
(V_{IN}=5V,VSEL=Floating, C_{IN}=0.1uF, C_{OUT}=10uF, R_{ILIM}=2.2kΩ, C_{SST}=100nF, R_L=1.25Ω)



Time (4ms/div)

Startup from V_{IN}

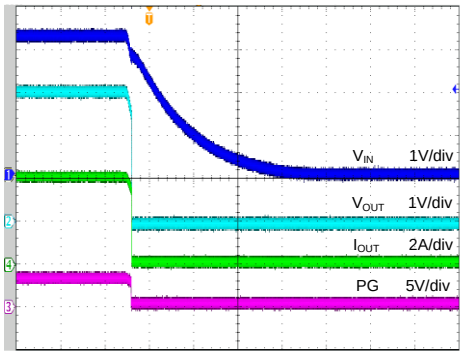
(V_{IN}=3.3V,VSEL=Low, C_{IN}=0.1uF, C_{OUT}=10uF, R_{ILIM}=2.2kΩ, C_{SST}=100nF, R_L=0.82Ω)



Time (10ms/div)

Shutdown from V_{IN}

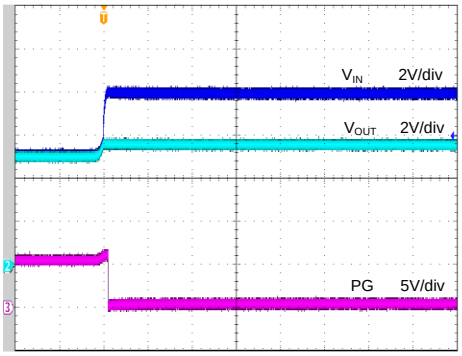
(V_{IN}=3.3V,VSEL=Low, C_{IN}=0.1uF, C_{OUT}=10uF, R_{ILIM}=2.2kΩ, C_{SST}=100nF, R_L=0.82Ω)



Time (4ms/div)

Clamp Protection Response

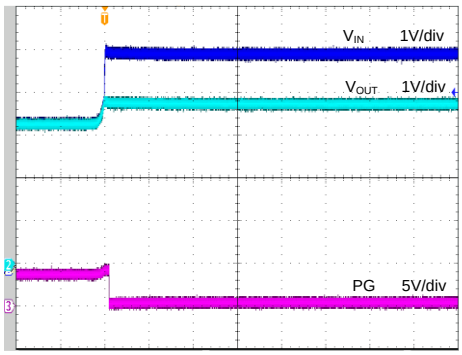
(V_{IN}=5V to 8V,VSEL=Floating, C_{IN}=0.1uF, C_{OUT}=10uF, R_{ILIM}=2.2kΩ, Null Load)



Time (100μs/div)

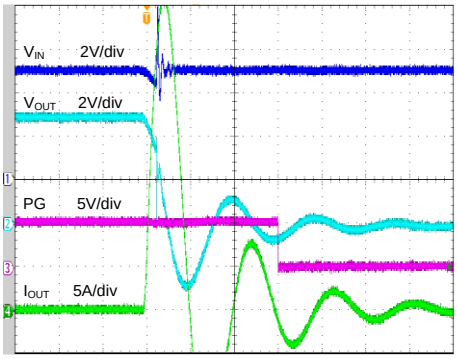
Clamp Protection Response

(V_{IN}=3.3V to 5V,VSEL=Low, C_{IN}=0.1uF, C_{OUT}=10uF, R_{ILIM}=2.2kΩ, Null Load)



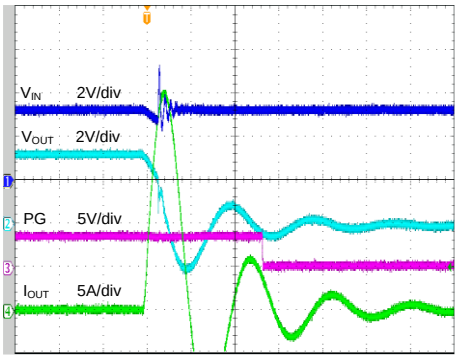
Time (100μs/div)

Short Circuit Response
(V_{IN}=5V, VSEL=Floating, C_{IN}=0.1μF,C_{OUT}=10μF)



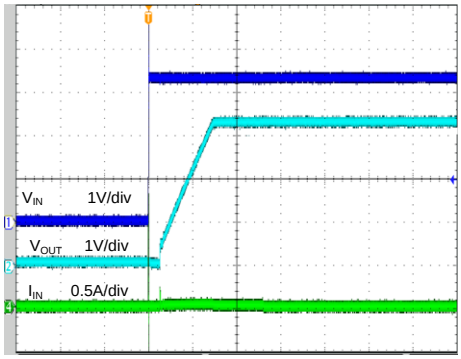
Time (4μs/div)

Short Circuit Response
(V_{IN}=3.3V, VSEL=Low, C_{IN}=0.1μF,C_{OUT}=10μF)



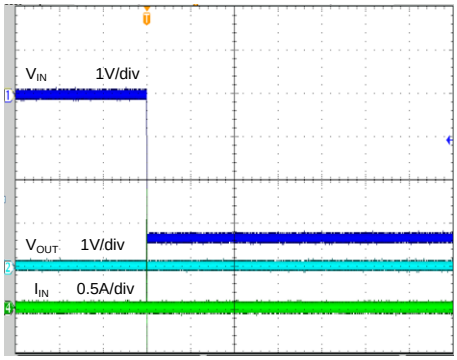
Time (4μs/div)

3.3V Hot Plug Response
(V_{IN}=3.3V,V_{SEL}=Low, C_{IN}=0.1μF, C_{OUT}=10μF)



Time (2ms/div)

Negative 3.3V Hot Plug Response
(V_{IN}=-3.3V,V_{SEL}=Low, C_{IN}=0.1μF, C_{OUT}=10μF)



Time (2ms/div)

Application Information

The SY20819E N-channel MOSFET power switch with programmable current limit, designed for high-side load-switching applications. It incorporates back-to-back N-channel MOSFETs, to prevent current flow from OUT to IN when OUT is externally forced to a higher voltage than IN and the chip is disabled.

Overcurrent Protection:

The SY20819E allows for current limit programming by connecting a resistor R_{LIM} from the ILIM pin to the ground. For optimal stability of the internal regulation loop, it's recommended to use a 1% resistor within the range of 2.2kΩ to 11kΩ for R_{LIM}.

The current limit value can be calculated using the following equation:

$$I_{LIM} = \frac{11k}{R_{LIM}} (A)$$

When an overcurrent condition is sensed, the gate of the pass switch is controlled to achieve a constant output current. If the overcurrent condition persists for a long time, the junction temperature may exceed 150°C, and overtemperature protection will shut down the part. Once the chip temperature drops below 130°C, the part will restart. The PG will be pulled down when an overcurrent event happens.

UVLO Protection:

The SY20819E incorporates undervoltage lockout (UVLO) protection by monitoring the input voltage (IN). If the IN voltage falls below the UVLO threshold voltage, the main power MOSFETs will automatically shut down. Note that this protection mechanism does not include a deglitch time and operates as a non-latch protection.

Output Voltage Clamp Protection:

The SY20819E integrates an output voltage clamp function to protect the system from overvoltage damage. When VOUT exceeds the configured output voltage clamp value, the SY20819E will control the gate of the main MOSFETs to regulate output voltage at the clamp value.

Output Voltage Select Function:

The SY20819E features an integrated select output voltage for the input pin. For a 5V application, leaving the VSEL pin floating will result in the output voltage being clamped at 5.7V (typ.), with an input UVLO threshold of 3.6V (typ.). For a 3.3V application, connect a resistor (0~10kΩ) from the VSEL pin to the ground. In this configuration, the output voltage will be clamped at 3.8V (typ.), and the input UVLO threshold will be 2.8V (typ.). The PG pin will be pulled down when the output voltage is clamped.

Power Good Indication (PG):

The power-good status for the supply is conveyed through the PG open-drain output. Typically, an external pull-up resistor is used to pull PG high. The PG output becomes high-impedance when the power switch is fully turned on. The PG output will be pulled down in situations where the output voltage is clamped or an overcurrent occurs. It is essential to note that connecting IN directly is prohibited in applications with a risk of reverse plug.

Fault Flag (FLG):

The FLG output open-drain will be asserted (active low) when the input voltage is larger than the UVLO threshold. FLG may be left floating when not used.

Supply Filter Capacitor:

In order to prevent input voltage dropping during hotplug events, a 0.1μF ceramic capacitor from VIN to GND is strongly recommended. Higher capacitor values can further reduce input voltage drop. Without an input capacitor, an output short can cause ringing on the input, which could destroy the internal circuitry when the input transient exceeds the absolute maximum supply voltage, even for a short duration.

Output Filter Capacitor:

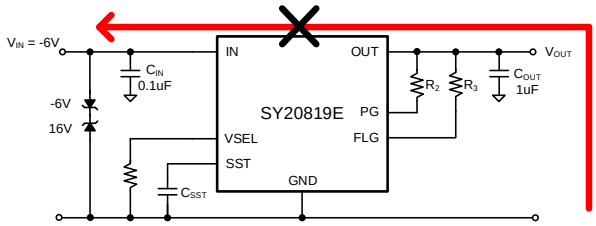
A 1μF output ceramic capacitor is recommended to be placed close to the device and output connector to reduce voltage drop during load transients. Higher output capacitor values can further reduce the drop during high-current applications.

Power Path Blocking for Negative VIN Plug-In:

The SY20819E is designed to withstand a maximum negative voltage of -6V. In the event of a reverse supply to the IN pin, the SY20819E will maintain the power path in the off state, blocking the power path from GND to IN. This protection mechanism ensures that the load connected to the SY20819E is not damaged by a negative power supply. Additionally, when the input voltage goes above the UVLO threshold, the SY20819E initiates a soft-start sequence.

In hotplug applications, where the supply voltage may experience a ringing effect exceeding -6V, it is strongly recommended to incorporate a -6V TVS (Transient Voltage Suppressor) between the IN and GND pins to ensure that the input voltage remains within the absolute minimum allowable range. For applications where both positive and negative voltages can exceed the absolute

maximum rating for the part, two TVS devices can be used as shown below:



Auto Output Capacitor Discharge:

The SY20819E includes an auto-output capacitor discharge function. When IN falls below the UVLO threshold, the power MOSFETs are shut down, and a discharge MOSFET is activated to discharge the output capacitor(s). In the absence of input voltage (IN at 0V), the output voltage can be discharged to a maximum of 0.9V.

PCB Layout Guide:

For best performance of the SY20819E, the following guidelines must be strictly followed:

1. Keep all VBUS traces as short and wide as possible and use at least 2-ounce copper for all VBUS traces.
2. Place the output capacitor as close to the connectors as possible to lower the impedance and inductance between the port and the capacitor and improve transient performance.
3. Place the input and output capacitors close to the device and connect them to the ground plane to reduce noise coupling.

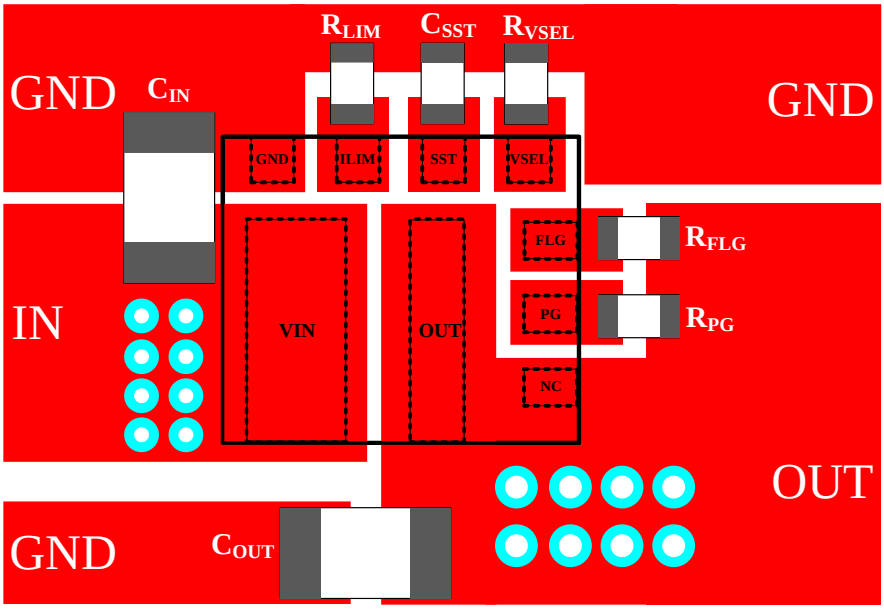
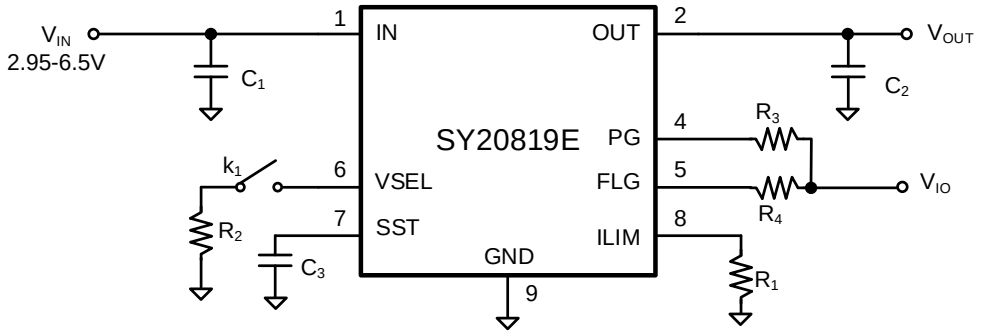


Figure 3. PCB Layout Suggestion

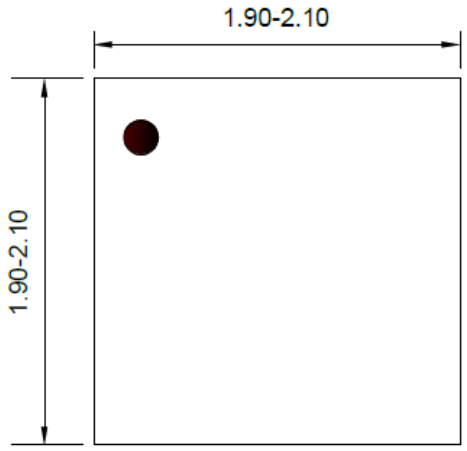
Schematic



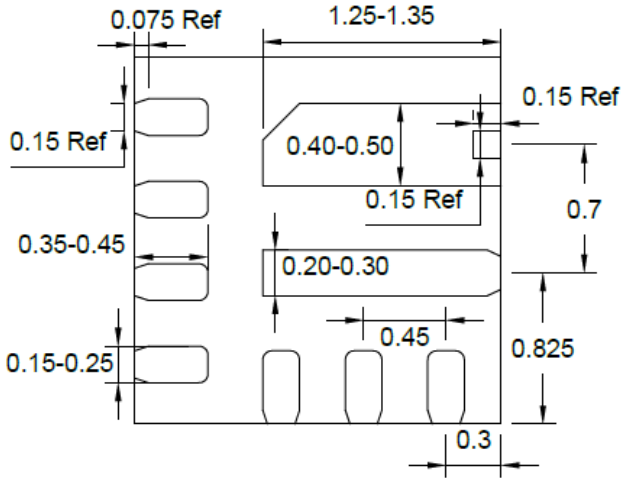
BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1	1μF/25V, 1206, X5R	GRM319R61E105KA12D	Murata
C_2	10μF/25V, 1206, X5R	GRM319R61E106KA12D	Murata
C_3	100nF/50V, 0603, X5R	GRM188R61H104KA93D	Murata
R_1	2.2kΩ, 0603	RC0603FR-072K2L	YAGEO
R_2	0Ω, 0603	RC0603FR-070RL	YAGEO
R_3, R_4	100kΩ, 0603	RC0603FR-07100KL	YAGEO

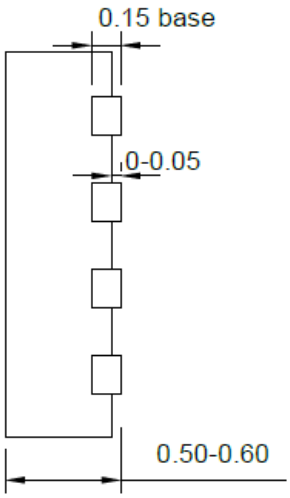
QFN2×2-9 Package Outline & PCB Layout



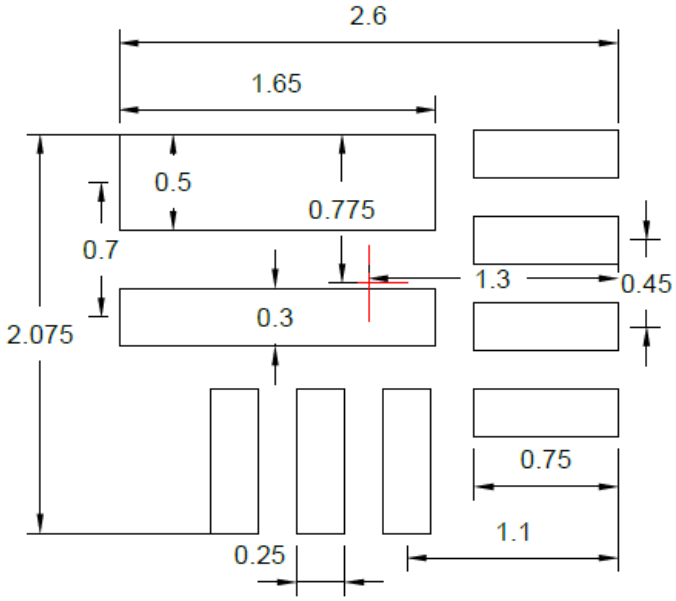
Top View



Bottom View



Side View

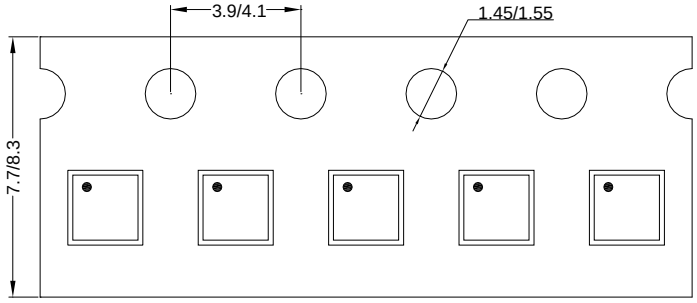


PCB Layout (Recommended)

Notes: 1. All dimensions are in millimeters and exclude mold flash and metal burr.
2: The center of the PCB diagram refers to the chip center.

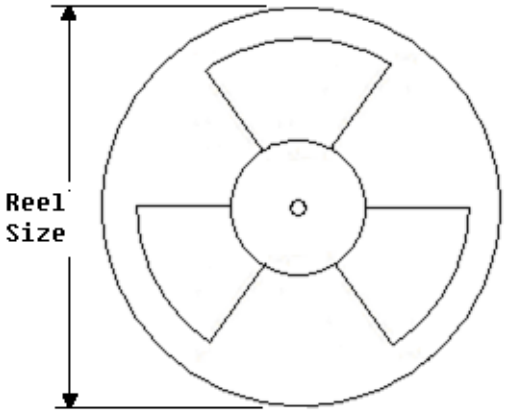
Taping & Reel Specification

QFN2×2 Taping Orientation



Feeding direction ⟶

Carrier Tape & Reel Specification for Packages



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
QFN2×2	8	4	7"	400	160	3000

Revision History

Date	Revision	Change
Dec.12, 2023	Revision 1.0	Language improvements for clarity
Oct.11, 2019	Revision 0.9	Initial Release

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please make sure that you have the latest revision.

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