SY20109

400nA ultra low I_Q, 1.0MHz, 500mA Synchronous Step Down Regulator

General Description

The SY20109 is a 400nA ultra low quiescent current, 1.0MHz synchronous step down DC/DC regulator capable of delivering up to 500mA output current. It can operate over a wide input voltage range from 2.2V to 6.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved at 1.0MHz switching frequency.

Ordering Information

SY20109 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20109DFC	DFN2×2-8	--

Features

- 2.2~6.5V Input Voltage Range
- Ultra Low Quiescent Current Down to 400nA
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom) 300mΩ /130mΩ
- Instant PWM Control to Achieve Ultra Fast Load Transient Speed
- High Switching Frequency 1.0MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- Power Good Indicator
- Hiccup Mode for Output Short Circuit Protection
- 100% Drop Out Operation
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: DFN2×2-8

Applications

- Battery Powered Applications
- Consumer and Portable Medical Products
- Personal Ware Products

Typical Applications

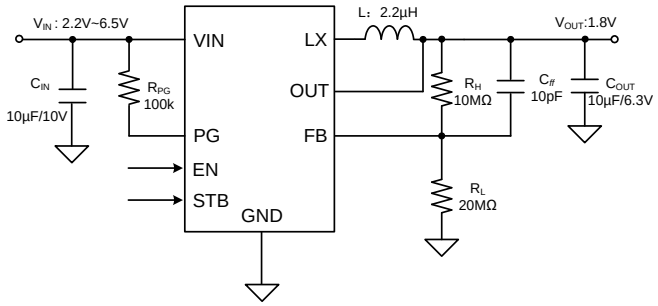


Figure1. Schematic Diagram

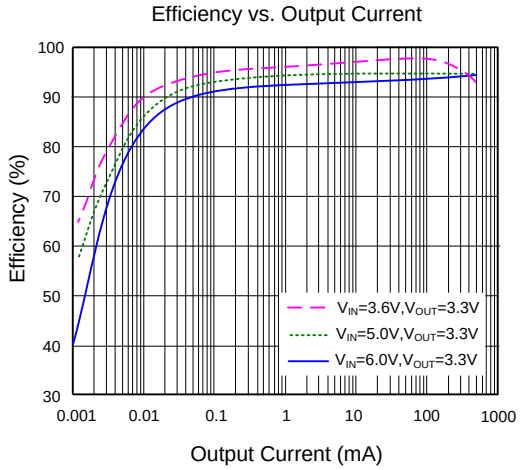
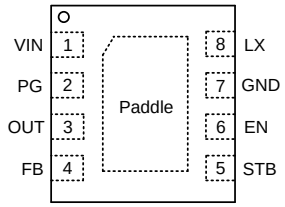


Figure2. Efficiency vs. Output Current

Pinout (Top View)



(DFN2×2-8)

Top Mark: gE*xyz* (device code: gE, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
VIN	1	Power input pin. Decouple this pin to the GND pin with at least a 10µF ceramic capacitor.
PG	2	Power good indicator (open-drain output). Low if the output < 90% of the regulation; high otherwise. Connecting a pull-up resistor to the input.
OUT	3	Output voltage feedback pin. Connecting this pin to the output side.
FB	4	Connecting this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=1.2V\times(1+R_H/R_L)$.
STB	5	This pin controls the standby mode. With STB = low, deep standby function will be activated, I_Q=400nA. With STB = high, deep standby function will be disabled, I_Q=15µA.
EN	6	Enable control. Pulled high to turn on. Do not leave it floating.
GND	7	Power ground pin.
LX	8	Inductor pin. Connect this pin to the switching node of the inductor.

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 7V
PG, OUT, STB, EN---------- -0.3V to V_{IN} + 0.6V
LX Voltage ---------- -0.3V (*1) to 7V (*2)
Power Dissipation, P_D @ T_A = 25°C,
DFN2×2-8 ---------- 1.1W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 85°C /W
θ_{JC} ---------- 45°C /W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
(*1) LX Voltage Tested Down to -3V<20ns
(*2) LX Voltage Tested Up to +7.5V<20ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.2V to 6.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5.0V, V_{OUT} = 1.8V, L = 2.2µH, C_{OUT} = 10µF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.2		6.5	V
Input UVLO Threshold	V_{UVLO}				2.2	V
Input UVLO Hysteresis	V_{HYS}			0.35		V
Quiescent Current	I_Q	V_{FB}=V_{REF}×115% , STB=0		400	600	nA
		V_{FB}=V_{REF}×115% , STB=1		15		µA
Shutdown Current	I_{SHDN}	V_{EN}=0V		10	100	nA
Feedback Reference Voltage	V_{REF}		1.182	1.2	1.218	V
LX Node Discharge Resistance	R_{DIS}			10		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			300		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			130		mΩ
EN Input Voltage High	$V_{EN,H}$		1.1			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
Power Good Threshold	V_{PG}	V_{FB} rising (good)		90		%V_{REF}
Power Good Delay	$t_{PG,F}$	High to low		20		µs
Min ON Time	$t_{ON,MIN}$			80		ns
Maximum Duty Cycle	D_{MAX}		100			%
Turn-on Delay	$t_{ON,DLY}$	from EN high to LX start switching		600		µs
Switching Frequency	f_{SW}	V_{OUT}=1.2V, I_{OUT}=500mA		1		MHz
Top FET Current Limit	$I_{LMT,TOP}$		0.9		1.5	A
Bottom FET Current Limit	$I_{LMT,BOT}$		0.5			A
Output Under Voltage Protection Threshold	$V_{UVP.OUT}$	V_{OUT} threshold		1		V
Output UVP Delay	$t_{UVP,DLY}$			20		µs
UVP Hiccup ON Time	$t_{UVP,ON}$			0.25		ms
UVP Hiccup OFF Time	$t_{UVP,OFF}$			0.25		ms
Thermal Shutdown Temperature	T_{SD}			150		ºC
Thermal Shutdown Hysteresis	T_{HYS}			15		ºC

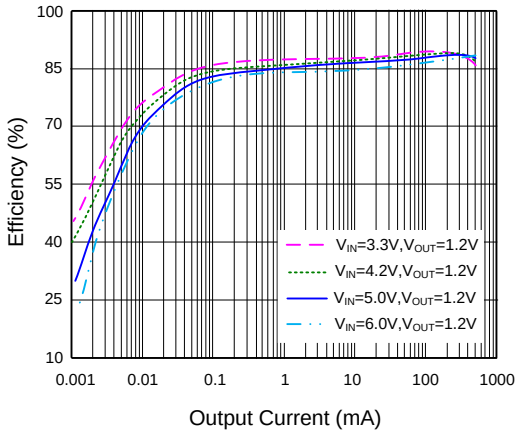
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY20109DFC is measured in the natural convection at T_A = 25°C on 2OZ two-layer Silergy evaluation board. Paddle of DFN2×2-8 package is the case position for SY20109DFC θ_{JC} measurement.

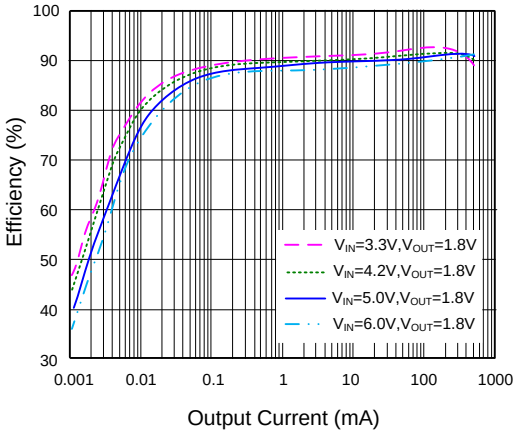
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

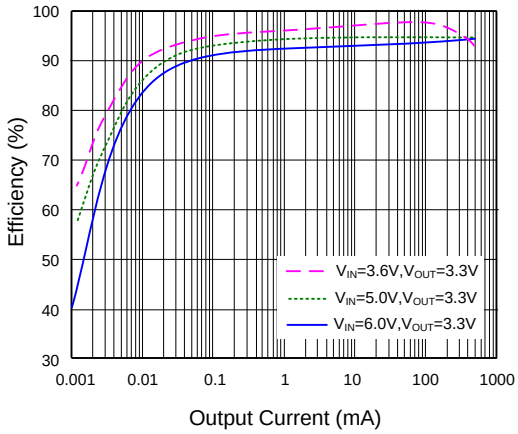
Efficiency vs. Output Current



Efficiency vs. Output Current

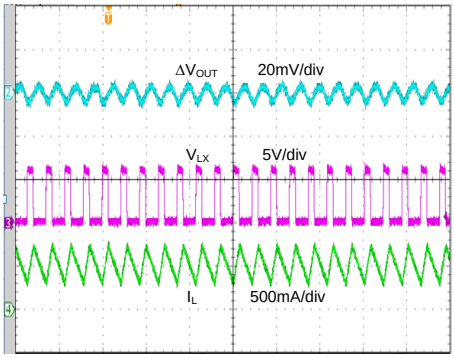


Efficiency vs. Output Current



Output Ripple

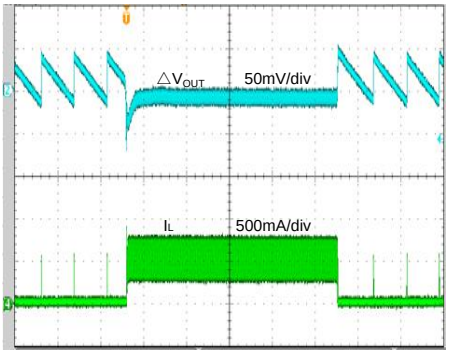
(V_{IN}=6.0V, V_{OUT}=1.8V, I_{OUT}=500mA)



Time (2μs/div)

Load Transient

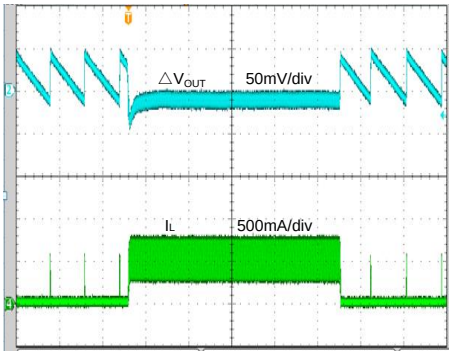
(V_{IN}=5V, V_{OUT}=1.8V, STB=0, I_{OUT}=0.5mA~500mA)



Time (100μs/div)

Load Transient

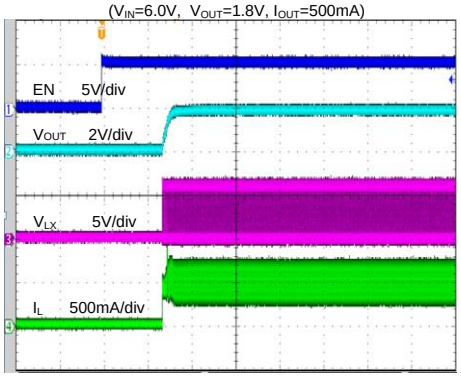
(V_{IN}=5V, V_{OUT}=1.8V, STB=1, I_{OUT}=0.5mA~500mA)



Time (100μs/div)

Startup from Enable

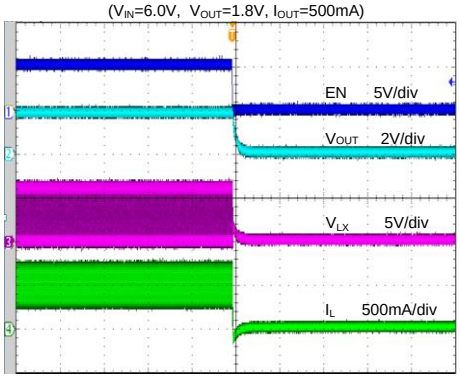
(V_{IN}=6.0V, V_{OUT}=1.8V, I_{OUT}=500mA)



Time (400μs/div)

Shutdown from Enable

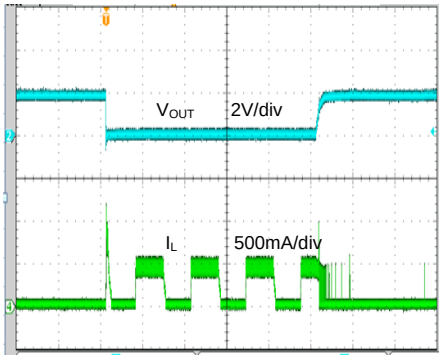
(V_{IN}=6.0V, V_{OUT}=1.8V, I_{OUT}=500mA)



Time (400μs/div)

Short Circuit Protection

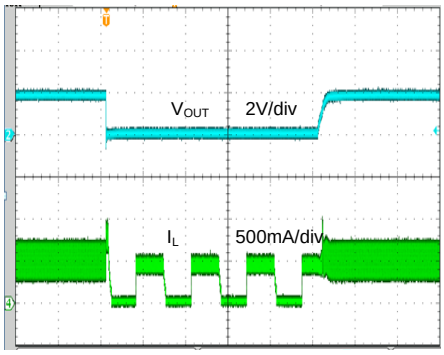
(V_{IN}=6.0V, V_{OUT}=1.8V,I_{LOAD}=0A~Short)



Time (400μs/div)

Short Circuit Protection

(V_{IN}=6.0V, V_{OUT}=1.8V,I_{LOAD}=500mA~Short)



Time (400μs/div)

Operation

The SY20109 is a high efficiency, 1.0MHz synchronous step down DC/DC regulator capable of delivering up to 500mA output current. It can operate over a wide input voltage range from 2.2V to 6.5V and integrates main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss.

Low output voltage ripple, small external inductor and capacitor sizes are achieved at 1.0MHz switching frequency.

Applications Information

Because of the high integration in the SY20109, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L, the feedback resistors (R_H and R_L) and the feed-forward capacitor C_{ff} need to be selected for the targeted application specifications.

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 10MΩ and 50MΩ is highly recommended for both resistors. If R_L =20MΩ is chosen, then R_H can be calculated to be:

$$R_H = \frac{(V_{OUT} - 1.2\,V)\cdot R_L}{1.2V}$$

Feed-forward Capacitor C_{ff}

The feed-forward capacitor is needed to achieve good stability and fast dynamic response. At least a 10pF ceramic capacitor is recommended for the application.

Input Capacitor C_{IN}

A typical X5R or a better grade ceramic capacitor with 10V rating and greater than 10µF capacitance is recommended. Place this ceramic capacitor really close to the IN and GND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<25mΩ to achieve a good overall efficiency.

Inductor vs. Output Capacitor

The instant PWM control strategy needs very little C_{OUT} to confirm stability. Too large inductor and C_{OUT} will lead to instability. The recommend inductance and output capacitor is shown as below.

Inductance vs. Output Capacitor Selection Table

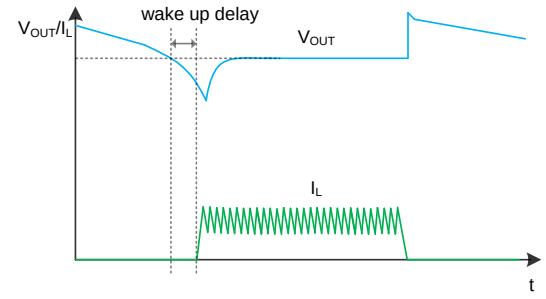
L	C_{OUT}				
	10µF	22µF	80µF	120µF	350µF
2.2µH	√	√	√	√	√
4.7µH	√	√	√	√	×
6.8µH	√	√	√	×	×

OCP and SCP Protection Method

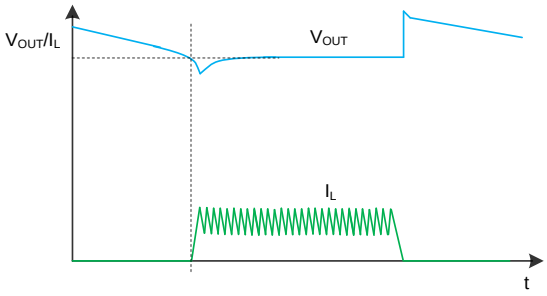
With load current increasing, as soon as the high side FET current gets higher than the peak current limit threshold, the high side FET will turn off and the low side FET will keep turning on until low side FET current decreases below the valley current limit threshold. If peak current limit is trigged twice, the valley current limit threshold will fold-back to 65%.
If the load current continues to increase, the output voltage will drop. When the output voltage falls below 1V, the output UVP will be detected and SY20109 will operate in hiccup mode. The hiccup frequency is 2kHz and the hiccup duty cycle is 50%. If the hard short is removed, the IC will return to normal operation.

STB Pin Function

Two stage quiescent current can be selected via STB pin. If STB=1, the quiescent current will be 15μA (typical). If STB=0, the quiescent current can be decreased to 400nA, while extra 3μs delay time will be needed when SY20109 wakes up from the standby mode. As a side effect, the output undershot will be intensified if a dynamic load is attached to the output side in null load condition.



(a) STB=0



(b) STB=1

Figure3. Load Transient Response

Bypass Mode

The SY20109 will enter 100% bypass mode when the input voltage is close to the output voltage. Once the input voltage falls below the bypass enter threshold V_{TH-}, the SY20109 will keep turning on the high side FET for 100% bypass mode. Because the output is connected to the input, the output voltage will track the input voltage minus the voltage drop across the internal high side FET and inductor, which is caused by the inductor current. Once the input voltage increases and trigger the bypass leave threshold V_{TH+}, the SY20109 will exit the 100% bypass mode and start switching again.

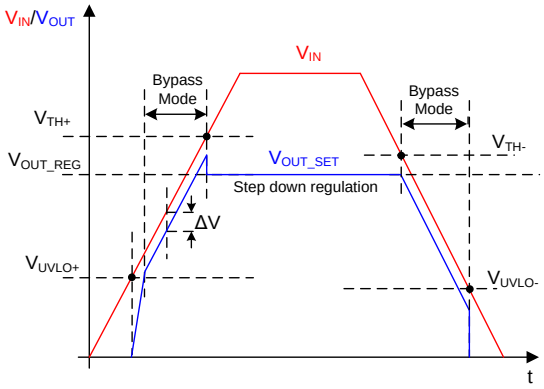


Figure4. Bypass Mode Transition

The V_{TH+}, V_{TH-}, ΔV can be calculated as below:

$V_{TH+}=V_{OUT\_SET}\times 1.03\%+I_{OUT}\times(DCR_L+R_{DS(ON)1})$

$V_{TH-}=V_{OUT\_SET}+I_{OUT}\times(DCR_L+R_{DS(ON)1})$

$\Delta V=I_{OUT}\times(DCR_L+R_{DS(ON)1})$

Layout Design

The layout design of the SY20109 is relatively simple. For the best efficiency and to minimize noise problems, we should place the following components close to the IC: C_{IN}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane will be highly desirable. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.
2) C_{IN} must be close to pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
4) The components R_H and R_L, and the trace connecting to the FB pin and OUT pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

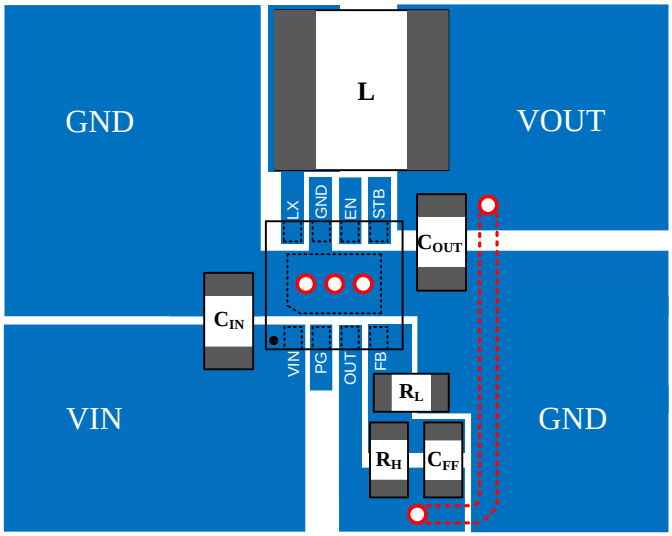
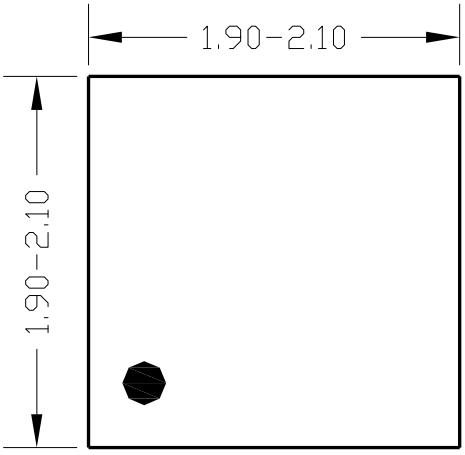
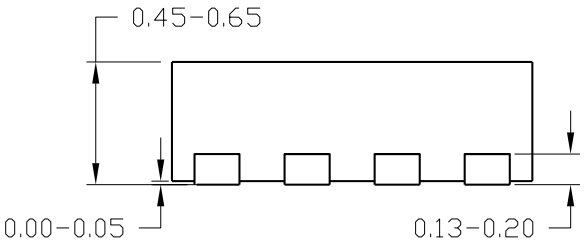


Figure5. PCB Layout Suggestion

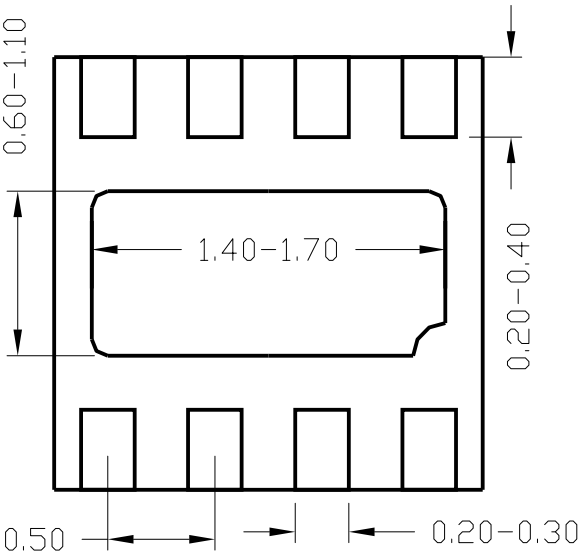
DFN2×2-8 Package Outline



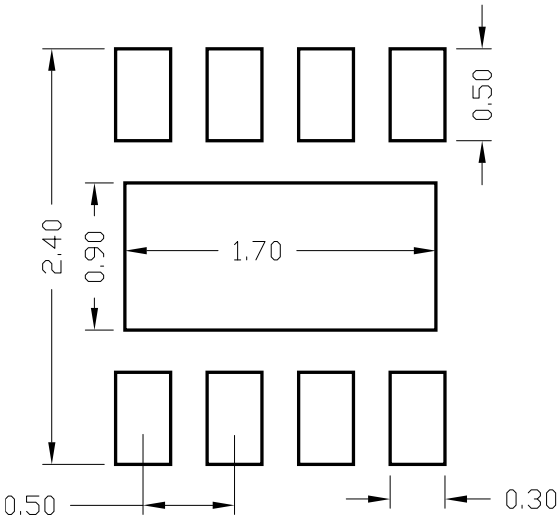
Top View



Side View



Bottom View

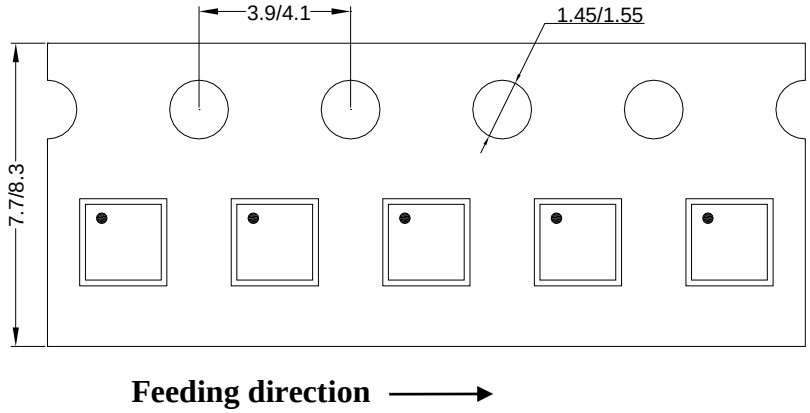


PCB Layout
(Reference Only)

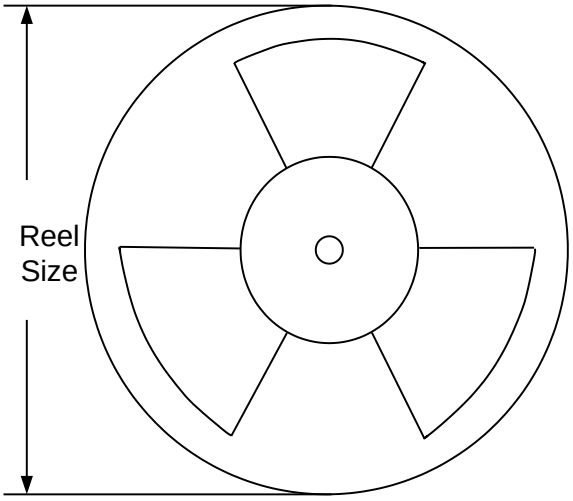
Notes: **All dimension in millimeters.**
All dimensions don't include mold flash & metal burr.

Taping & Reel Specification

1. DFN2×2



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2×2	8	4	7"	400	160	3000

3. Others: NA

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