SY20783

High Efficiency, 2-4 cells Buck Li-Ion Battery Charger

General Description

SY20783 is a wide input, high integrated and high efficiency Buck mode battery charger. It accepts 4-28V input and supports 2-4 cells Li-ion and Li-polymer battery. The charge current up to 2A can be programmed by using the external resistor for different portable applications. It also has a programmable charge timer and adaptive input power limit for safety battery charge operation. It consists of 30V rating reverse blocking FET and power switching FETs with low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

SY20783 along with small QFN3x3-18 footprint provides small PCB area application.

Ordering Information

SY20783 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20783QIC	QFN3×3-18	

Features

- Wide Input Voltage Range: 4V to 28V
- Constant Voltage Selectable: 4.1V/4.2V/4.35V per Cell
- Charge Current up to 2A for 2 Cells Battery
- Charge Current up to 1.6A for 3 Cells Battery
- Charge Current up to 1.5A for 4 Cells Battery
- Programmable VDPM
- Programmable Input Current Limit
- Programmable Charge Timer
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Thermal Regulation
- Input Voltage UVLO and OVP Protection
- BAT OVP and Short Protection
- Over Temperature Protection
- Charge Status Indication
- NTC JEITA Compliance
- Package QFN3x3-18

Applications

- Floor Cleaning Robot
- Window & Door Automation
- Smart Speaker
- Electrical Tools

Application Circuit

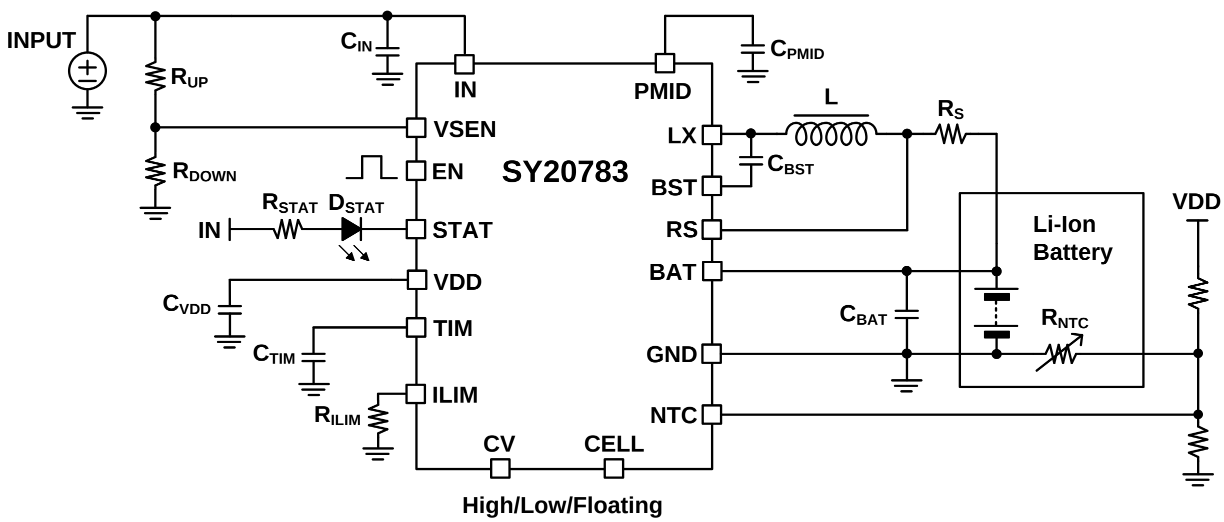
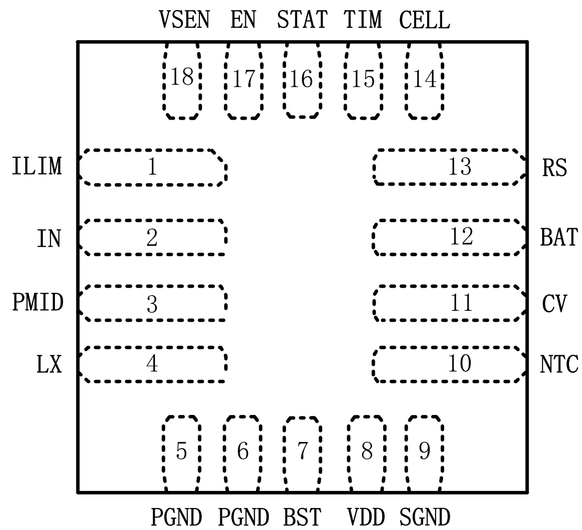


Figure1. Schematic Diagram

Pinout (top view)



(QFN3x3-18)

Top Mark: **CNW*xyz***, **(**Device code: CNW, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin No	Description
ILIM	1	Input current limit program pin. Connect a resistor from this pin to ground to program input current limit. The mirror current about 1/2700 of the blocking FET current will dump into the external resistor through ILIM pin and compared to the internal reference 1V. So I_{INLIM} = (1V/R_{ILIM}) ×2700. The maximum setting value of input current limit is 1.2A.
IN	2	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area. Suggest 1uF at least on this pin to ground.
PMID	3	Connected to the drains of the reverse blocking NFET and HSFET. Suggest 10uF at least on this pin to ground.
LX	4	Switch node pin. Connect to external inductor.
PGND	5,6	Power ground pin.
BST	7	Boot strap for high HSFET driver.
VDD	8	Internal LDO output. Connect this pin with 1uF capacitor to ground.
SGND	9	Signal ground pin.
NTC	10	Thermal protection pin. It will meet JEITA spec and refer to description section.
CV	11	Battery CV voltage selection pin. Pull low for 4.2V/cell, pull high for 4.35V/cell and float for 4.1V/cell.
BAT	12	Battery positive pin.
RS	13	Charge current sense resistor positive pin.
CELL	14	Battery cell selection pin. Different cell numbers can be selected by this pin. Float for 2 cells, pull low for 3 cells, and pull high for 4 cells.
TIM	15	Charge time limit pin. Connect this pin with a capacitor to ground. Internal current source charges and discharges the capacitor for TC mode and fast charge (CV&CC) mode's charge time limit. TC charge time limit is about 1/9 of fast charge time limit.
STAT	16	Charge status indication pin. It is open drain output and pulled up to IN thru a LED to indicate charge status. When the charge is done, LED is off. When any fault happens during charging, LED will flash with 1.8Hz frequency.
EN	17	IC enable pin. Pull high to enable the IC and low to shut down the IC. Floating this pin will also shut down the IC.
VSEN	18	Input voltage sense pin. If the voltage of this pin drops to internal 1.2V reference voltage, the input voltage will be clamped to the setting value.

Block Diagram

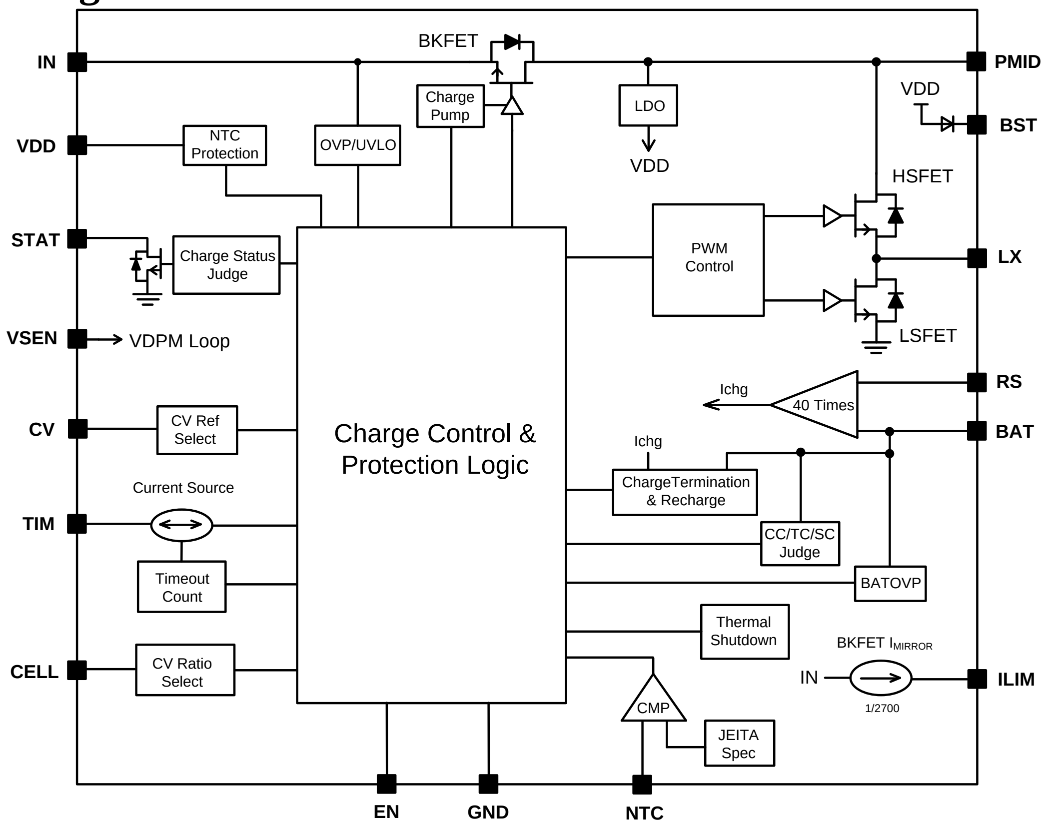


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, PMID, LX, RS, BAT, VSEN, STAT, CV, CELL, EN ---------- -0.3V to 33V
TIM, VDD, NTC, ILIM ---------- -0.3V to 4V
RS-BAT ---------- -0.3V to +0.3V
BST-LX ---------- -0.3V to 4V
LX Pin Current Continuous ---------- 2A
Power Dissipation, P_D @ T_A = 25°C, QFN3x3-18 ---------- 1.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 75°C/W
θ_{JC} ---------- 20°C/W
Junction Temperature Range ---------- -40°C to +125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ---------- 4V to 28V
PMID, LX, RS, BAT, VSEN, STAT, CV, CELL, EN ---------- 0V to 28V
TIM, ILIM, NTC ---------- 0V to 3.3V
RS-BAT ---------- -0.25V to +0.25V
Junction Temperature Range ---------- -40°C to 100°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

T_A=25°C, V_{IN}=20V, GND=0V, C_{IN}=1uF, C_{PMID}=10uF, L=4.7uH, R_S=25mΩ, C_{TIM}=330nF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{IN})						
Supply Voltage Operation Range	V_{IN}		4		28	V
Input Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising and measured from IN to PGND	3.5		3.9	V
Input Voltage Lockout Hysteresis	ΔV_{UVLO}	Measured from IN to PGND		0.2		V
Input Over Voltage Protection	V_{IN_OVP}	V_{IN} rising and measured from IN to PGND	28	29	30	V
Input Over Voltage Protection Hysteresis	ΔV_{IN_OVP}	Measured from IN to PGND		0.5		V
Quiescent Current						
Battery Discharge Current	I_{BAT}	Input absent, EN=0，V_{BAT}=17.4V		10	20	uA
Input Quiescent Current	I_{IN}	V_{IN}=28V, EN=1, No switching		0.8	1.1	mA
Input Shutdown Current	I_{SD}	V_{IN}=28V, EN=0		70	90	uA
Oscillator and PWM						
Switching Frequency	f_{SW}		400	500	600	kHz
Main N-FET Minimum On Time	t_{ON_MIN}			100		ns
Main N-FET Minimum Off Time	t_{OFF_MIN}			100		ns
Power MOSFET						
$R_{DS(ON)}$ of Main N-FET	R_{HSFET}			120		mΩ
$R_{DS(ON)}$ of Rectified N-FET	R_{LSFET}			180		mΩ
$R_{DS(ON)}$ of Blocking N-FET	R_{BKFET}			170		mΩ
Voltage Regulation						
Battery Charge Voltage	V_{BAT_REG}	2-cell, CV is floating	8.159	8.2	8.241	V
		2-cell, V_{CV}<0.5V	8.358	8.4	8.442	
		2-cell, V_{CV}>3V	8.657	8.7	8.743	
		3-cell, CV is floating	12.239	12.3	12.361	
		3-cell, V_{CV}<0.5 V	12.537	12.6	12.663	
		3-cell, V_{CV}>3V	12.985	13.05	13.115	
		4-cell, CV is floating	16.318	16.4	16.482	
		4-cell, V_{CV}<0.5V	16.716	16.8	16.884	
		4-cell, V_{CV}>3V	17.313	17.4	17.487	
Recharge Threshold refer to V_{BAT_REG}	ΔV_{RCH}	2-cell battery	150	200	250	mV
		3-cell battery	250	300	350	
		4-cell battery	300	400	500	
Trickle Charge Rising Edge Threshold	V_{TRK}	2-cell battery	5.4	5.6	5.8	V
		3-cell battery	8.1	8.4	8.7	
		4-cell battery	10.8	11.2	11.6	
Charge Current						
Charge Current Accuracy for Constant Current Mode	I_{CC}	I_{CC}=30mV/R_S	-3%		5%	
	I_{CC_COOL}	I_{CC_COOL}=15mV/R_S	-6%		10%	
Charge Current Accuracy for Trickle Current Mode	I_{TC}	I_{TC}=3mV/R_S	-25%		25%	
Termination Current	I_{TERM}	I_{TERM}=3mV/R_S	-25%		25%	

Input Current Limit						
Input Current Limit Accuracy	I_{INLIM}	I_{INLIM}=1.2A	-5%		5%	
BAT Voltage OVP						
BAT OVP Threshold	V_{BAT_OVP}	V_{BAT} rising	102.4	104	105.6	% V_{BAT_REG}
BAT OVP Threshold Hysteresis	ΔV_{BAT_OVP}			2		% V_{BAT_REG}
VDPM Reference						
Reference for VDPM	V_{VSEN_DPM}		1.182	1.2	1.218	V
VDD Regulation						
VDD LDO Voltage	V_{VDD}	V_{IN}>4V, EN=1	3.15	3.3	3.45	V
VDD Current Capacity	I_{VDD}	V_{VDD}=3V	20			mA
VDD Short Current	I_{VDD_SC}	VDD short to ground			15	mA
Timer						
Trickle Current Charge Timeout	t_{TC}	C_{TIM}=330nF	0.425	0.5	0.575	hour
Fast Charge Current Charge Timeout	$t_{CC/CV}$		3.85	4.5	5.15	hour
Charge Mode Change Delay Time	t_{MC}			30		ms
Termination Delay Time	t_{TERM}			30		ms
Recharge Delay Time	t_{RCHG}			30		ms
Cycle-by-Cycle Peak Current Limit						
Power FET Current Limit	I_{PEAK}	V_{BAT}> V_{SHORT}		3		A
BAT Short Protection						
BAT Short Protection Threshold	V_{SHORT}	V_{BAT} falling	1.9	2.0	2.1	V
Auto Shutdown						
Auto Shutdown Voltage Threshold	V_{ASD}	V_{IN} falling, measured from IN to BAT	140	180	220	mV
Auto Shutdown Voltage Threshold Hysteresis	V_{ASD_HYS}	V_{IN} rising hysteresis, measured from IN to BAT		80		
Logic Control						
High Level Logic for EN	V_{EN_H}		1.5			V
Low Level Logic for EN	V_{EN_L}				0.4	V
High Level Logic for CV,CELL	V_{LOGIC_H}		3			V
Low Level Logic for CV,CELL	V_{LOGIC_L}				0.5	V
NTC Thermal Protection JEITA Spec						
T1(0 ºC) Threshold	V_{NTC_T1}	V_{NTC} rising	72.75	73.25	73.75	%V_{VDD}
T1(0 ºC) Threshold Hysteresis	$V_{NTC\_T1\_HYS}$			1.25		
T2(10 ºC) Threshold	V_{NTC_T2}	V_{NTC} rising	67.25	68.25	69.25	
T2(10 ºC) Threshold Hysteresis	$V_{NTC\_T2\_HYS}$			1.25		
T3(45 ºC) Threshold	V_{NTC_T3}	V_{NTC} falling	43.75	44.75	45.75	
T3(45 ºC) Threshold Hysteresis	$V_{NTC\_T3\_HYS}$			1.2		
T5(60 ºC) Threshold	V_{NTC_T5}	V_{NTC} falling	33.875	34.375	34.875	
T5(60 ºC) Threshold Hysteresis	$V_{NTC\_T5\_HYS}$			1.2		
Thermal Regulation and Thermal Shutdown						
Junction Thermal Regulation Accuracy	T_{J_REG}		120	130	140	ºC
Thermal Shutdown Threshold	T_{SD}			150		ºC
Thermal Shutdown Threshold Hysteresis	T_{SD_HYS}	Falling edge		20		ºC

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

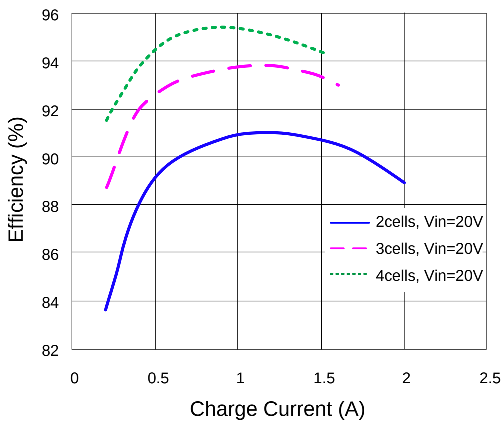
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

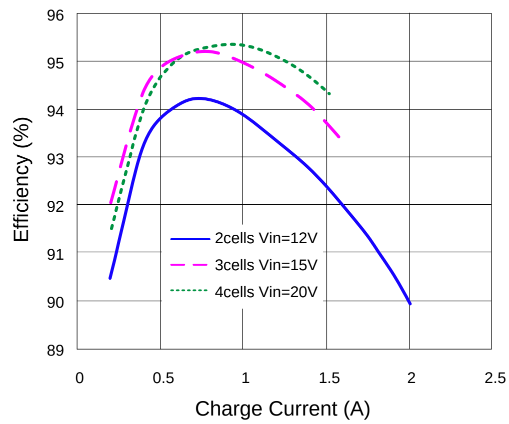
Typical Performance Characteristics

(T_A=25°C, V_{IN}=20V, C_{IN}=1uF, C_{PMID}=10uF, L=4.7uH, R_S=25mΩ, unless otherwise specified)

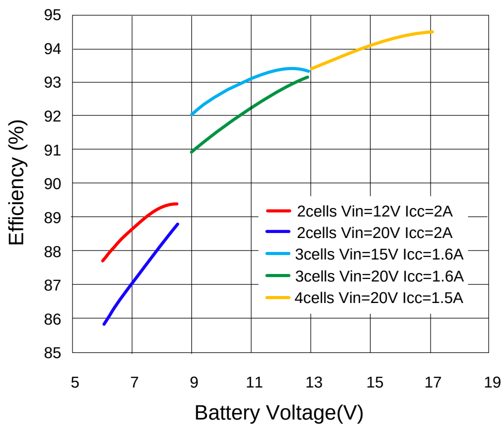
Efficiency vs. Charge Current (CV Mode)



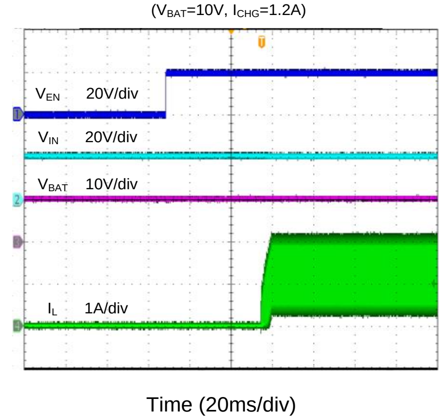
Efficiency vs. Charge Current (CV Mode)



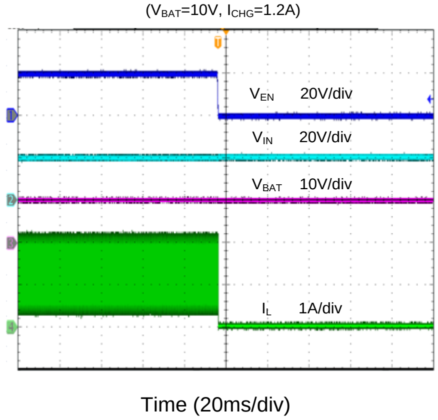
Efficiency vs. Battery Voltage (CC Mode)



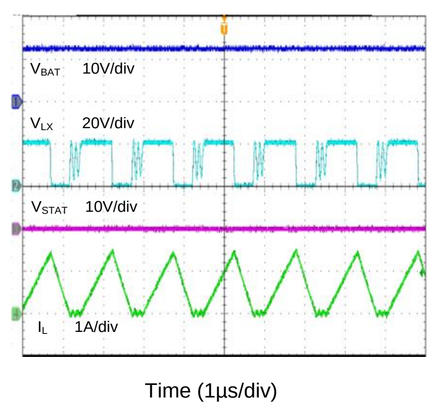
Startup from EN
(V_{BAT}=10V, I_{CHG}=1.2A)



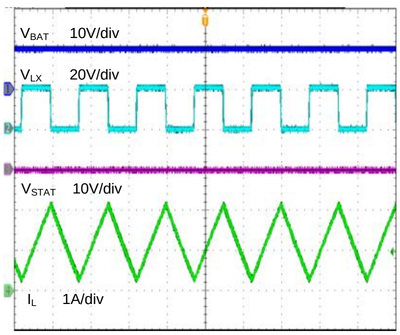
Shutdown from EN
(V_{BAT}=10V, I_{CHG}=1.2A)



Steady Waveform at CV Mode
(V_{BAT}=12.6V, I_{CHG}=0.6A)

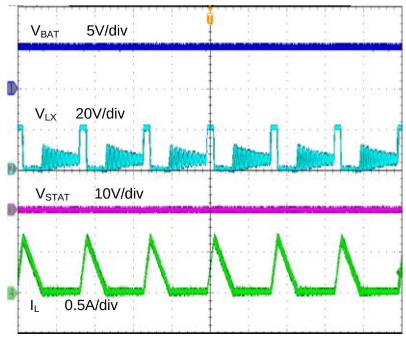


Steady Waveform at CC Mode
(V_{BAT}=10V, I_{CHG}=1.2A)



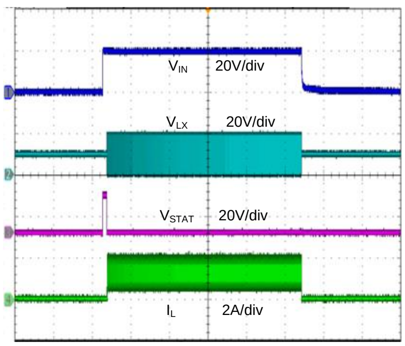
Time (1µs/div)

Steady Waveforms at TC Mode
(V_{BAT}=5V, I_{CHG}=0.12A)



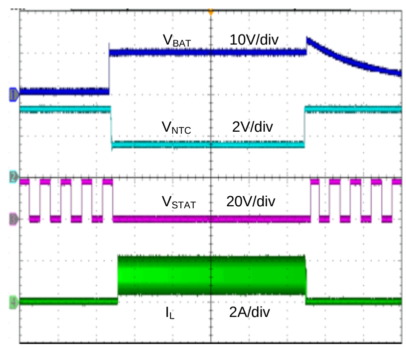
Time (1µs/div)

Insert and Remove Adapter
(CC Mode, V_{BAT}=10V)



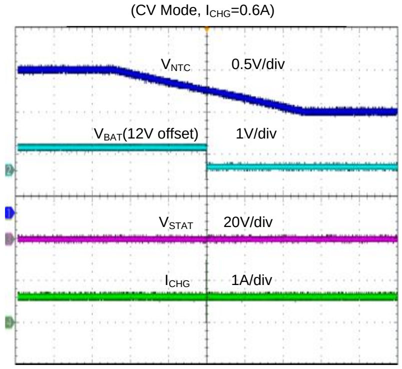
Time (400ms/div)

Insert and Remove Battery
(CC Mode, V_{BAT}=10V)



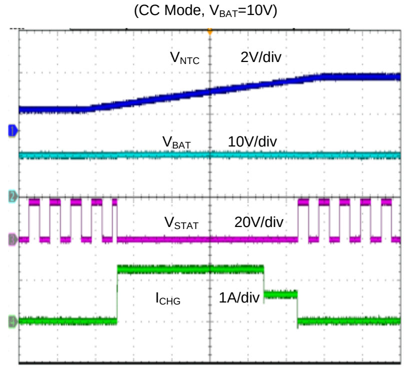
Time (1s/div)

NTC JEITA Function
(CV Mode, I_{CHG}=0.6A)



Time (1s/div)

NTC JEITA Function
(CC Mode, V_{BAT}=10V)



Time (1s/div)

General Function Description

SY20783 is a 4-28V input, 2-4 cells Li-Ion synchronous Buck charger. The charge current up to 2A can be programmed by using the external resistor for different portable applications. It also has a programmable charge timer and adaptive input power limit for safety battery charge operation. It consists of 30V rating reverse blocking FET and power switching FETs with low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

SY20783 along with small QFN3x3-18 footprint provides small PCB area application.

Switching Mode Control Strategy

SY20783 utilizes quasi-fixed frequency control to simplify the internal close-loop compensation design. The quasi-fixed frequency settled at 500 kHz is easy for the size minimization of peripheral circuit design.

Operation Principle

SY20783 works as a synchronous Buck mode battery charger when the adapter is present. It utilizes 500 kHz switching frequency to minimize the PCB design.

The charger will operate in battery short mode, trickle charge mode, constant current charge mode and constant voltage charge mode according to the battery voltage. The charge current in every mode is showed in following charge curve. In constant voltage mode, if charge current is lower than termination current, the charger will stop charging until battery voltage drops to recharge voltage.

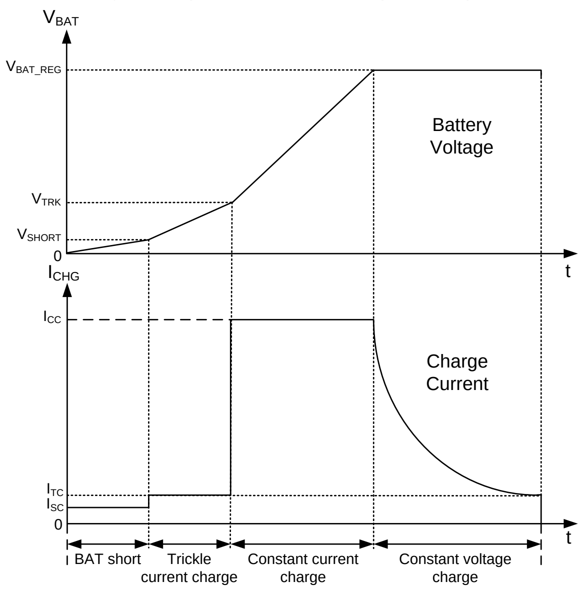


Figure3. Charge Curve

Input Power Limit Principle

For prevent input source overloading, SY20783 has IDPM and VDPM loop to limit the input power.

It will automatically decrease charge current when input current exceeds setting value or VSEN voltage drops to internal 1.2V reference.

Charge Status Indication Description

STAT is an open drain output pin and can indicate charge status. Connect a LED from IN to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flashing with 1.8Hz means Fault Mode.

1. Charge-In-Process – Pull and keep STAT pin to Low;
2. Charge Done – Pull and keep STAT pin to High;
3. Fault Mode – Output high and low voltage alternatively with 1.8Hz frequency. The faults include input OVP, BAT OVP, BAT short, NTC JEITA UTP/OTP (below T_1 or above T_5), Time-out and Thermal shutdown.

Full Charger Protections Description

In charge mode, SY20783 has full protections to protect the IC and the battery.

Input Over Voltage Protection – SY20783 has IN over voltage protection. It will stop charging when input OVP occurs. IC will auto recover normal operation when this fault removes.

BAT Over Voltage Protection – SY20783 will stop charging when BAT OVP occurs. IC will auto recover normal operation when this fault removes.

Timeout Protection – The charger can detect a bad battery. It will stop charging and latch off when the charger works over safety time which is set by C_{TIM}. Only recycling the input or EN signal can release this fault.

JEITA NTC Thermal Protection – When NTC voltage is lower than V_{NTC_T5} threshold or higher than V_{NTC_T1} threshold, the charger will stop charging. IC will auto recover when this fault removes.

Thermal Shutdown Protection – The IC will stop operation when the junction temperature is higher than 150°C. It will auto recover normal when this fault removes.

Charge JEITA Guideline Compliance

To improve the safety of charging Li-ion batteries, JEITA recommends the voltage on NTC pin must be within the V_{NTC_T1} to V_{NTC_T5} thresholds. If NTC voltage exceeds the V_{NTC_T1}–V_{NTC_T5} range, the charger suspends charging and waits until the battery temperature is within the T_1 to T_5 range. At cool temperature (T_1–T_2), JEITA recommends the charge current reduces to at least half of the constant charge current or lower. At warm temperature (T_3–T_5), JEITA recommends charge voltage is lower than 4.1V (for 4.2V CV voltage).

SY20783 can meet the JEITA requirement. The voltage setting at warm temperature (T_3–T_5) can be 150mV*cells lower than V_{BAT_REG}. The current setting at cool temperature (T_1–T_2) can be reduced to 50% of constant charge current I_{CC}.

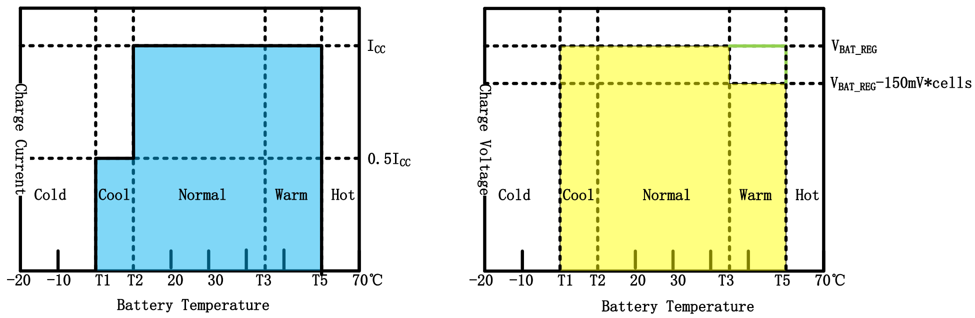


Figure4. JEITA Guideline

Power Path Management Function

SY20783 can also support power path management for system application and an extra PFET is needed. When adapter is present, adapter will supply system load and battery charge power simultaneously if input power limit is trigged. When adapter is absent, the battery will discharge to supply system load by the external PFET.

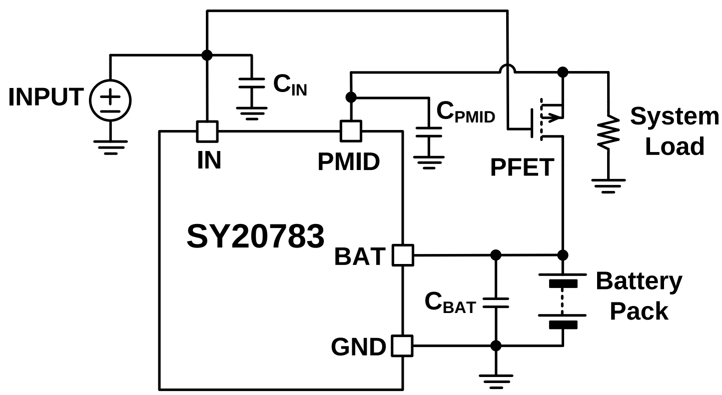


Figure5. Power Path Schematic Diagram

Application Information

Because of the high integration of SY20783, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{PMID}, output capacitor C_{BAT}, inductor L, NTC resistors R_1, R_2, charge current sense resistor R_S and timer capacitor C_{TIM} need to be selected for the targeted application specification.

NTC Resistor

SY20783 monitors battery temperature by measuring the VDD voltage and NTC voltage. It will trigger JEITA protection when the ratio K ($K= V_{NTC}/V_{VDD}$) reaches the related threshold.

The temperature sensing network is showed as below.

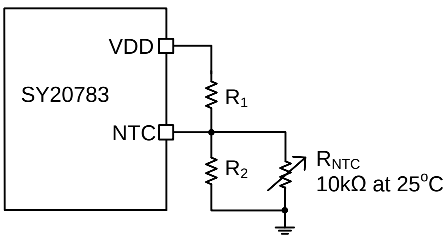


Figure6. NTC Resistors Network

For JEITA standard, T_1=0ºC, T_2=10ºC, T_3=45ºC, T_5=60ºC.

NTC resistors should be chosen at R_1=5.24kΩ, R_2=30.28kΩ.

Input Voltage Threshold for Input Power Limit

SY20783 will monitor input voltage by measuring the VSEN voltage. When VSEN voltage drops below the internal 1.2V reference, SY20783 will decrease the duty cycle to reduce the charge current.

The input voltage sense network is shown below, choose R_{UP}, R_{DOWN} to set the input voltage threshold V_{INT}:

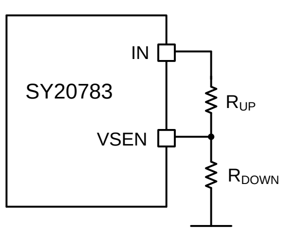


Figure7. Input Voltage Sense Network

$$V_{INT} = \frac{V_{VSEN\_DPM} \times (R_{DOWN} + R_{UP})}{R_{DOWN}} \quad \text{Unit: V}$$

V_{VSEN_DPM} is 1.2V.

If VDPM function is not used, remove R_{DOWN} and pull up VSEN pin to IN by R_{UP}.

Input Current Threshold for Input Power Limit

SY20783 will monitor input current by sensing internal BKFET current. When actual input current exceeds the setting value at ILIM pin, SY20783 will decrease the duty cycle to reduce the charge current. The input current limit value is programmed by below equation:

$I_{INLIM} = (1V/R_{ILIM}) \times 2700$

Note that the maximum I_{INLIM} setting value is 1.2A.

In those applications where charge current is expected to maximum value or system load is necessary, IDPM is maybe not suitable and VDPM is recommended for input power limit.

If IDPM function is not used, connect ILIM pin to GND with 1k resistor.

Charge Current Sense Resistor Rs

The charge current sense resistor R_S is calculated as below:

$$R_S = \frac{30mV}{I_{CC}}, \quad \text{Unit: m}\Omega$$

where the I_{CC} is the battery constant charge current, unit is ampere.

Timer Capacitor C_{TIM}

The charger also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is given by the formula:

$C_{TIM}=2\times10^{-11}S\times t_{CC/CV}$ Unit: F

$t_{CC/CV}$ is the permitted fast charge time, unit is second.

Input Capacitor C_{PMID}

The main input capacitor is connected between PMID pin to PGND. It can absorb input ripple current from the Buck stage, which is given by below equation.

$$I_{RMS}=I_{CHG}\times\frac{\sqrt{V_{BAT}\times(V_{IN}-V_{BAT})}}{V_{IN}}$$

The maximum value of this RMS ripple current in the application must be smaller than the rated RMS current in the chosen capacitor datasheet. Care should be taken to minimize the loop area formed by C_{PMID}, and PMID and PGND pins.

To minimize the potential noise problem, IN should be decoupled to PGND with typical 1μF capacitance, X7R or a better grade ceramic capacitor.

Output Capacitor C_{BAT}

The output capacitor in parallel with the battery is used for absorbing the high frequency switching ripple current and smoothing the output voltage. The RMS value of the output ripple current I_{RMS} is calculated as follow.

$$I_{RMS}=\frac{V_{IN}\times D\times(1-D)}{\sqrt{12}\times L\times f_{SW}}$$

where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for CCM mode which is typical operation for the battery charger. During the battery charge period, battery voltage varies from its initial battery voltage to the rated voltage. The maximum value of this RMS ripple current in the application must be smaller than the rated RMS current in the chosen capacitor datasheet. A typical 20μF ceramic capacitor is recommended to absorb this current and also has small size.

Output Inductor L

There are several considerations in choosing the inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 20%-40% of the maximum charge current I_{CC}. The inductance is calculated as:

$$L=\frac{V_{BAT\_REG}(1-V_{BAT\_REG}/V_{IN})}{f_{SW}\times I_{CC}\times(20\%\sim40\%)}$$

where f_{SW} is the switching frequency and V_{IN} is the input voltage in the application

SY20783 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the maximum peak inductor current under all the range of battery voltage and full load conditions.

$$I_{SAT}\geq I_{CC}+\frac{V_{BAT\_REG}(1-V_{BAT\_REG}/V_{IN})}{2\times f_{SW}\times L}$$

The maximum peak inductor current happens when battery voltage is equivalent with half of input voltage.

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<20mohm to achieve a good overall efficiency.

A 4.7uH inductor is usually recommended to cover most of the conventional applications.

Layout Design

The layout design of SY20783 is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, C_{PMID}, L, C_{VDD} and C_{BST}.

1) It is desirable to maximize the PCB copper area connecting to PGND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{PMID} must be close to pins PMID and PGND. The loop area formed by C_{PMID} and PGND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The capacitor C_{TIM} and the trace connecting to the TIM pin must not be adjacent to the LX net on the PCB.

The SY20783 PCB layout is suggested as below.

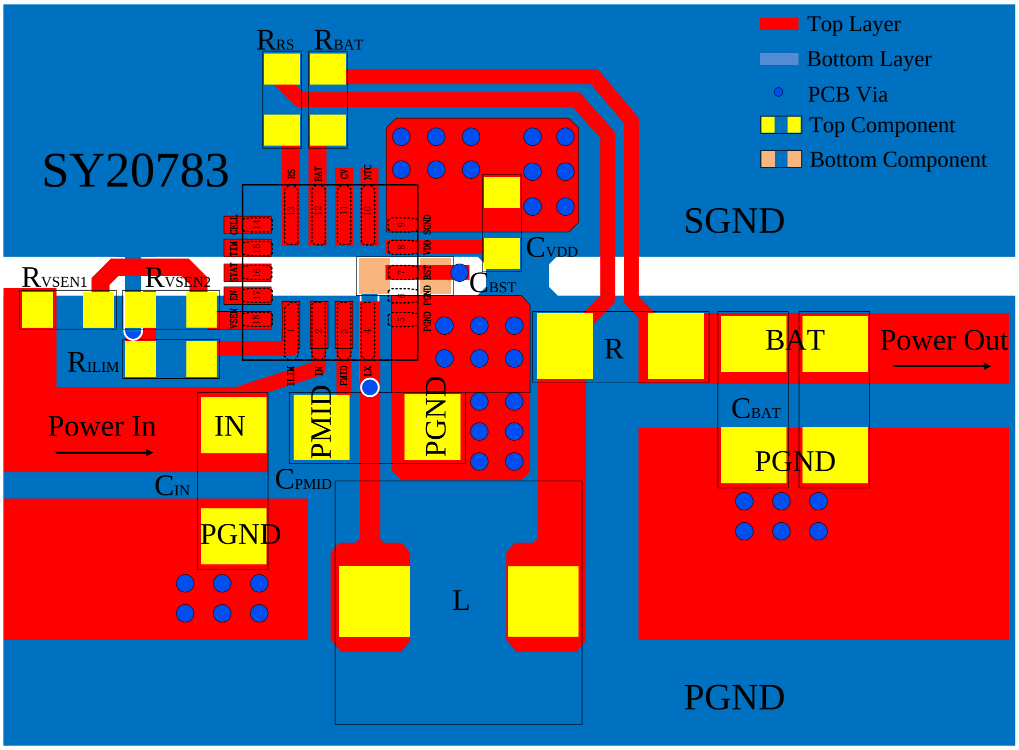
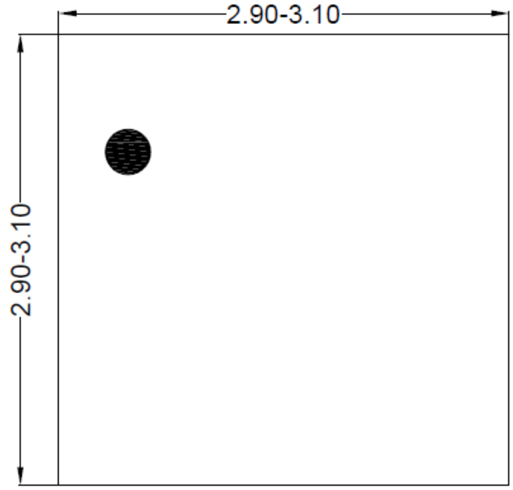
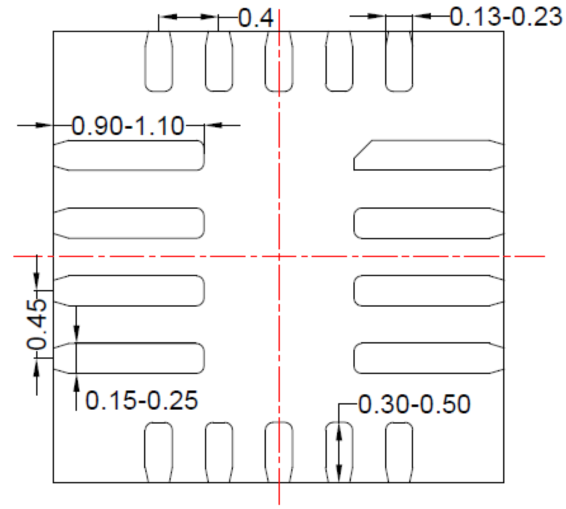


Figure8.Proposed PCB Layout

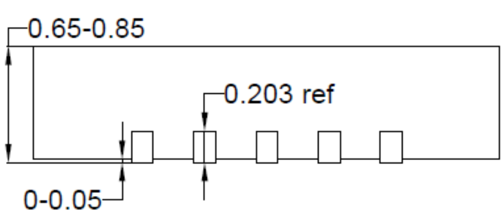
QFN3×3-18 Package Outline Drawing



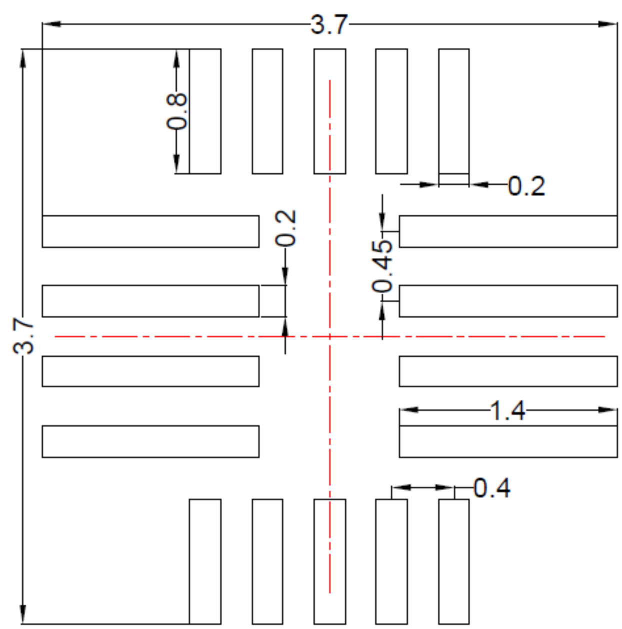
Top View



Bottom View



Front View

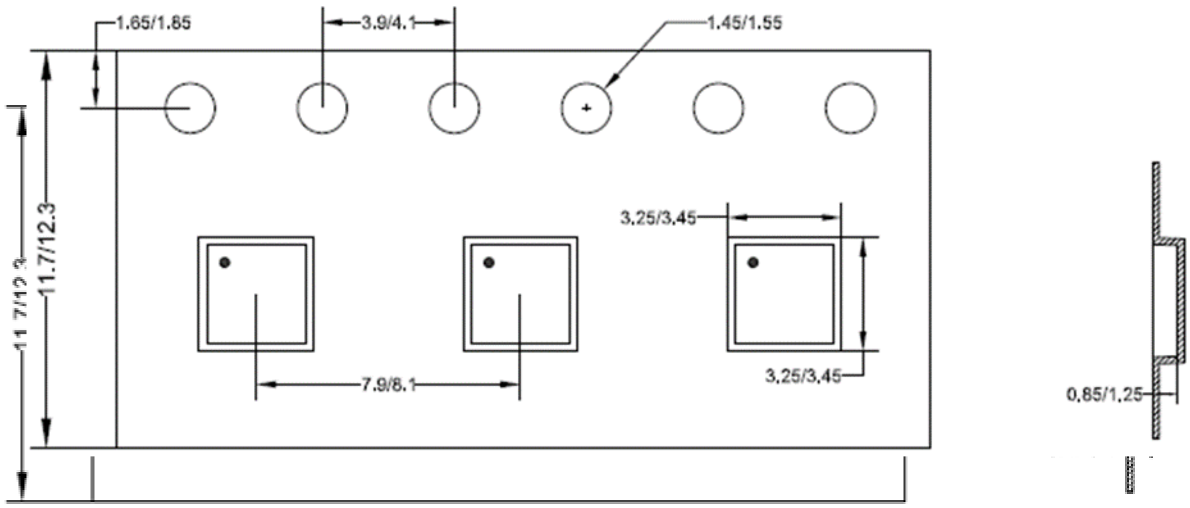


Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr

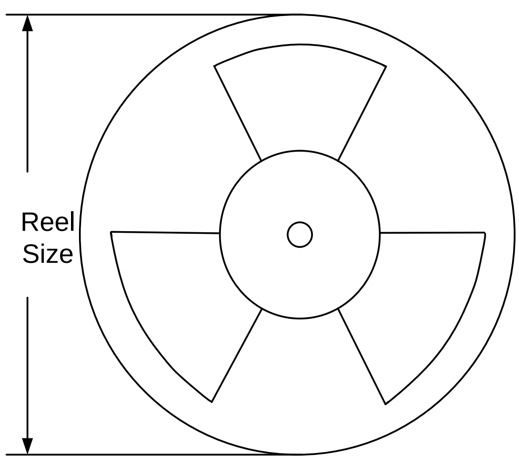
Taping & Reel Specification

1. QFN3×3 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA

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