General Description

The SY21114 develops high efficiency 500kHz synchronous step-down DC/DC converter capable of delivering 3A current. The device operates over a wide input voltage range from 4.2V to 18V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY21114 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500kHz to minimize the size of the inductor and the capacitor.

Ordering Information

SY21114 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21114ADC	TSOT23-6	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 80mΩ/40mΩ
- 4.2-18V Input Voltage Range
- 3A Output Current Capability
- 500kHz Switching Frequency Minimize the External Components
- Stable with 10μF C_{OUT} and 2.2μH Inductor
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Startup from Pre-biased Output
- Cycle-by-cycle Peak/Valley Current Limitation
- Hic-cup Mode Output Short Circuit Protection
- Over Temperature Protection with Auto Recovery
- Output Auto Discharge Function
- ±1.0% Internal Reference Voltage
- RoHS Compliant and Halogen Free
- Compact Package: TSOT23-6

Typical Application

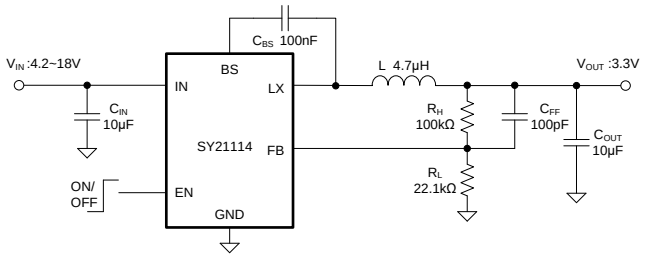


Figure1. Schematic Diagram

Inductor and C_{OUT} Selection Table

V_{OUT} [V]	L [μH]	C_{OUT} [μF]		
		4.7	10	22
1.2	1.5			√
	2.2			☆
3.3	2.2		√	√
	4.7		☆	√
5	3.3		√	√
	6.8		☆	√

Note: '☆ ' means recommended for most applications.

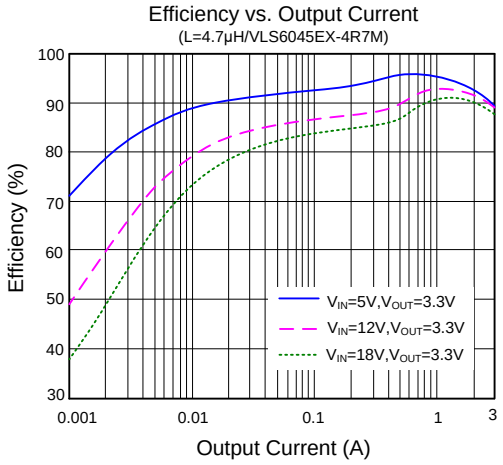
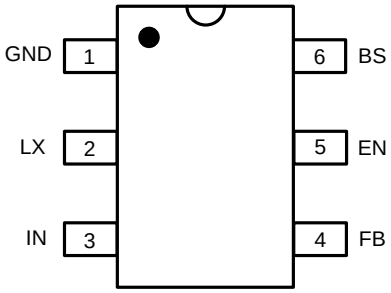


Figure2. Efficiency vs. Output Current

Pin-out (Top View)



(TSOT23-6)

Top Mark: L8*xyz* (device code: L8; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
GND	1	Power ground pin.
LX	2	Inductor pin. Connect this pin to the switching node of the inductor.
IN	3	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
FB	4	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$
EN	5	Enable control. Pull high to turn on. Do not leave this pin floating.
BS	6	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.

Block Diagram

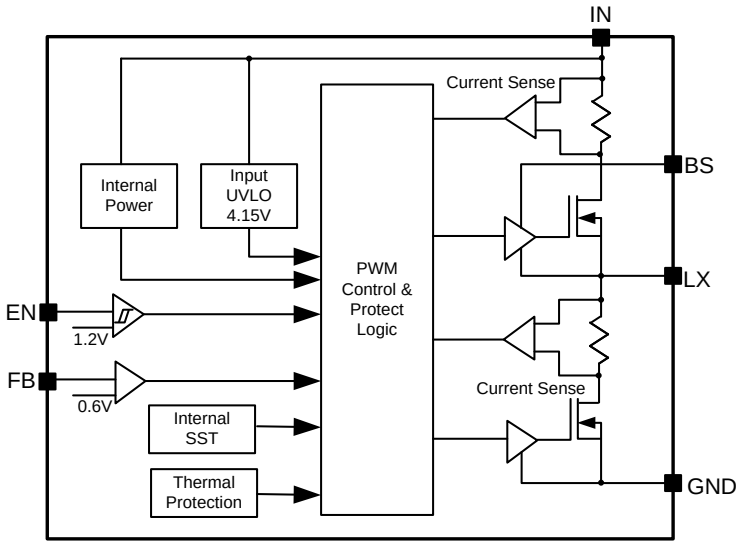


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 19V
LX, EN Voltage---------- -0.3V to V_{IN} + 0.3V
FB Voltage---------- -0.3V to 3.3V
BS-LX Voltage---------- -0.3V to 4V
Power Dissipation, P_D @ T_A = 25°C TSOT23-6, ---------- 1.5W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 66°C/W
θ_{JC} ---------- 15°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX Voltage in 10ns Duration (Note3) ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.2V to 18V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7μH, C_{OUT} = 10μF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.2		18	V
Input UVLO Threshold	V_{UVLO}				4.15	V
UVLO Hysteresis	V_{HYS}			0.6		V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		250		μA
Shutdown Current	I_{SHDN}	EN=0		5	10	μA
Feedback Reference Voltage	V_{REF}	Under CCM condition	594	600	606	mV
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Output Discharge Resistance	R_{DIS}			40		Ω
Top FET RON	$R_{DS(ON)1}$			80		mΩ
Bottom FET RON	$R_{DS(ON)2}$			40		mΩ
EN Rising Threshold	$V_{EN,R}$		1.08	1.2	1.32	V
EN Falling Threshold	$V_{EN,F}$		0.9	1.0	1.1	V
EN Leakage Current	I_{EN}		-1		1	μA
Min ON Time	$t_{ON,MIN}$			50		ns
Min OFF Time	$t_{OFF,MIN}$			200		ns
Turn On Delay	$t_{ON,DLY}$	from EN high to LX start switching		300		μs
Soft-start Time	t_{SS}	V_{OUT} from 0 to 100%		1		ms
Switching Frequency	f_{SW}	V_{OUT}=3.3V, CCM		500		kHz
Top FET Peak Current Limit	$I_{LIM,TOP}$		4.5			A
Bottom FET Valley Current Limit	$I_{LIM,BOT}$		3			A
Output UVP Threshold	V_{UVP}			33		%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$			100		μs
UVP Hiccup On Time	$t_{UVP,ON}$			2		ms
UVP Hiccup Off Time	$t_{UVP,OFF}$			6		ms
Thermal Shutdown Temperature	T_{SD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYS}			15		˚C

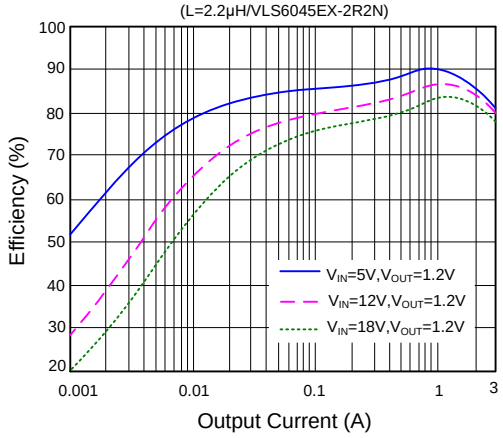
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2-oz two-layer Silergy evaluation board. Paddle of TSOT23-6 package is the case position for SY21114ADC θ_{JC} measurement.

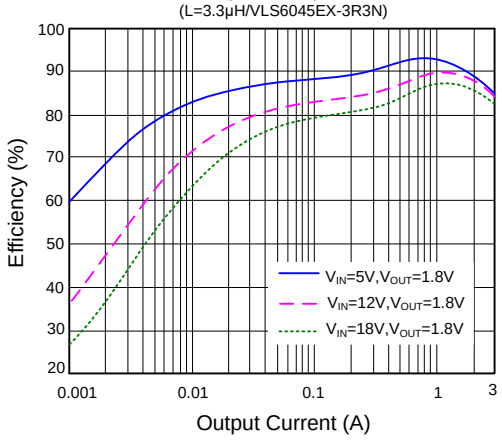
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

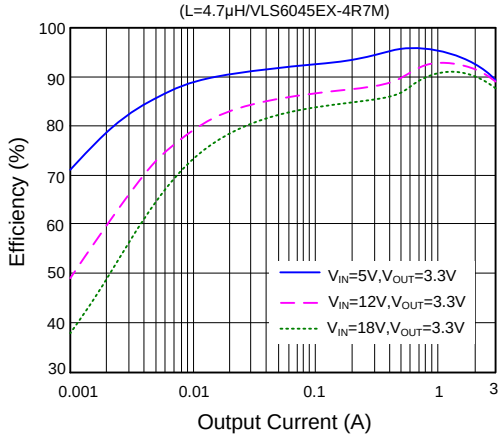
Efficiency vs. Output Current
(L=2.2μH/VLS6045EX-2R2N)



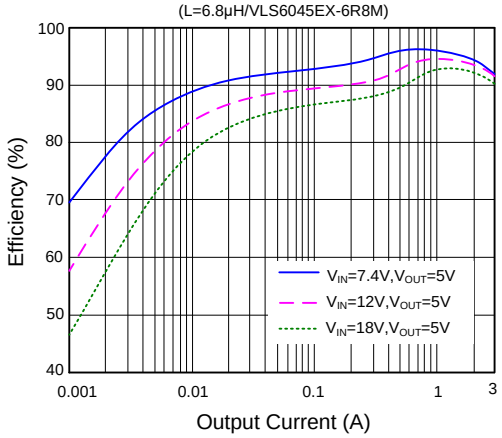
Efficiency vs. Output Current
(L=3.3μH/VLS6045EX-3R3N)



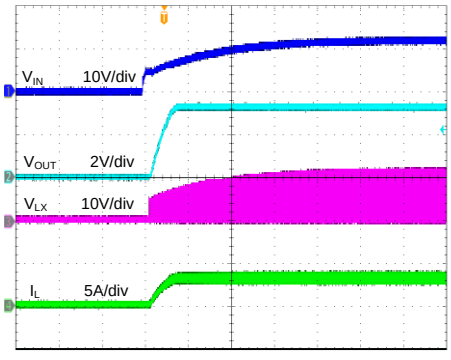
Efficiency vs. Output Current
(L=4.7μH/VLS6045EX-4R7M)



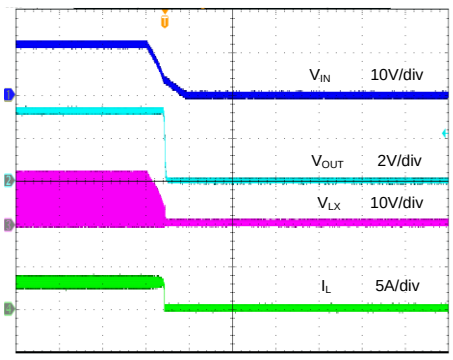
Efficiency vs. Output Current
(L=6.8μH/VLS6045EX-6R8M)



Startup from V_{IN}
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)

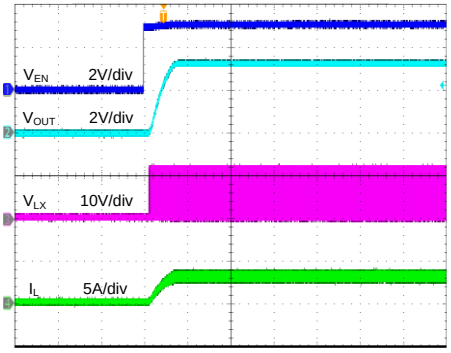


Shutdown from V_{IN}
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Startup from EN

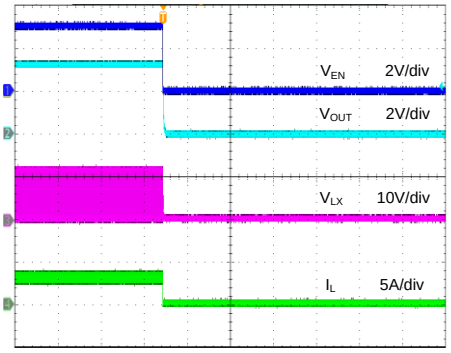
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Time (2ms/div)

Startup from EN

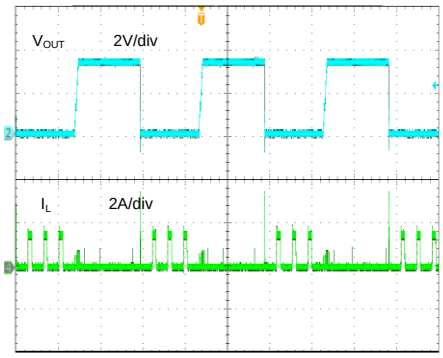
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Time (2ms/div)

Short Circuit Protection

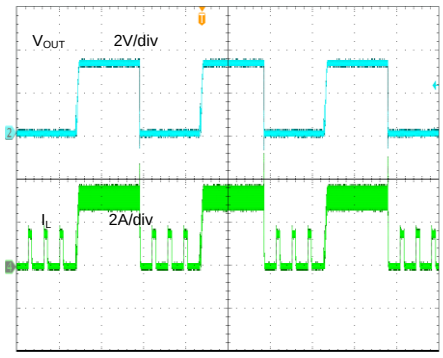
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A~Short)



Time (20ms/div)

Short Circuit Protection

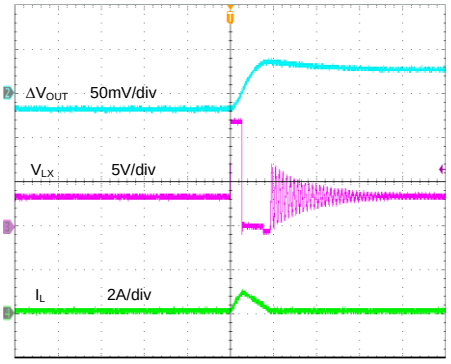
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A~Short)



Time (20ms/div)

Output Ripple

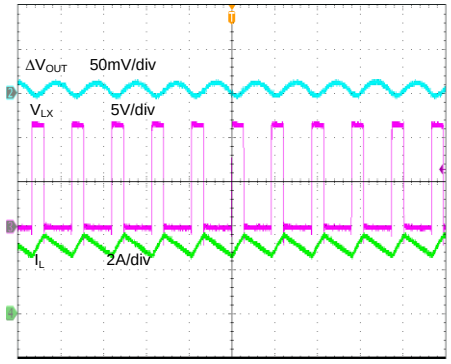
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A)



Time (2μs/div)

Output Ripple

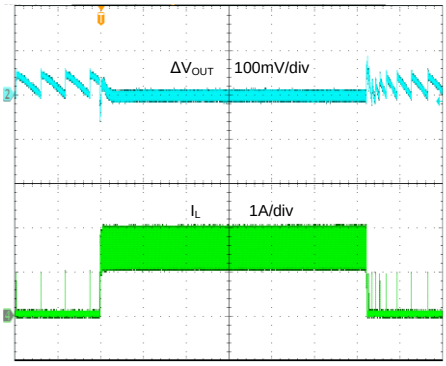
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Time (2μs/div)

Load Transient

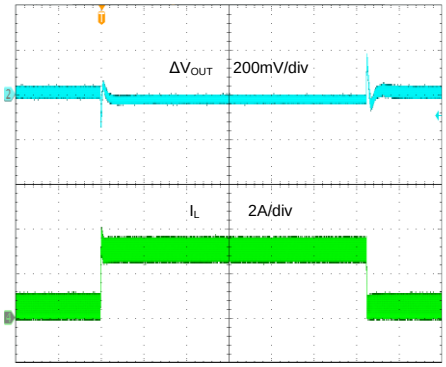
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0~1.5A)



Time (400μs/div)

Load Transient

(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0.3~3A)



Time (400μs/div)

Operation

The SY21114 is a high efficiency 500kHz synchronous step-down DC/DC regulator capable of delivering up to 3A load current. It can operate over a wide input voltage range from 4.2V to 18V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The SY21114 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads.

The SY21114 provides protection functions such as cycle-by-cycle current limiting and thermal shutdown protection. The SY21114 will sense the output voltage conditions for the fault protection.

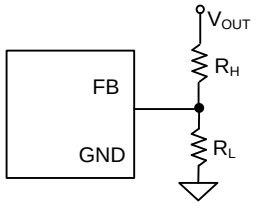
Applications Information

Because of the high integration in the SY21114 IC, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_H and R_L) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_H and R_L:

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_H=100kΩ is chosen, then using the following equation, R_L can be calculated to be 22.1kΩ:

$$R_L = \frac{0.6V}{V_{OUT} - 0.6V} \times R_H$$



Input Capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} and IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with 16V rating and more than 22μF capacitance.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21114 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

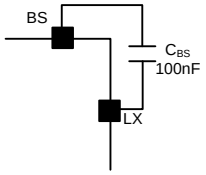
Soft-start

The SY21114 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC start-up. The typical soft-start time is 1ms.

External Bootstrap Capacitor

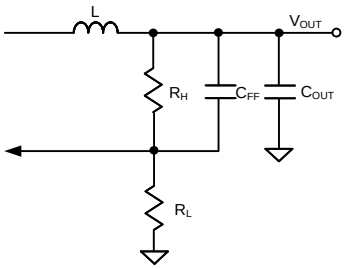
This capacitor provides the gate driver voltage for internal high side MOSFET. A 100nF low ESR

ceramic capacitor connected between the BS pin and the LX pin is recommended.



Load Transient Considerations:

The SY21114 integrates the compensation components to achieve good stability and fast transient responses. Adding a small ceramic cap in parallel with R_H may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

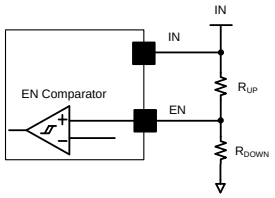


OCP and SCP Protection Method

If the high side power FET current gets higher than the peak current limit threshold, the high side power FET will turn off and the low side power FET will turn on. If the low side FET current gets higher than the valley current limit threshold, the low side FET will keep turning on until low side FET current decreases below the valley current limit threshold. So both peak and valley current are limited. If the load current continues to increase in these conditions, the output voltage will drop. When the output voltage falls below 33% of the regulation level, the output short will be detected and the IC will operate in hic-cup mode. The hic-cup on time will be 2ms and hic-cup off time will be 6ms. If the hard short is removed, the IC will return to normal operation.

Enable and Adjusting Under Voltage Lockout

The EN pin has accurate rising and falling threshold, it provides programmable ON/OFF control by connecting an external resistor divider. Once the EN pin voltage exceeds the rising threshold, the device will start operation. If the EN pin voltage is pulled below the falling threshold, the regulator will stop switching and enter the shutdown state.



It is not recommended to connect EN and IN directly. A resistor in a range of 1kΩ to 1MΩ should be adopted if EN is pulled high by IN.

Layout Design:

The layout design of SY21114 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_H and R_L and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

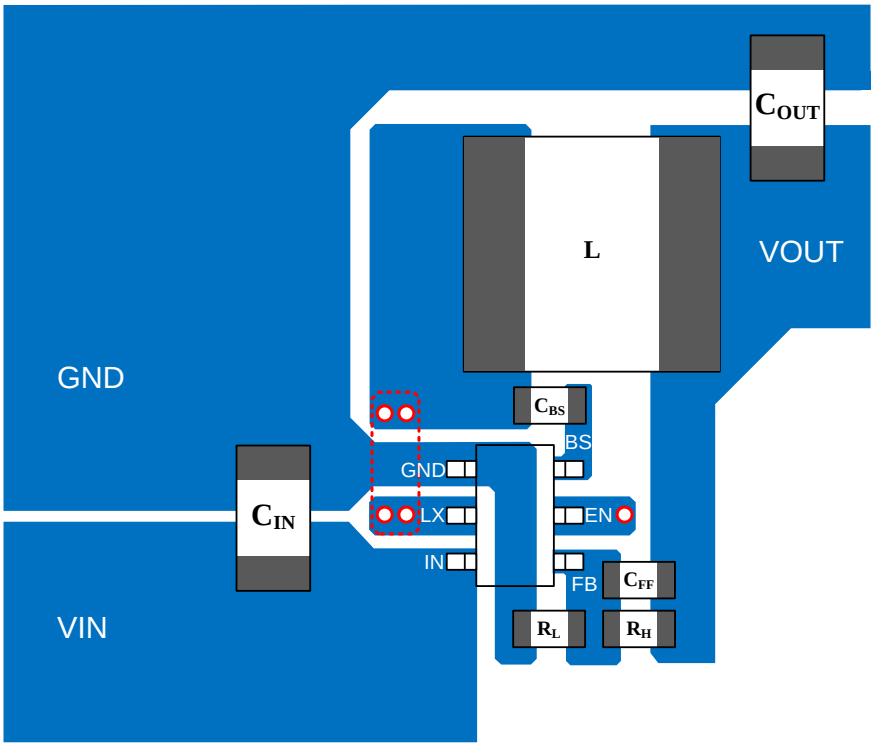
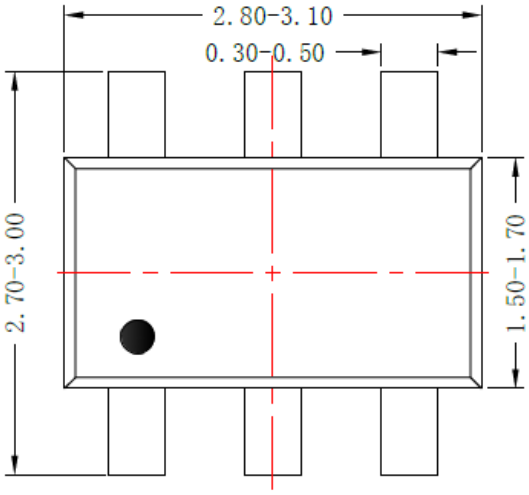
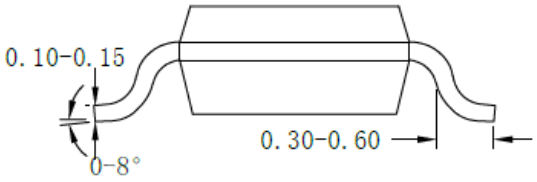


Figure 4. PCB Layout Suggestion

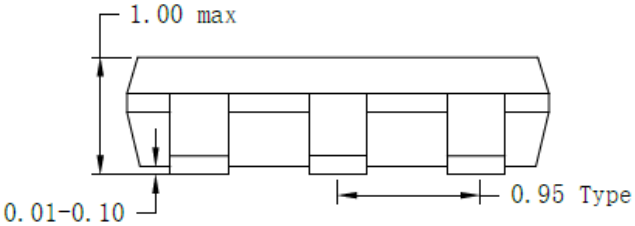
TSOT23-6 Package Outline & PCB Layout



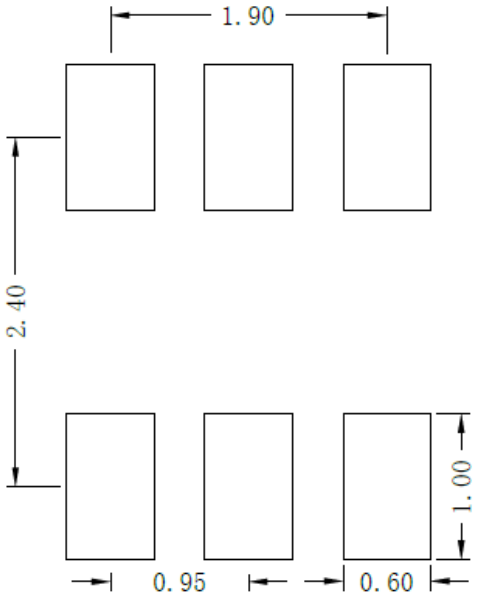
Top view



Side view



Front view



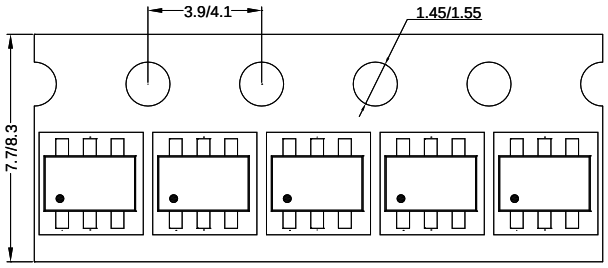
Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

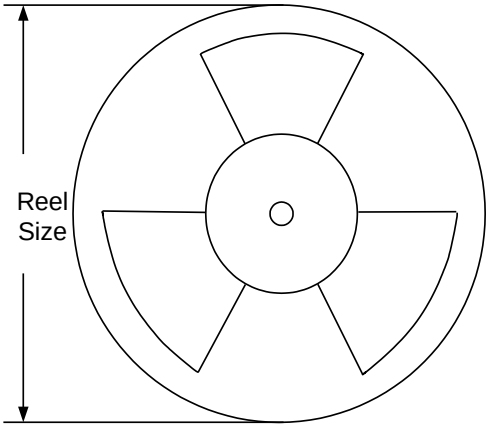
1. Taping orientation

TSOT23-6



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-6	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec.01, 2020	Revision 0.9A	Update the Package Outline Drawing (page 11)
Sep. 01, 2020	Revision 0.9	Initial Release

IMPORTANT NOTICE

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