

### General Description

The SY21243A high-efficiency synchronous step-down DC/DC regulator is capable of delivering 8A current over a wide input voltage range of 4V to 24V.

Silergy's constant on-time (COT) ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near-constant operating frequency over line, load, and output voltage ranges. This control method provides stable operation without complex compensation, even with low-ESR ceramic capacitors.

Internal 20mΩ power and 10mΩ synchronous rectifier switches provide excellent efficiency over a range of applications, especially for low output voltages and low duty cycles. The SY21243A also integrates a bypass switch that allows the IC to be powered by an external DC source. The SY21243A offers protection against multiple conditions, including cycle-by-cycle current limit, input undervoltage lockout, output undervoltage and overvoltage protection, internal soft-start, and thermal shutdown.

Only the input and output capacitors, inductor, and feedback resistors need to be selected for the targeted application.

The SY21243A is available in a compact QFN2.5x2.5-16 package.

### Features

- 4–24V Input Voltage Range
- Up to 8A Output Current
- Low  $R_{DS(ON)}$  for Internal Switches: 20 mΩ Top, 10mΩ Bottom
- Integrated 1.5Ω Bypass Switch
- COT Ripple-Based Control to Achieve Fast Transient Responses
- Soft-Start Inrush Current Limit
- Pseudoconstant Frequency: 600kHz
- Adjustable Output Voltage
- $\pm 1\%$  Internal Reference Voltage
- PFM/FCCM Selectable Light Load Operation Mode
- Power-Good Indicator
- Output-Discharge Function
- Cycle-by-Cycle Valley and Peak-Current Limit (OCP)
- Programmable Valley-Current Limit Threshold by  $I_{LMT}$  Pin
- Hiccup Mode Output Undervoltage (UVP)
- Automatic Recovery Mode Output Overvoltage (OVP) and Overtemperature (OTP)
- Input Undervoltage (UVLO)
- RoHS-Compliant and Halogen-Free
- Compact Package: QFN2.5mmx2.5mm-16

### Applications

- LCD TV/3DTV
- Set-Top Box
- Notebook
- High-Power AP

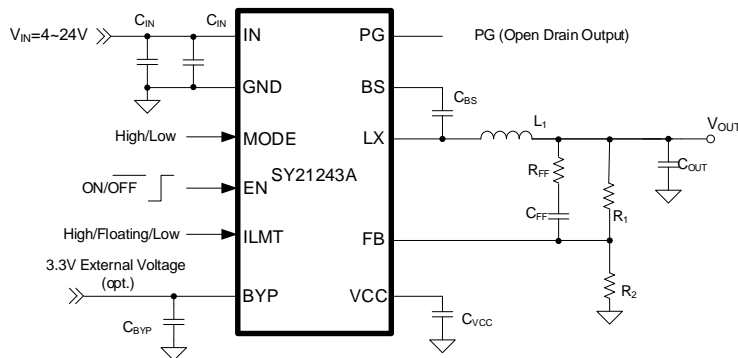


Figure 1. Typical Application Circuit

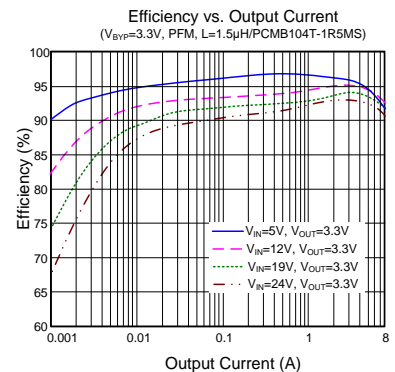


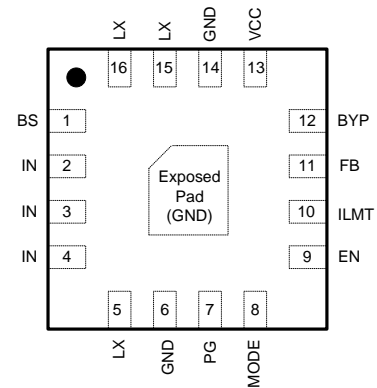
Figure 2. Efficiency vs. Output Current

## Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21243ARHC	QFN2.5x2.5-16 RoHS-Compliant and Halogen-Free	<b>B3xyz</b>

*x = year code, y = week code, z = lot number code*

## Pinout (top view)



## Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply for high-side gate driver. Connect a 0.1 $\mu$ F ceramic capacitor between the BS and the LX pin.
2, 3, 4	IN	Input pin. Decouple this pin to the GND pin with at least a 10 $\mu$ F ceramic capacitor. A 0.1 $\mu$ F input ceramic capacitor is recommended to reduce input noise.
5, 15, 16	LX	Inductor pin. Connect this pin to the switching node of the inductor.
6, 14, EP	GND	Ground pin.
7	PG	Power-good Indicator. Open-drain output when the output voltage is within 90% to 120% of the regulation point.
8	MODE	Operating mode selection under light load. Pull this pin low for PFM operation. Pull this pin high for FCCM operation. Do not leave this pin floating.
9	EN	Enable control pin. Pull high to turn on the IC and pull low to turn off the IC. Do not leave floating.
10	ILMT	Valley current-limit threshold selection pin. See Table 1 for details.
11	FB	Output feedback pin. Connect to the center point of the resistor-divider.
12	BYP	External 3.3V bypass power-supply input. Decouple this pin to GND with a 1 $\mu$ F ceramic capacitor. Leave this pin floating or connect this pin to the GND if it is not used.
13	V <sub>CC</sub>	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with a 2.2 $\mu$ F ceramic capacitor.

## Block Diagram

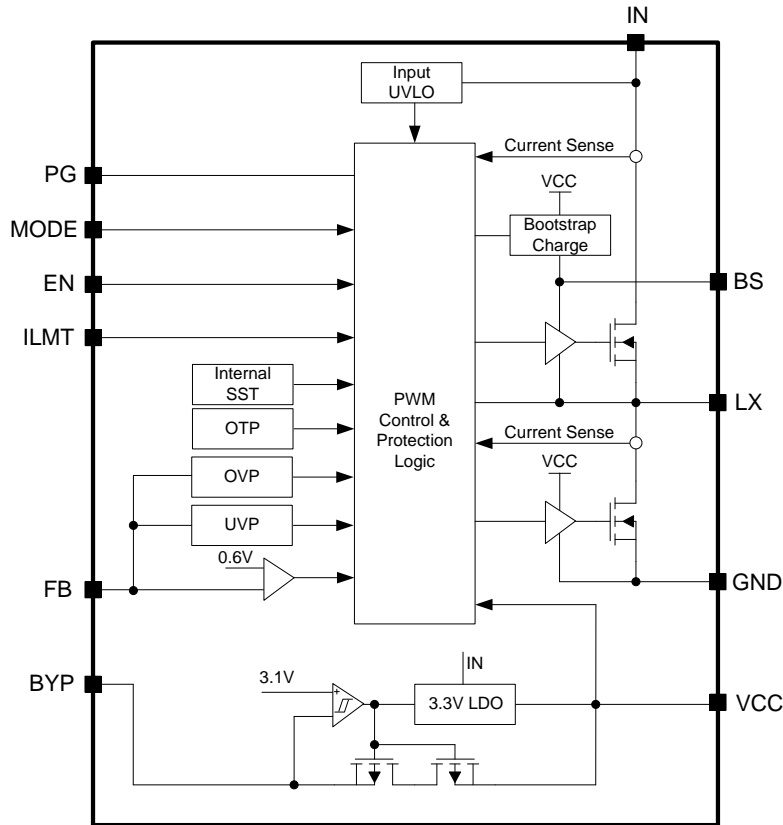


Figure 3. Block Diagram



## Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	26	V
IN-LX, LX, PG, MODE, EN	-0.3	IN + 0.3	
BS-LX, V <sub>CC</sub> , I <sub>LMT</sub>	-0.3	4	
BYP, FB	-0.3	6	
Dynamic LX Voltage in 10ns Duration (3)	GND - 5	IN + 3	
Dynamic LX Voltage in 20ns Duration (3)	GND - 5	IN + 2	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

## Thermal Information

Parameter (Note 2)	Min	Max	Unit
$\theta_{JA}$ Junction-to-ambient Thermal Resistance		33	°C/W
$\theta_{JC}$ Junction-to-case Thermal Resistance		5.5	
P <sub>D</sub> Power Dissipation T <sub>A</sub> = 25°C		3	W

## Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	4	24	V
Junction Temperature, Operating	-40	125	
Ambient Temperature	-40	85	A

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $C_{OUT} = 66\mu F$ ,  $T_A = 25^\circ C$ ,  $I_{OUT} = 1A$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input	Voltage Range	$V_{IN}$	4		24	V	
	UVLO Threshold	$V_{UVLO}$	$V_{IN}$ rising		3.9	V	
	UVLO Hysteresis	$V_{HYS}$		0.5		V	
	Quiescent Current	$I_Q$	PFM, $I_{OUT} = 0A$ , $V_{OUT} = V_{SET} \times 105\%$		140	170	$\mu A$
	Shutdown Current	$I_{SHDN}$	$EN = 0$		4	9	$\mu A$
Output	Voltage Range	$V_{OUT}$	0.78		12	V	
	Feedback Reference Voltage	$V_{REF}$	0.594	0.600	0.606	V	
	FB Input Current	$I_{FB}$	$V_{FB} = 1V$	-50		50	nA
	Discharge Current	$I_{DIS}$	$V_{OUT} = 5V$		100		mA
	Soft-Start Time	$t_{SS}$	$V_{FB}$ from 0% to 100% $V_{REF}$ (Note 4)		1.2	1.98	ms
	OVP Threshold	$V_{OVP}$	$V_{FB}$ rising	115	120	125	% $V_{REF}$
	OVP Hysteresis	$V_{OVP,HYS}$			5		% $V_{REF}$
	OVP Delay	$t_{OVP,DLY}$	(Note 4)		20		$\mu s$
	UVP Threshold	$V_{UVP}$		55	60	65	% $V_{REF}$
	UVP Delay	$t_{UVP,DLY}$	(Note 4)		200		$\mu s$
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$		20		m $\Omega$	
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$		10		m $\Omega$	
	Top FET Current Limit	$I_{LMT, TOP}$		22		A	
	Bottom FET Current Limit	$I_{LMT, BOT}$	$I_{LMT} = \text{low}$	8			A
			$I_{LMT} = \text{floating}$	12			A
$I_{LMT} = \text{high}$			16			A	
Bottom FET Reverse Current Limit	$I_{LMT, RVS}$	FCCM mode	3	4.8		A	
Enable(EN)	Input Voltage High	$V_{EN, H}$	1			V	
	Input Voltage Low	$V_{EN, L}$			0.4	V	
	Input Current	$I_{EN}$	$V_{EN} = 3.3V$		1	$\mu A$	
MODE	Voltage for PFM Mode	$V_{MODE, PFM}$	0		0.4	V	
	Voltage for FCCM Mode	$V_{MODE, FCCM}$	1		$V_{IN}$	V	
	Input Current	$I_{EN}$	$V_{MODE} = 3.3V$		1	$\mu A$	
$I_{LMT}$	Input Voltage High	$V_{ILMT, H}$	$V_{CC} - 0.8$			V	
	Input Voltage Low	$V_{ILMT, L}$			0.4	V	
Frequency	Switching Frequency	$f_{SW}$	$V_{OUT} = 5V$ , CCM	510	600	690	kHz
	Min ON Time	$t_{ON, MIN}$	$V_{IN} = V_{IN, MAX}$ (Note 4)		50		ns
	Min OFF Time	$t_{OFF, MIN}$			150		ns
Power Good	Rising Threshold	$V_{PG, F}$	$V_{FB}$ falling (not good)	80	83	86	% $V_{REF}$
	Hysteresis	$V_{PG, HYS}$	$V_{FB}$ rising (good)		7		% $V_{REF}$
	Delay Time	$t_{PG, R}$	Low to high (Note 4)		200		$\mu s$
		$t_{PG, F}$	High to low (Note 4)		30		$\mu s$
$V_{CC}$	Low Voltage	$V_{PG, LOW}$	$V_{FB} = 0V$ , $I_{PG} = 5mA$			0.45	V
	Output Voltage	$V_{CC}$	$V_{CC}$ adds 1mA load	3.15	3.3	3.45	V



SILERGY

# SY21243A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BYP	R <sub>DS(ON)</sub>	R <sub>DS(ON),BYP</sub>		1.5		Ω
	Turn-On Voltage	V <sub>BYP</sub>	2.97	3.1		V
	Turn-On Hysteresis	V <sub>BYP,HYS</sub>		0.2		V
	OVP Voltage	V <sub>BYP,OVP</sub>		120		% V <sub>LDO</sub>
OTP	Temperature	T <sub>OTP</sub>	T <sub>J</sub> rising (Note 4)		150	°C
	Temperature Hysteresis	T <sub>OTP, HYS</sub>	(Note 4)		15	°C

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

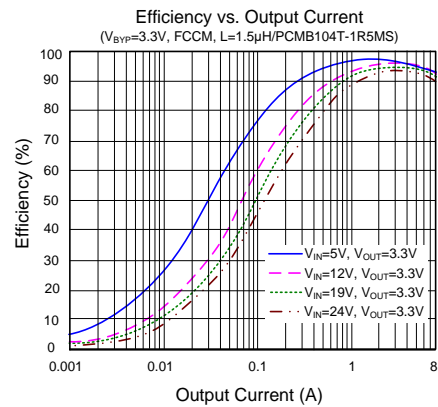
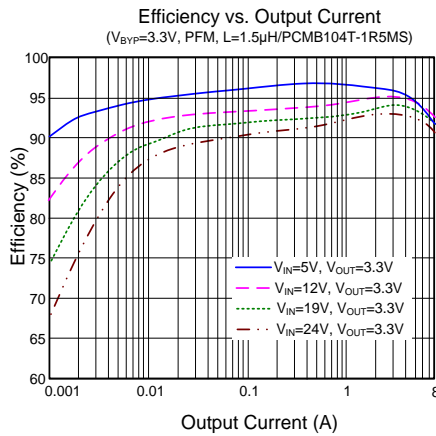
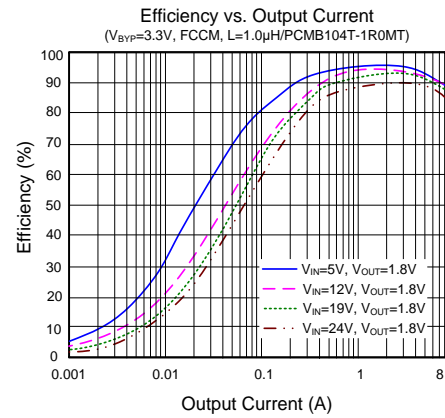
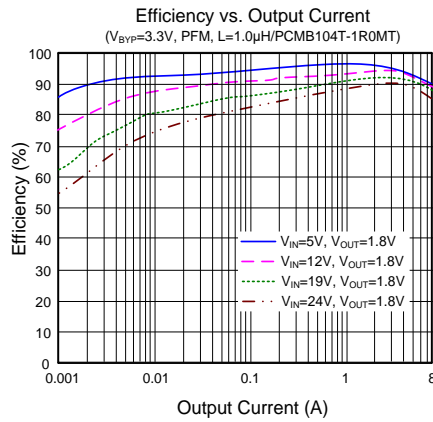
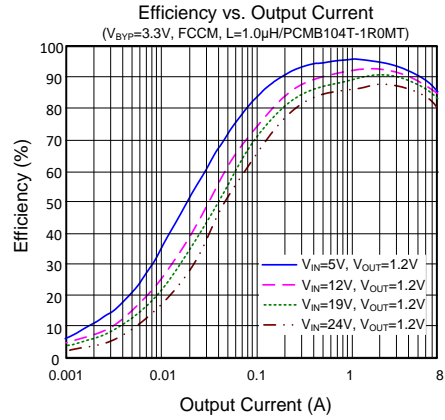
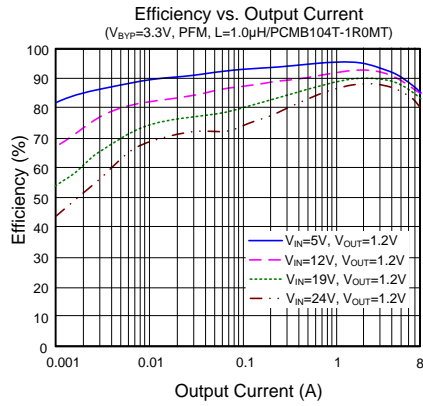
**Note 2:** Package thermal resistance is measured in the natural convection at T<sub>A</sub> = 25 °C on an 8.5cm × 8.5cm four-layer Silergy Evaluation Board with 2oz copper.

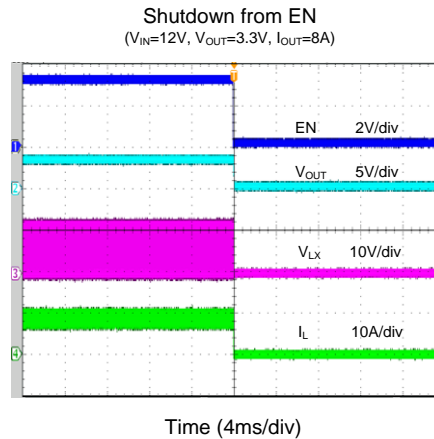
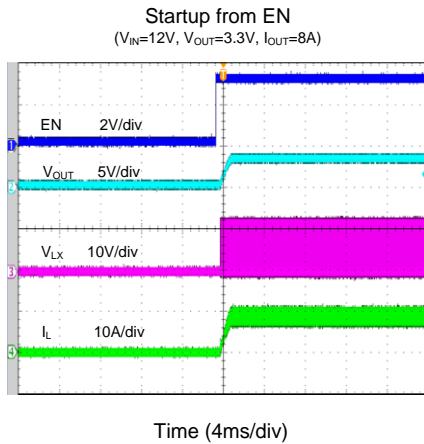
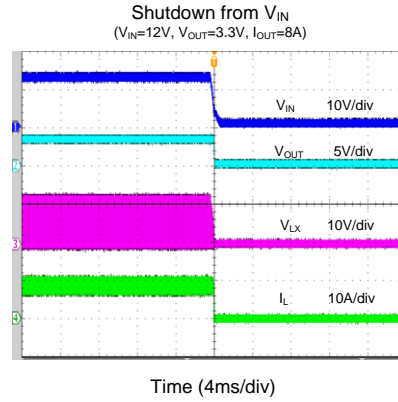
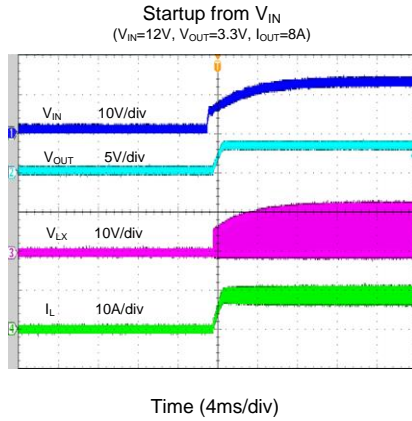
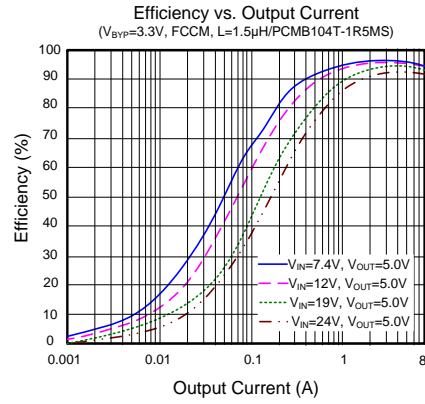
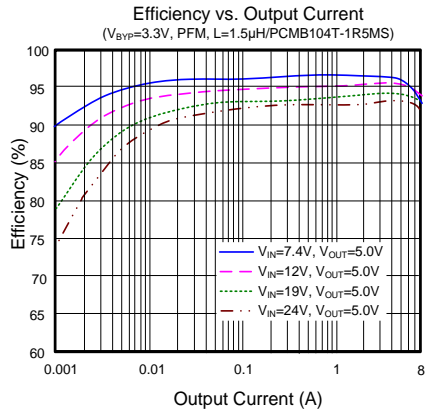
**Note 3:** The device is not guaranteed to function outside its operating conditions.

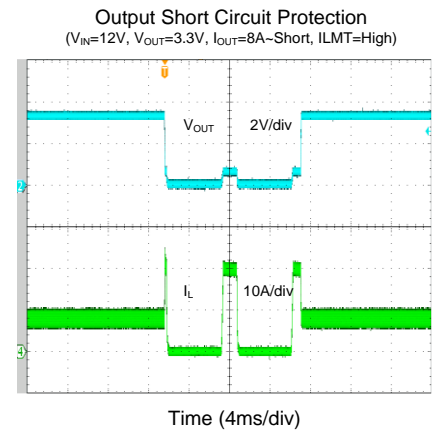
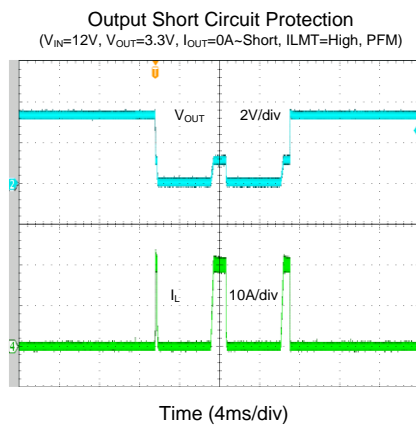
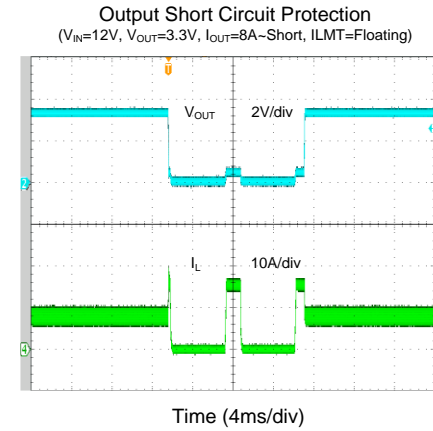
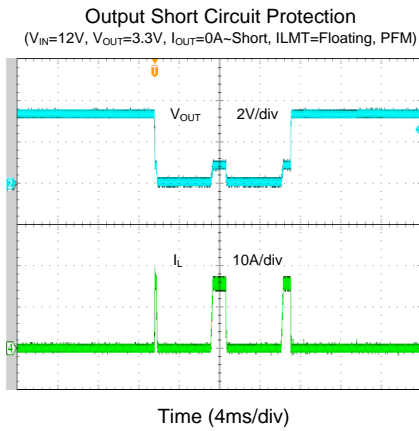
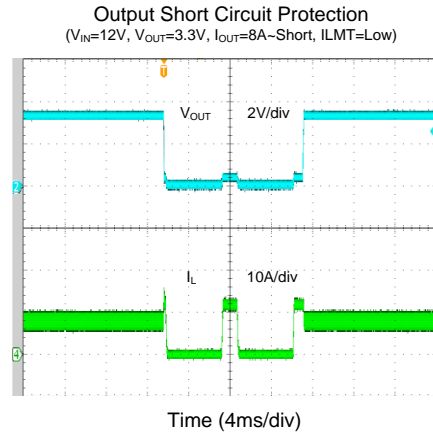
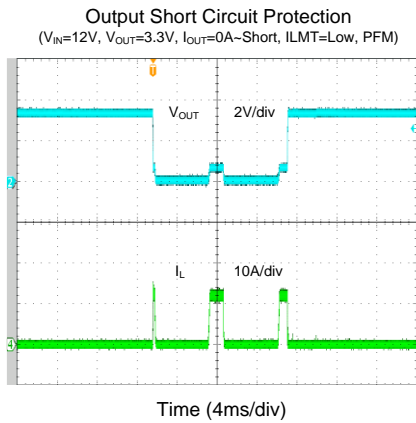
**Note 4:** Guaranteed by design.

## Typical Performance Characteristics

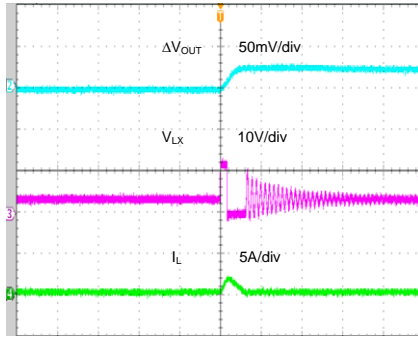
( $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 3.3\text{V}$ ,  $L = 1.5\mu\text{H}$ ,  $C_{OUT} = 66\mu\text{F}$ , unless otherwise noted)





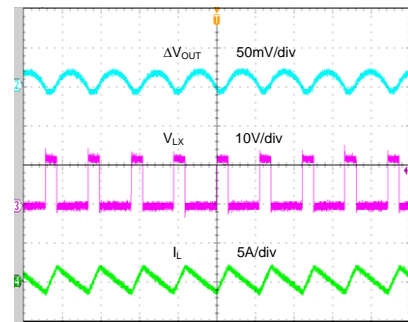


**Output Ripple**  
( $V_{IN}=12V$ ,  $V_{OUT}=3.3V$ ,  $I_{OUT}=0A$ , PFM)



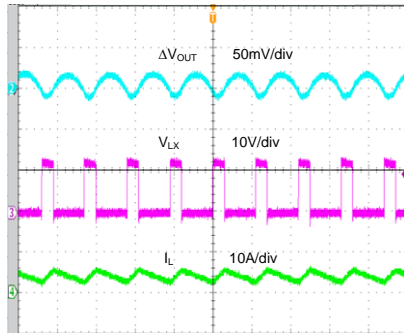
Time (2μs/div)

**Output Ripple**  
( $V_{IN}=12V$ ,  $V_{OUT}=3.3V$ ,  $I_{OUT}=0A$ , FCCM)



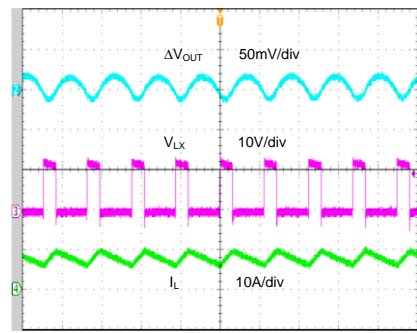
Time (2μs/div)

**Output Ripple**  
( $V_{IN}=12V$ ,  $V_{OUT}=3.3V$ ,  $I_{OUT}=4A$ )



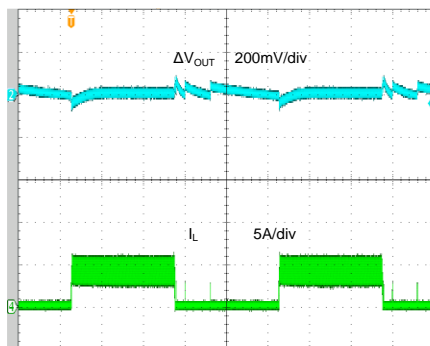
Time (2μs/div)

**Output Ripple**  
( $V_{IN}=12V$ ,  $V_{OUT}=3.3V$ ,  $I_{OUT}=8A$ )



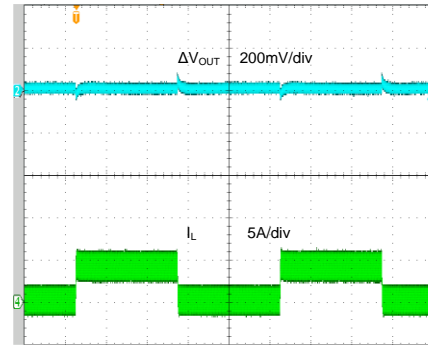
Time (2μs/div)

**Load Transient**  
( $V_{IN}=12V$ ,  $V_{OUT}=3.3V$ ,  $I_{OUT}=0-4A$ , PFM)

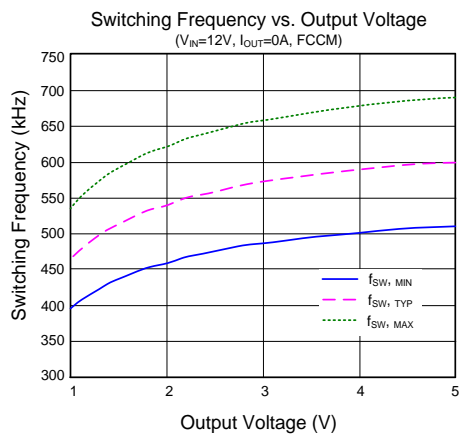
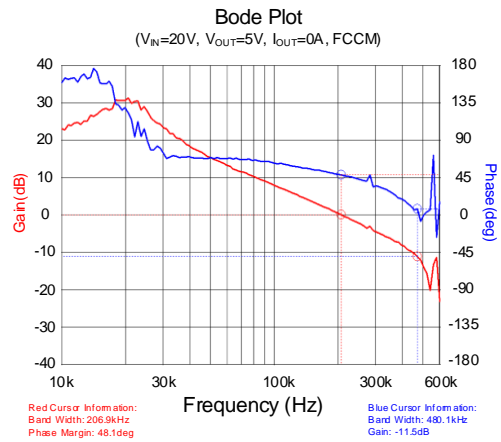
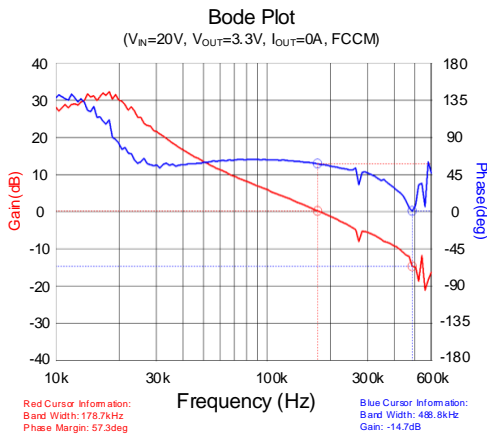
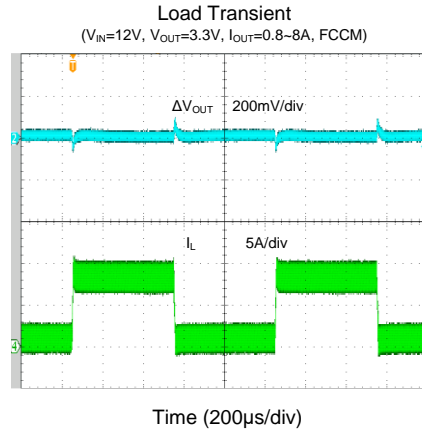
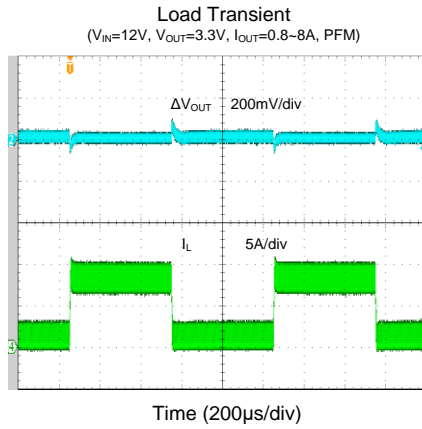


Time (200μs/div)

**Load Transient**  
( $V_{IN}=12V$ ,  $V_{OUT}=3.3V$ ,  $I_{OUT}=0-4A$ , FCCM)



Time (200μs/div)



## Detailed Description

### General Features

#### Constant-on-time Architecture

The one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch, is fundamental to any constant-on-time (COT) architecture. Each on-time ( $t_{ON}$ ) is a fixed period internally calculated to operate the step-down regulator at the desired switching frequency, considering the input and output voltage ratio,  $t_{ON} = (V_{OUT}/V_{IN}) \times (1/f_{SW})$ . For example, considering that a hypothetical converter targets 3.3V output from a 12V input at 600kHz, the target on-time is  $(3.3V/12V) \times (1/600kHz) = 458ns$ . Each  $t_{ON}$  pulse is triggered by the feedback comparator when the output voltage as measured at FB drops below the target value. After one  $t_{ON}$  period, a minimum off-time ( $t_{OFF,MIN}$ ) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids making any switching decisions during the noisy periods immediately after switching events, or while the switching node (LX) is rapidly rising or falling.

There is no fixed clock in a COT architecture, so the high-side power switch can turn on almost immediately after a load transient. Subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Conventional current-mode or voltage-mode control methods determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier based on current feedback, feedback voltage, internal ramps, and internal compensation signals, so these must all be monitored. These signals are difficult to observe immediately after switching large currents, however, which makes such architectures difficult to implement in noisy environments and at low duty cycles.

#### Minimum Duty Cycle and Maximum Duty Cycle

There is no limitation for minimum duty cycle in COT architecture. This is because when the on-time is close to the minimum on-time, the switching frequency can be reduced as needed to always ensure proper operation.

The SY21243A can support approximately 75% maximum duty cycle operation under  $T_J = -40-125^\circ C$  condition.

### Instant-PWM Operation

Silergy's instant-PWM control method adds several proprietary improvements to the traditional COT architecture. First, whereas most legacy COT implementations require a dedicated connection to the output voltage terminal to calculate the  $t_{ON}$  duration, the instant-PWM control method derives this signal internally.

Additionally, it optimizes operation with low-ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain smooth operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the  $t_{ON}$  pulse is triggered as long as the minimum  $t_{OFF}$  has been satisfied and the inductor current as measured in the low-side synchronous rectifier is lower than the bottom FET current limit. When the  $t_{ON}$  pulse is triggered, the low-side synchronous rectifier turns off and the high-side power switch turns on. The inductor current then ramps up linearly during the  $t_{ON}$  period. At the conclusion of the  $t_{ON}$  period, the high-side power switch turns off, the low-side synchronous rectifier turns on, and the inductor current ramps down linearly.

This action also initiates the minimum  $t_{OFF}$  timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum  $t_{OFF}$  is relatively short so that transient  $t_{ON}$  can be retriggered with minimal delay during high-speed load, allowing the inductor current to ramp quickly and provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time ( $t_{DEAD}$ ) is generated internally between the time when the high-side power switch turns off and the low-side synchronous rectifier on-period, or between the time when the low-side synchronous rectifier turns off and the high-side power switch on-period.

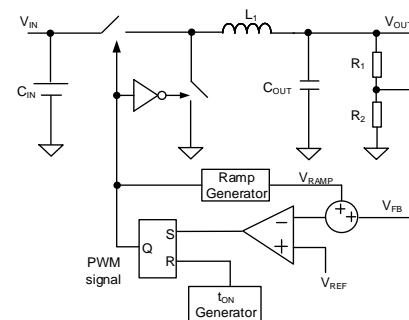


Figure 4. Instant-PWM

## Light-Load Operation Mode Selection

PFM or FCCM light-load operation is selected by the MODE pin. Pull MODE low for PFM operation or high for FCCM operation.

If PFM light-load operation is selected, under light load conditions (typically  $I_{OUT} < 1/2 \times \Delta I_L$ ), the current through the low-side synchronous rectifier will ramp to near zero before the next  $t_{ON}$  time. When this occurs, the low-side synchronous rectifier turns off, preventing recirculation current that can seriously reduce efficiency under light-load conditions. As load current is further reduced and the combined feedback and ramp signals remain much greater than the reference voltage, the instant-PWM control loop will not trigger another  $t_{ON}$  until needed. The apparent operating switching frequency will drop accordingly, further enhancing efficiency. The switching frequency can be lower than audible frequency area under deep light-load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next  $t_{ON}$  cycle. The device enters CCM once the load current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range. The critical level of the load current is determined as follows:

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1-D)}{2 \times f_{SW} \times L_1}$$

If FCCM light-load operation is selected, under light-load conditions, the low-side synchronous rectifier still turns on even when the inductor current crosses zero. Current flow will continue until the next  $t_{ON}$  cycle. In this mode, the SY21243A keeps fairly constant switching frequency across the output current range.

## Input Undervoltage Lockout (UVLO)

To prevent operation before all internal circuitry is ready, and to ensure that the power and synchronous rectifier switches work reliably, instant-PWM incorporates input undervoltage lockout protection. The SY21243A remains in a low-current state and all switching actions are inhibited until  $V_{IN}$  exceeds the UVLO (rising) threshold. At that time, if EN is enabled, the device will start up by initiating a soft-start ramp. If  $V_{IN}$  falls below  $V_{UVLO}$  by less than the input UVLO hysteresis, switching actions will again be suppressed.

If required, Increasing the default input UVLO threshold is possible by using a resistor divider to the EN pin as shown in Figure 5.

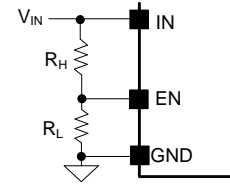


Figure 5. UVLO adjustment

## Enable Control

The EN input is a high-voltage capable input with logic-compatible threshold. When EN is driven above 1V, normal device operation is enabled. When driven to less than 0.4V, the device will shut down, reducing input current to less than 10 $\mu$ A.

It is not recommended to connect EN and IN directly. Use a resistor with a value between 1k $\Omega$  and 1M $\Omega$  if EN is pulled high to  $V_{IN}$ .

## Startup and Shutdown

The SY21243A incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1.2ms, which avoids high current flow and transients during startup. The startup and shutdown sequences are shown in Figure 6.

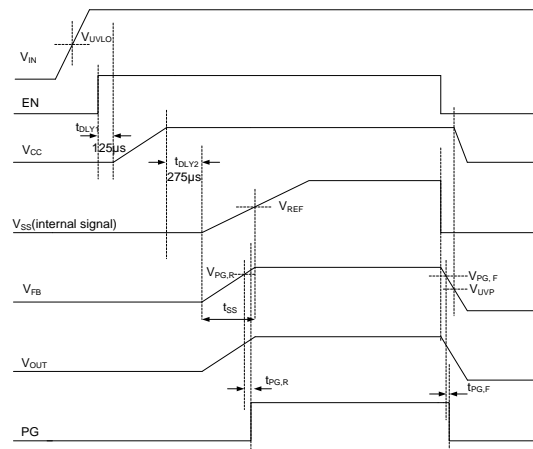


Figure 6. Startup and shutdown sequence

Once the input voltage exceeds its own UVLO (rising) threshold,  $V_{CC}$  is turned on after EN is enabled for one delay time  $t_{DLY1}$ . After the  $V_{CC}$  ramps up, the buck

regulator is turned on after delay time  $t_{DLY2}$ . When the output voltage is 90% of the regulation target, PG becomes high-impedance after a  $t_{PG,R}$  delay.

If the output is pre-biased to a certain voltage before startup, the device disables the switching of both the high-side power switch and the low-side synchronous rectifier until the voltage on the internal soft start circuit voltage  $V_{SS}$  exceeds the sensed output voltage at the FB node.

### Output Discharge

The SY21243A discharges the output voltage when the converter shuts down from  $V_{IN}$  or EN, or due to thermal shutdown, so that output voltage can be discharged in a minimal amount of time, even if the output load current is zero. The discharge FET in parallel with the low-side synchronous rectifier turns on after the low-side synchronous rectifier turns off when shutdown logic is triggered. The output discharge current is typically 100mA when LX voltage is 5V. Note that the discharge FET is not active outside these shutdown conditions.

### Output Power-Good Indicator

The buck power-good indicator is an open-drain output controlled by a window comparator connected to the feedback signal. If  $V_{FB}$  is greater than  $V_{PG,R}$  and less than  $V_{OVP}$  for at least the power-good delay time (low to high), PG will be high-impedance.

PG should be connected to  $V_{IN}$  or another voltage source through a resistor (e.g., 100k $\Omega$ ). After the input voltage exceeds its own UVLO (rising) threshold, the PG MOSFET is turned on so that PG is pulled to GND before output voltage is ready. After the feedback voltage  $V_{FB}$  reaches  $V_{PG,R}$ , PG is pulled high (after one delay time, typical 200 $\mu$ s). When  $V_{FB}$  drops to  $V_{PG,F}$ , or rises to  $V_{OVP}$  for one OVP delay time, PG is pulled low (after one delay time, typical 30 $\mu$ s).

### External Bootstrap Capacitor Connection

The SY21243A integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1 $\mu$ F low-ESR ceramic capacitor to be connected between BS and LX.

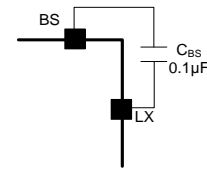


Figure 7. Bootstrap capacitor connection

### V<sub>CC</sub> Linear Regulator

An internal linear regulator ( $V_{CC}$ ) produces a 3.3V supply from  $V_{IN}$  that powers the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a 2.2 $\mu$ F low-ESR ceramic capacitor from  $V_{CC}$  to GND as shown in Figure 8.

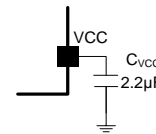


Figure 8. V<sub>CC</sub> regulator

## BYP Input

The control and drive circuit can also be powered by an external 3.3V power supply. When a 3.3V external power supply is connected to the BYP pin, the V<sub>CC</sub> LDO is turned off and the switch between BYP and V<sub>CC</sub> is turned on. The overall efficiency may be improved by connecting the BYP pin to an external 3.3V switching power supply. Connect a 1.0μF low-ESR ceramic capacitor from the BYP pin to GND when BYP is supplied by 3.3V external power. Leave the BYP pin floating or connect this pin to the GND pin if it is not used.

## Fault Protection Modes

### Output Current Limit

Instant-PWM architecture incorporates a cycle-by-cycle “valley” current limit. The inductor current is measured in the low-side synchronous rectifier when it turns on and as the inductor current ramps down. If the current exceeds the bottom FET current-limit threshold, t<sub>ON</sub> is inhibited until the current returns to a level at or below the limit threshold, as shown in Figure 9.

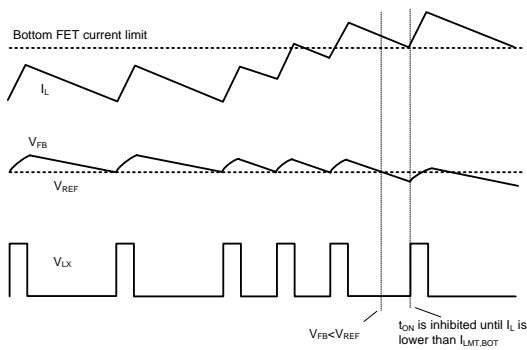


Figure 9. Output current limit

The valley current-limit threshold is programmable using the I<sub>LMT</sub> pin. Pull I<sub>LMT</sub> low, floating, or high to configure the target valley current-limit threshold. The detailed pin configuration is shown in Table 1. When the valley current-limit is reached, the output current-limit value is given by the following equations:

$$I_{LMT,OUT} = I_{LMT,BOT} + \Delta I_L / 2,$$

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

Table 1. Programmable valley current limit

I <sub>LMT</sub>	I <sub>LMT,BOT</sub>	Recommended Table
I <sub>LMT</sub> = low	≥8A	Pull I <sub>LMT</sub> to GND using ≤10kΩ resistor
I <sub>LMT</sub> = floating	≥12A	I <sub>LMT</sub> pin floating
I <sub>LMT</sub> = high	≥16A	Pull I <sub>LMT</sub> to V <sub>CC</sub> using ≤10kΩ resistor

When FCCM light-load operation is selected, there is one bottom-FET reverse-current limit to ensure the negative current can be limited to a safe level. The low-side synchronous rectifier current is monitored during time t<sub>OFF</sub>. If the monitored current exceeds the reverse-current limit, the low-side synchronous rectifier is turned off and another t<sub>ON</sub> is triggered.

The SY21243A also incorporates a cycle-by-cycle “peak” current limit (top FET current limit). The high-side power-switch current is monitored during t<sub>ON</sub> time. If the monitored current exceeds the top-FET current limit, the high-side power switch is turned off, the low-side synchronous rectifier is turned on, and t<sub>ON</sub> is inhibited. t<sub>ON</sub> is no longer inhibited once low-side synchronous-rectifier current is lower than the bottom-FET current-limit value.

### Output Undervoltage Protection (UVP)

If V<sub>OUT</sub> is less than approximately 60% of the target output voltage for approximately 200μs when the output short circuits or the load current is much higher than the maximum current capacity, the output undervoltage protection (UVP) will be triggered, and the device will enter into hiccup protection mode. The hiccup on-time is 1.5ms, and the hiccup off-time is 6ms. If the output fault conditions are removed, the device will return to normal operation in the subsequent hiccup on time, as shown in Figure 10.

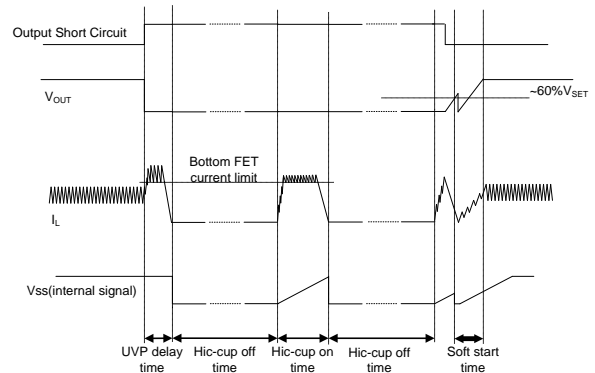


Figure 10. Output undervoltage protection

To avoid output overshoot, the internal soft-start circuit voltage  $V_{SS}$  is pulled low temporarily when  $V_{FB}$  exceeds the UVP threshold if the output fault conditions are removed during hiccup on-time, and then the  $V_{SS}$  rises smoothly to ramp the output to the desired voltage during a new soft-start cycle.

### Output Overvoltage Protection (OVP)

If the output voltage rises above the feedback regulation level, the high-side power switch naturally remains off, and various protections are activated depending on the operation mode.

When operating in PFM light-load mode, if the output voltage remains high, the low-side synchronous rectifier remains on until the inductor current reaches zero and the switching actions are suppressed. The switching actions are resumed once the combined feedback and ramp signals are lower than the reference voltage.

When operating in FCCM mode, if the output voltage remains high, the reverse-current limit will be triggered and the inductor current average value becomes negative as the device attempts to lower the output voltage. If the output voltage continues to rise and exceeds the output overvoltage threshold for more than the OVP delay time, the output overvoltage protection (OVP) is triggered and the switching actions are suppressed. The switching will resume once the combined feedback and ramp signals are lower than the reference voltage. False OVP may happen under light-load conditions if the chosen inductance is too small and the reverse-current limit is triggered.

### Overtemperature Protection (OTP)

Instant-PWM includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds  $150^{\circ}\text{C}$ . Once the junction temperature cools by approximately  $15^{\circ}\text{C}$ , the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

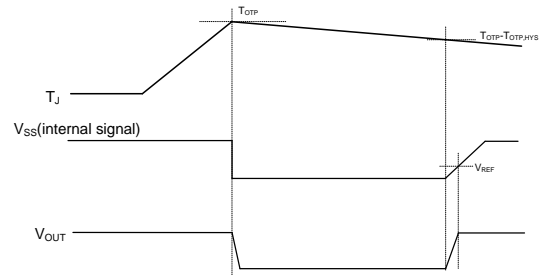


Figure 11. Overtemperature protection

## Application Information

### Feedback Resistor-Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. A value between 10kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. For example, if V<sub>SET</sub> is 3.3V and R<sub>1</sub> = 100kΩ, then R2 can be calculated using the following equation:

$$R2 = \frac{0.6V}{V_{SET} - 0.6V} \times R1$$

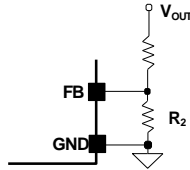


Figure 12. Feedback resistor selection

With a calculated value of 22.2kΩ for R2, a standard 1% 22.1kΩ resistor is selected.

### Input Capacitor Selection

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10μF X5R capacitor is sufficient in most applications.

## Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost, and size for a particular application. Selecting a low inductor value will help reduce size and cost, and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low-value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current ( $\Delta I_L$ ) approximately 20–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency ( $f_{SW}$ ), the maximum output current ( $I_{OUT,MAX}$ ), and estimated  $\Delta I_L$  as a percentage of that current:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current ( $\Delta I_L$ ) and required peak-current inductor current  $I_{L,PEAK}$ .

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \Delta I_L / 2$$

Select an inductor with a saturation current and thermal rating in excess of  $I_{L,PEAK}$ .

If FCCM light-load operation is selected, make sure the inductor value is high enough to avoid triggering the reverse-current limit under steady state if the load current is zero.

For maximum efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low-loss ferrite materials should be considered.

## Inductor Design Example

Consider a typical design for a device providing 3.3V<sub>OUT</sub> at 8A from 12V<sub>IN</sub>, operating at 600kHz and using target inductor ripple current ( $\Delta I_L$ ) of 40% or 3.2A. First determine the approximate inductance value:

$$L_1 = \frac{3.3V \times (12V - 3.3V)}{12V \times 600kHz \times 3.2A} = 1.246\mu H$$

Next, select the nearest standard inductance value (in this case 1.5 $\mu$ H) and calculate the resulting inductor ripple current ( $\Delta I_L$ ):

$$\Delta I_L = \frac{3.3V \times (12V - 3.3V)}{12V \times 600kHz \times 1.5\mu H} = 2.66A$$

$$I_{L,PEAK} = 8A + 2.66A / 2 = 9.33A$$

The resulting 2.66A ripple current is approximately 33.3% (2.66A/8A), well within the 20–40% target.

$$I_{L,PEAK,RVS} = 2.66A / 2 = 1.33A < I_{LIM,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting  $I_{L,PEAK}$  of 9.33A.

## Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

## Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple ( $\Delta I_L$ ) on the output capacitors ESR (ESR ripple), as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{\text{RIPPLE,ESR}} = \Delta I_L \times \text{ESR}$$

$$V_{\text{RIPPLE,CAP}} = \frac{\Delta I_L}{8 \times C_{\text{OUT}} \times f_{\text{SW}}}$$

Consider a typical application with  $\Delta I_L = 2.66\text{A}$  using three  $22\mu\text{F}$  ceramic capacitors, each with an ESR of approximately  $6\text{m}\Omega$  for a parallel total of  $66\mu\text{F}$  and  $2\text{m}\Omega$  ESR.

$$V_{\text{RIPPLE,ESR}} = 2.66\text{A} \times 2\text{m}\Omega = 5.32\text{mV}$$

$$V_{\text{RIPPLE,CAP}} = \frac{2.66\text{A}}{8 \times 66\mu\text{F} \times 600\text{kHz}} = 8.40\text{mV}$$

Total ripple =  $13.72\text{mV}$ . The actual capacitive ripple may be higher than the calculated value because the capacitance decreases with the voltage on the capacitor.

Using a  $150\mu\text{F}$   $40\text{m}\Omega$  POS cap, the result is as follows:

$$V_{\text{RIPPLE,ESR}} = 2.66\text{A} \times 40\text{m}\Omega = 106.40\text{mV}$$

$$V_{\text{RIPPLE,CAP}} = \frac{2.66\text{A}}{8 \times 150\mu\text{F} \times 600\text{kHz}} = 3.69\text{mV}$$

Total ripple =  $110.09\text{mV}$ .

## Output Transient Undershoot/Overshoot

If very fast load transients must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, but some considerations are still required, especially when using small ceramic capacitors. These capacitors have low capacitance, which results in insufficient stored energy for load transients. Output-transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor, and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as  $V_{\text{ESR}} = \Delta I_{\text{OUT}} \times \text{ESR}$ . Using the ceramic capacitor example above and a fast load transient of  $\pm 4\text{A}$ ,  $V_{\text{ESR}} = \pm 4\text{A} \times 2\text{m}\Omega = \pm 8\text{mV}$ . The POS capacitor result with the same load transient is  $V_{\text{ESR}} = \pm 4\text{A} \times 40\text{m}\Omega = \pm 160\text{mV}$ .

Capacitive undershoot (load increasing) is a function of the output capacitance, load step, inductor value, input-output voltage difference, and maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of  $t_{\text{ON}}$  and the minimum  $t_{\text{OFF}}$ , as the control scheme is designed to rapidly ramp the inductor current by grouping together many  $t_{\text{ON}}$  pulses in this case. The maximum duty factor  $D_{\text{MAX}}$  may be calculated as:

$$D_{\text{MAX}} = \frac{t_{\text{ON}}}{t_{\text{ON}} + t_{\text{OFF,MIN}}}$$

Given this, the capacitive undershoot may be calculated as:

$$V_{\text{UNDERSHOOT,CAP}} = -\frac{L_1 \times \Delta I_{\text{OUT}}^2}{2 \times C_{\text{OUT}} \times (V_{\text{IN,MIN}} \times D_{\text{MAX}} - V_{\text{OUT}})}$$

Consider a  $4\text{A}$  load increase using the ceramic capacitor case when  $V_{\text{IN}} = 12\text{V}$ . At  $V_{\text{OUT}} = 3.3\text{V}$ , the result is  $t_{\text{ON}} = 458\text{ns}$ ,  $t_{\text{OFF,MIN}} = 150\text{ns}$ ,  $D_{\text{MAX}} = 458 / (458 + 150) = 0.753$ , and:

$$V_{\text{UNDERSHOOT,CAP}} = -\frac{1.5\mu\text{H} \times (4\text{A})^2}{2 \times 66\mu\text{F} \times (12\text{V} \times 0.753 - 3.3\text{V})} = -31.7\text{mV}$$

Using the POS capacitor case, the above result is:

$$V_{\text{UNDERSHOOT,CAP}} = -\frac{1.5\mu\text{H} \times (4\text{A})^2}{2 \times 150\mu\text{F} \times (12\text{V} \times 0.753 - 3.3\text{V})} = -13.95\text{mV}$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, inductor value, and output voltage.

$$V_{\text{OVERSHOOT,CAP}} = \frac{L_1 \times \Delta I_{\text{OUT}}^2}{2 \times C_{\text{OUT}} \times V_{\text{OUT}}}$$

Consider a  $4\text{A}$  load decrease using the ceramic capacitor case above. At  $V_{\text{OUT}} = 3.3\text{V}$  the result is:

$$V_{\text{OVERSHOOT,CAP}} = \frac{1.5\mu\text{H} \times (4\text{A})^2}{2 \times 66\mu\text{F} \times 3.3\text{V}} = 55.1\text{mV}$$

Using the POS capacitor case, the above result is:

$$V_{\text{OVERSHOOT,CAP}} = \frac{1.5\mu\text{H} \times (4\text{A})^2}{2 \times 150\mu\text{F} \times 3.3\text{V}} = 24.2\text{mV}$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

### Load Transient Considerations

The SY21243A adopts the instant-PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC feed-forward compensation network  $R_{FF}$  and  $C_{FF}$  may further speed up the load-transient responses.  $R_{FF} = 1\text{k}\Omega$  and  $C_{FF} = 220\text{pF}$  have been shown to perform well in most applications. Increasing  $C_{FF}$  will speed up the load-transient response if there is no stability issue.

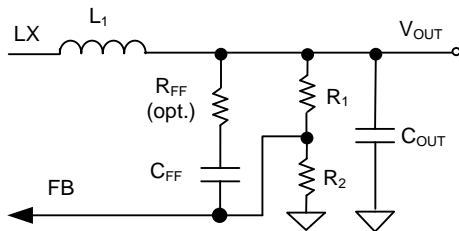


Figure 13. Feed-forward network

Note that when  $C_{OUT} > 500\mu\text{F}$  and minimum load current is low, using the feed-forward values  $R_{FF} = 1\text{k}\Omega$  and  $C_{FF} = 2.2\text{nF}$  is recommended to provide sufficient ripple to the FB node for reliable operation.

### Thermal Design Considerations

The maximum power dissipation depends on multiple factors: PCB layout, IC package thermal resistance, local airflow, and the junction temperature relative to ambient. The maximum power dissipation may be calculated as:

$$P_{D,\text{MAX}} = (T_{J,\text{MAX}} - T_A) / \theta_{JA}$$

Where,  $T_{J,\text{MAX}}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is  $125^\circ\text{C}$ . The junction to ambient thermal resistance  $\theta_{JA}$  is layout dependent. For the QFN2.5x2.5-16 package the thermal resistance  $\theta_{JA}$  is  $33^\circ\text{C/W}$  when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at  $T_A = 25^\circ\text{C}$  may be calculated using the following formula:

$$P_{D,\text{MAX}} = (125^\circ\text{C} - 25^\circ\text{C}) / (33^\circ\text{C/W}) = 3\text{W}$$

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J,\text{MAX}}$  and thermal resistance  $\theta_{JA}$ . Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

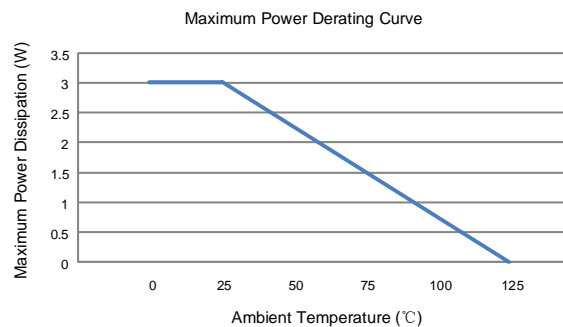
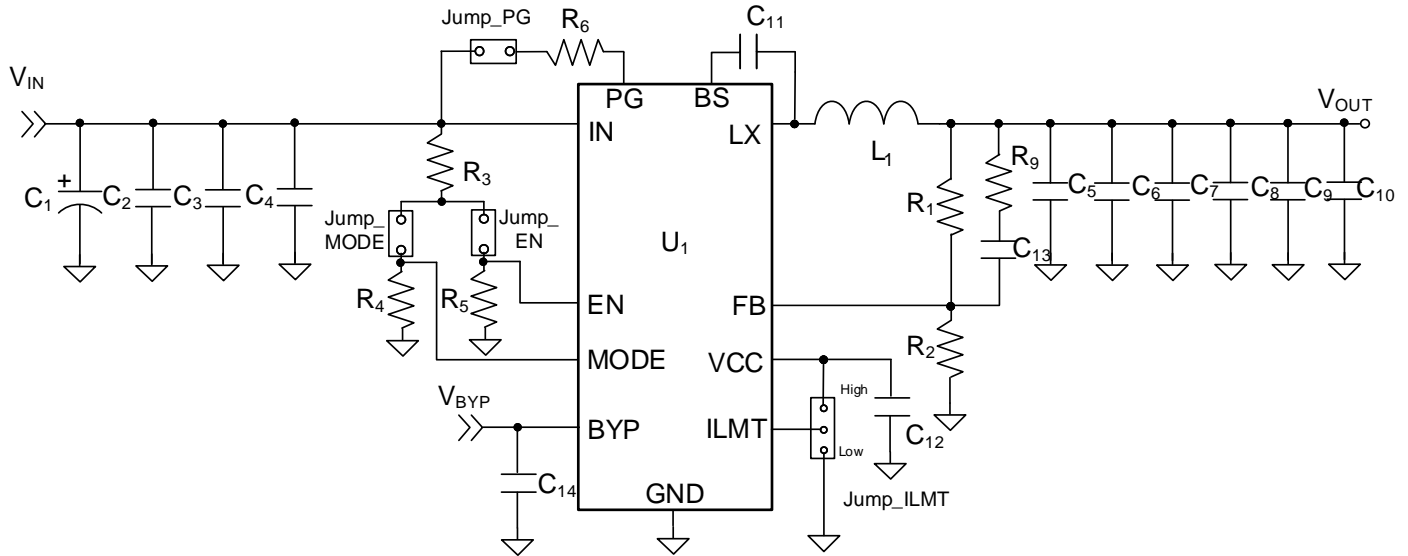


Figure 14. Maximum power dissipation

## Application Schematic ( $V_{OUT} = 3.3V$ )



## BOM List

Designator	Description	Part Number	Manufacturer
U1	8A, Buck	SY21243ARHC	Silergy
C1	47 $\mu$ F/50V Electrolytic Cap		
C2, C8, C9, C10	NC		
C3	10 $\mu$ F/50V/X5R, 1206	GRM31CR61H106KA12L	m $\mu$ Rata
C4, C11	0.1 $\mu$ F/50V/X5R, 0603	GRM188R61H104KA93D	m $\mu$ Rata
C5, C6, C7	22 $\mu$ F/16V/X5R, 1206	GRM31CR61C226ME15L	m $\mu$ Rata
C12	2.2 $\mu$ F/16V/X5R, 0603	GRM188R61C225KE15D	m $\mu$ Rata
C13	47pF/50V/C0G, 0603	GRM1885C1H470JA01D	m $\mu$ Rata
C14	1.0 $\mu$ F/25V/X5R, 0603	GRM155R61E105KE11D	m $\mu$ Rata
L1	1.5 $\mu$ H/16A, inductor	PCMB104T-1R5MS	CYNTEC
R1, R6	100k $\Omega$ , 1%, 0603		
R2	22.1k $\Omega$ , 1%, 0603		
R3	10k $\Omega$ , 1%, 0603		
R4, R5	1M $\Omega$ , 1%, 0603		
R7, R8	NC		
R9	1k $\Omega$ , 1%, 0603		

## Recommended Components for Typical Applications

$V_{OUT}$ (V)	R1 (k $\Omega$ )	R2 (k $\Omega$ )	C13 (pF)	L1/Part Number
1.2	100	100	220	1.0 $\mu$ H/PCMB104T-1R0MT
1.8	100	49.9	220	1.0 $\mu$ H/PCMB104T-1R0MT
3.3	100	22.1	47	1.5 $\mu$ H/PCMB104T-1R5MS
5.0	100	13.7	100	1.5 $\mu$ H/PCMB104T-1R5MS

## Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- **Input Capacitors:** Place the input capacitors very close to IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND by wide copper plane. An additional 0.1 $\mu$ F input ceramic capacitor, placed in parallel is recommended to reduce the input noise.
- **Output Capacitors:** Connect the C<sub>OUT</sub> negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- **V<sub>CC</sub> Capacitor:** Place the V<sub>CC</sub> capacitor close to V<sub>CC</sub> using a short, direct copper trace to one nearest device GND pin (pin 14).
- **BYP Capacitor:** Place the BYP capacitor close to BYP using short, a direct copper trace to the nearest device GND pin (pin 14) if the bypass function is used.
- **Feedback Network:** Place the feedback components (R<sub>1</sub>, R<sub>2</sub>, R<sub>FF</sub>, and C<sub>FF</sub>) as close to the FB pin as possible. Avoid routing the feedback line near LX, BS, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C<sub>OUT</sub> rather than the inductor output terminal.
- **LX Connection:** Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance. Use a wide LX copper trace between pin 5 and pins 15, 16 to improve efficiency.
- **BS Capacitor:** Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX, and C<sub>BS</sub>) as short as possible.
- **Control Signals:** It is not recommended to connect control signals directly to V<sub>IN</sub>. A resistor in a range of 1k $\Omega$  to 1M $\Omega$  should be used if the lines are pulled high to V<sub>IN</sub>.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place four GND vias on it for heat dissipation.
- **PCB Board:** A four-layer layout with 2oz copper is strongly recommended to achieve better thermal performance. The top and bottom layers should use power and GND copper pours as wide as possible. Middle1 layer should be assigned as a GND layer for conducting heat and shielding the Middle2 layer used for signal lines from top layer crosstalk. Place signal lines on the Middle2 layer instead of the other layers, to keep a solid GND plane.

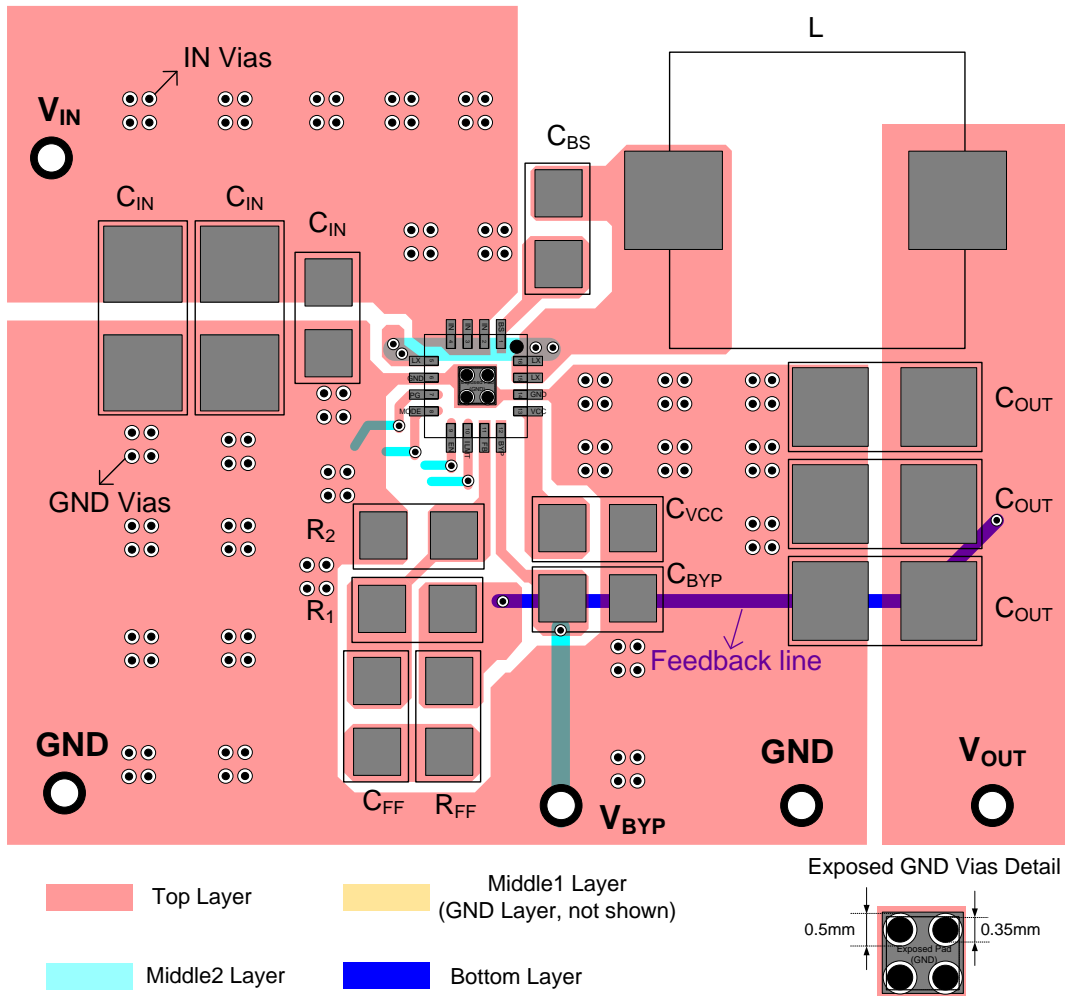
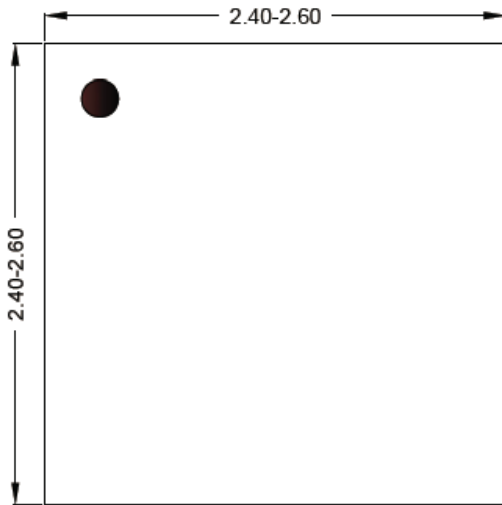
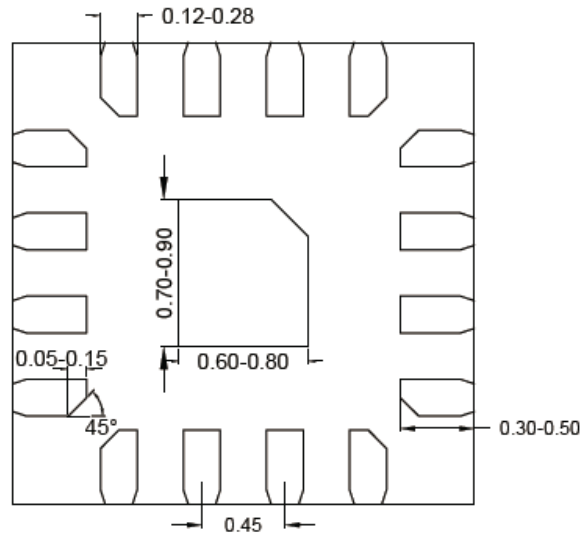


Figure 4. PCB Layout Suggestion

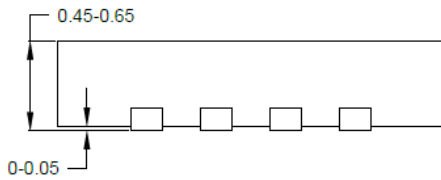
**QFN2.5x2.5-16 Package Outline and PCB Layout Design**



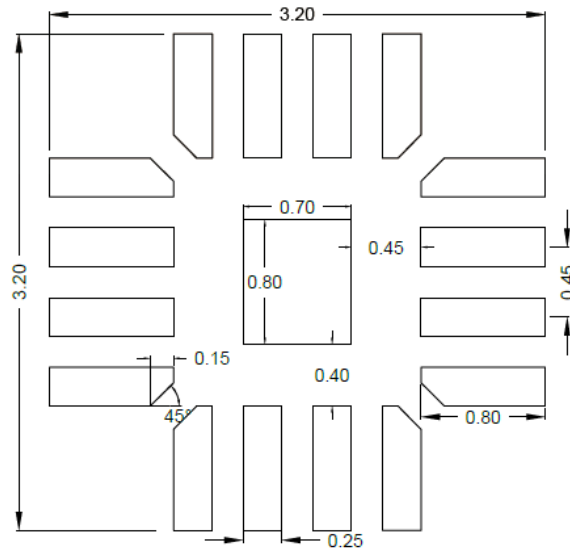
**Top view**



**Bottom view**



**Side view**

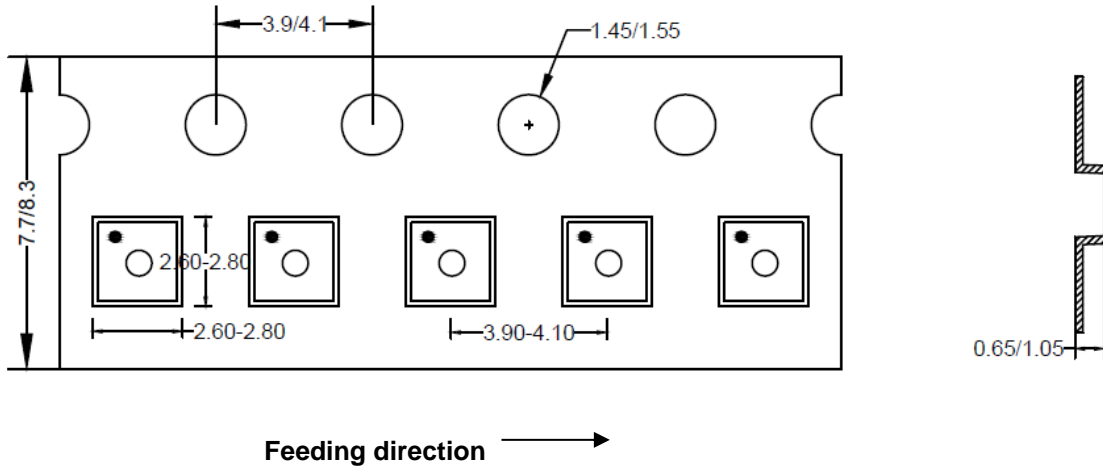


**Recommended PCB layout  
(Reference only)**

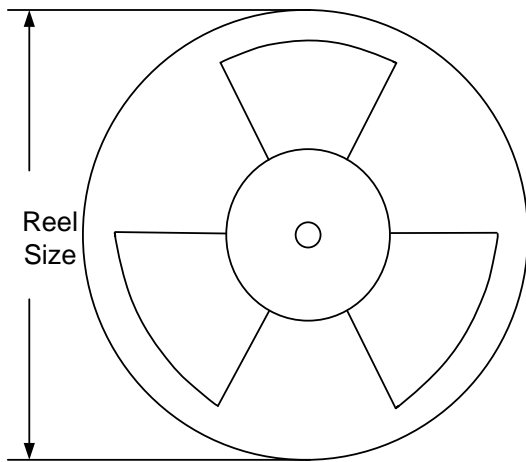
**Note: All dimensions are in millimeters and exclude mold flash and metal burr.**

**Taping and Reel Specification**

**QFN2.5x2.5 taping orientation**



**Carrier Tape and Reel specification for packages**



Package Types	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
QFN2.5x2.5	8	4	7"	400	160	3000

**Others: NA**

## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Aug.1,2023	Revision 1.0	Language improvements for clarity
Jan.22, 2021	Revision 0.9B	<ol style="list-style-type: none"> <li>1. Add (IN-LX) voltage in Absolute Maximum Ratings;</li> <li>2. Add "A 0.1μF input ceramic capacitor is recommended to reduce the input noise." in the pin description and the layout design;</li> <li>3. Update in Table1 (page14):               <ul style="list-style-type: none"> <li>----Change "Pull ILMT to GNG by 0~20kΩ" to "Pull ILMT to GND by ≤10kΩ Resistor" (ILMT = Low);</li> <li>---- Change "Pull ILMT to VCC by 0~150kΩ" to "Pull ILMT to VCC by ≤10kΩ Resistor" (ILMT = High).</li> </ul> </li> </ol>
Sep.21,2020	Revision 0.9A	Fixed an error in the calculation formula of $D_{MAX}$ ( $t_{ON}$ is 458ns) (page17)
Jul.24, 2020	Revision 0.9	Initial Release

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