

1.8V Minimum Input and 5.5V Maximum Output 3A Peak Current Synchronous Boost with Output Disconnect

General Description

The SY7063 is a high efficiency synchronous Boost regulator that converts down to 1.8V input and up to 5.5V output voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch. It can disconnect the output from input during the shutdown mode.

Ordering Information

SY7063 □(□□)□
 □ Temperature Code
 □ Package Code
 □ Optional Spec Code

Ordering Number	Package type	Note
SY7063QMC	QFN2×2-10	----

Features

- 1.8V Minimum Input Voltage
- Adjustable Output Voltage from 2.5V to 5.5V
- 3A Peak Current Limit
- Input Under Voltage Lockout
- Load Disconnect during Shutdown
- Output Over Voltage Protection
- Input Battery Voltage Monitor
- Low $R_{DS(ON)}$ (Main Switch/Synchronous Switch) at 5.0V Output: 36/40m Ω
- Output Auto-discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: QFN2×2-10

Applications

- All Single-cell Li or Dual-cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment

Typical Applications

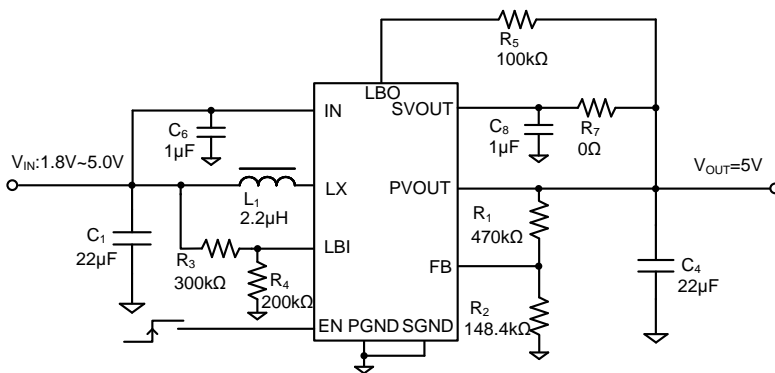


Figure 1. Schematic Diagram

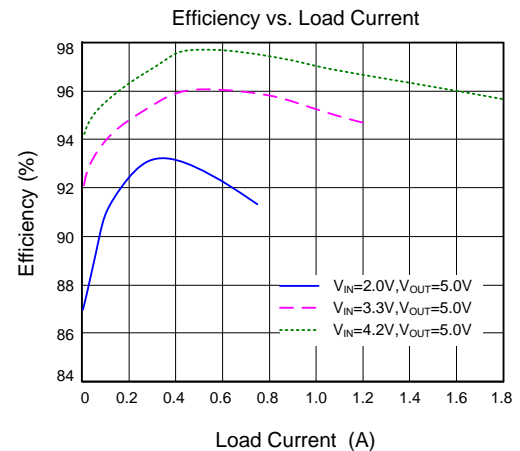
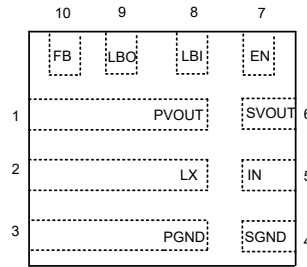


Figure 2. Efficiency Figure

Pinout (top view)



(QFN2x2-10)

Top mark: **UJxyz** (Device code: UJ, *x*=year code, *y*=week code, *z*=lot number code)

Name	QFN2x2-10	Description
PVOUT	1	Power output pin. Decouple this pin to the GND pin with at least a 22μF ceramic capacitor.
LX	2	Inductor node. Connect an inductor between the IN pin and the LX pin.
PGND	3	Power ground pin.
SGND	4	Signal ground pin.
IN	5	Signal input pin.
SVOUT	6	Signal output pin. Decouple this pin to the GND pin with at least a 1.0μF ceramic capacitor for noise immunity consideration.
EN	7	Enable pin. Internal integrated with a 1MΩ pull-down resistor.
LBI	8	Low battery comparator input.
LBO	9	Low battery comparator output (open-drain).
FB	10	Feedback pin. Connect a resistor R_1 between the OUT and the FB, and a resistor R_2 between the FB and the GND to program the output voltage. $V_{OUT}=1.2V \times (R_1/R_2+1)$.

Block Diagram

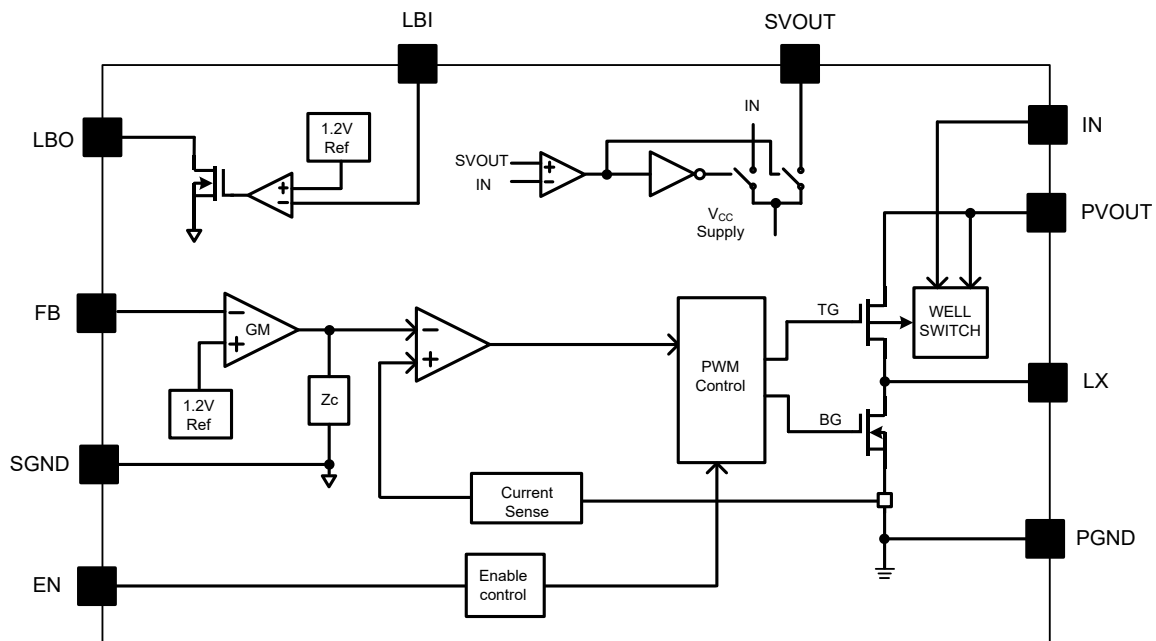


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

EN-----	-V _{OUT} +0.3V
Other Pins-----	6V
Power Dissipation, P _D @ T _A =25°C QFN2×2-10-----	2.5W
Package Thermal Resistance (Note 2)	
θ _{JA} -----	50°C/W
θ _{JC} -----	10°C/W
Junction Temperature Range -----	150°C
Lead Temperature (Soldering, 10 sec.) -----	260°C
Storage Temperature Range -----	-65°C to 150°C

Recommended Operating Conditions (Note 3)

IN -----	1.8V to 5.25V
PVOUT, SVOUT-----	2.5V to 5.5V
EN -----	0V to V _{OUT} +0.3V
All other pins -----	0-5.5V
Junction Temperature Range -----	-40°C to 125°C
Ambient Temperature Range -----	-40°C to 85°C

Electrical Characteristics

(V_{IN}=2.4V, V_{OUT}=5V, I_{OUT}=500mA, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V _{IN}		1.8		5.25	V
Output Voltage Range	V _{OUT}		2.5		5.5	V
Quiescent Current	V _{IN}	I _O =0A, V _{EN} =V _{IN} =1.8V, V _{OUT} =5.0V		10		μA
	V _{OUT}			27		μA
Shutdown Current	I _{SHDN}	V _{EN} =0V, V _{IN} =2.4V		0.1	1	μA
Linear Charge Current	I _{CHARGE}	V _{OUT} ≤1V		1.5		A
		1V<V _{OUT} <90% V _{IN}		1.2		
Soft-start Time	t _{SS}			1		ms
Input V _{IN} UVLO Threshold	V _{UVLO}				1.78	V
V _{IN} UVLO Hysteresis	V _{HYS}			0.1		V
EN Rising Threshold	V _{ENH}		1.2			V
EN Falling Threshold	V _{ENL}				0.4	V
LBI Voltage Threshold	V _{LBI}		1.176	1.2	1.224	V
LBI Input Hysteresis	V _{LBI_HYS}			20		mV
Low Side Main FET R _{ON}	R _{D(S)ON1}	V _{OUT} =5.0V		36		mΩ
Synchronous FET R _{ON}	R _{D(S)ON2}	V _{OUT} =5.0V		40		mΩ
Main FET Current Limit	I _{LIM1}		3.2			A
Switching Frequency	f _{SW}			500		kHz
Feedback Reference Voltage	V _{REF}		1.182	1.2	1.218	V
Output Over Voltage Protection	V _{OV} P			6		V
Minimum ON Time	t _{ON_MIN}			100		ns
Minimum OFF Time	t _{OFF_MIN}			100		ns
Max ON Time	t _{ON_MAX}			2		μs
Thermal Shutdown Temperature	T _{SD}			150		°C
Thermal Shutdown Hysteresis	T _{HYS}			20		°C
Output Discharge Resistor	R _{DSC}			80		Ω



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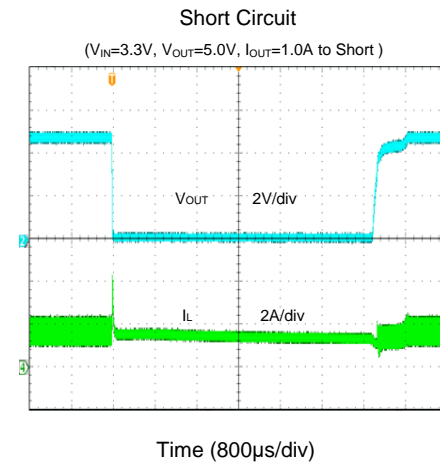
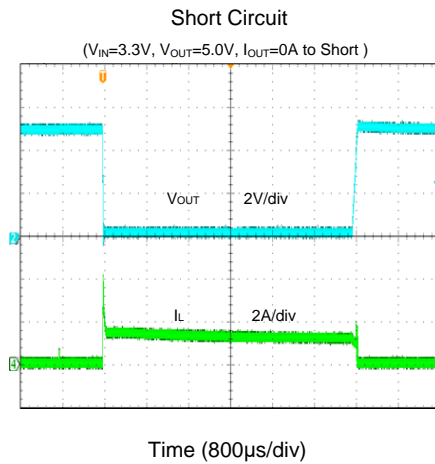
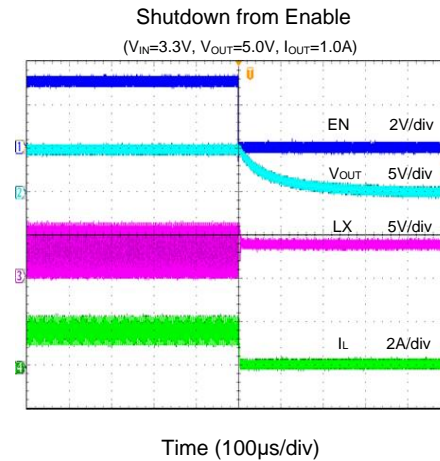
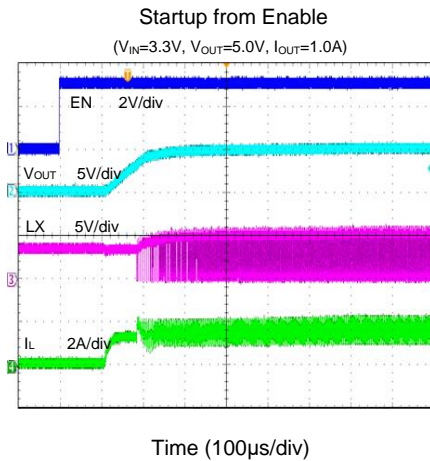
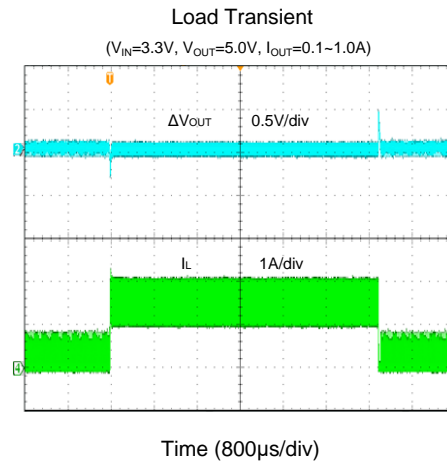
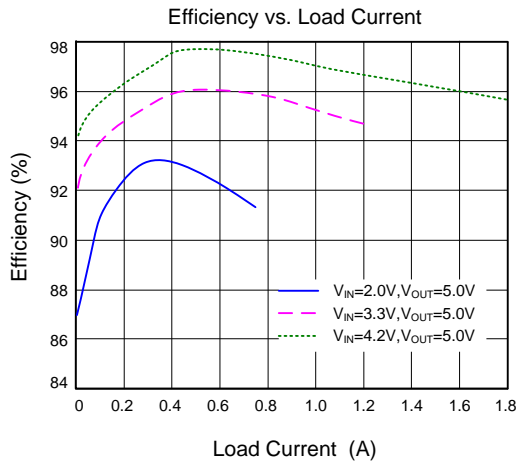
SY7063

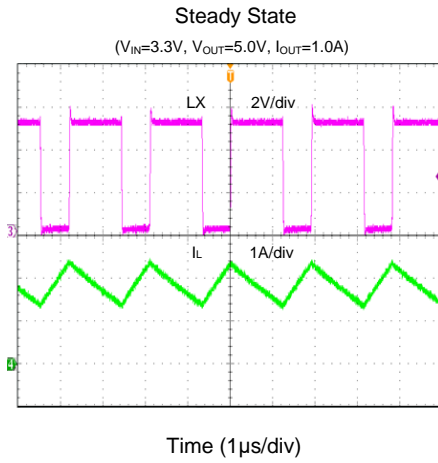
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a four-layer Silergy evaluation board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics





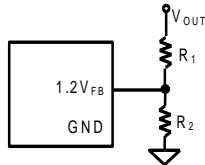
Applications Information

Because of the high integration for the SY7063, only the input capacitor C_{IN} , the output capacitor C_{OUT} , the inductor L and the feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2 :

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2 . A value of between $10k\Omega$ and $1M\Omega$ is recommended for both resistors. If V_{OUT} is $5.0V$, $R_1=470k\Omega$ is chosen, using the following equation, then R_2 can be calculated to be $148.4k\Omega$:

$$R_2 = \frac{1.2V}{V_{OUT} - 1.2V} R_1 \quad (1)$$



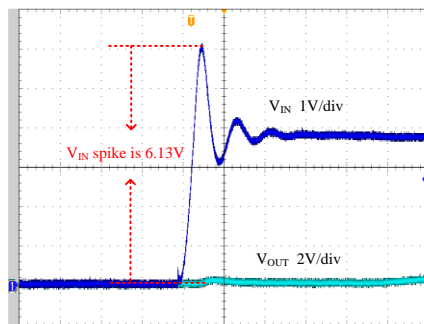
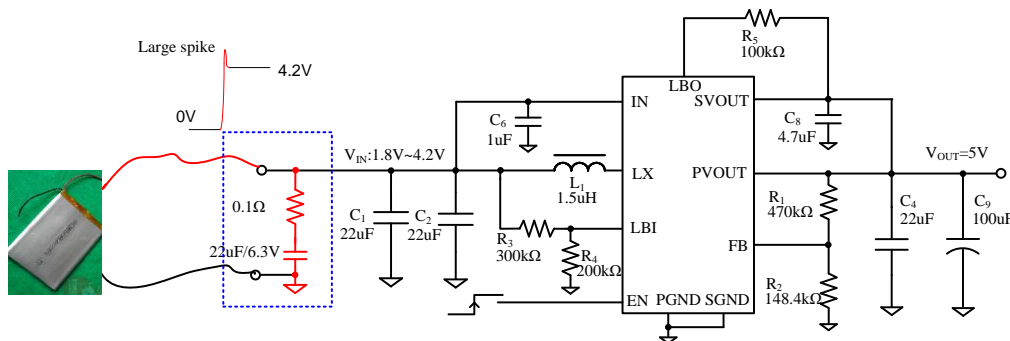
Input Capacitor C_{IN} :

The input capacitor is selected to handle the input ripple current requirements. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with $6.3V$ rating and greater than $22\mu F$ capacitance.

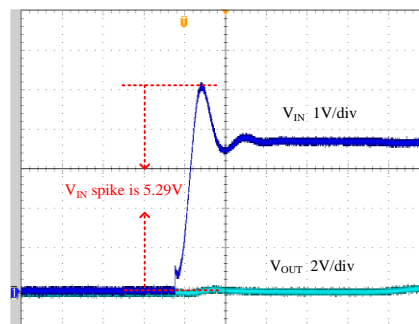
Li-Ion Battery Hot Plug Consideration:

In the mass production stage, the Li-ion battery will always hot plug in between the IN and the GND pin. The hot plug may lead to large voltage spike and even lead to the IC EOS fail. To avoid this potential risk, $1\ 22\mu F$ ceramic capacitor serial with a 0.1Ω resistor is recommended to absorb the input voltage spike.

With the recommended input absorb solution, the voltage spike can be reduced from $6.13V$ to $5.29V$.



Time (10us/div)
 $C_{IN}=22\mu F/6.3V*2$



Time (10us/div)
 $C_{IN}=22\mu F/6.3V*2 // (22\mu F+0.1\Omega)$

Inductor L Selection:

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}} \right)^2 \frac{(V_{OUT} - V_{IN})}{f_{SW} \times I_{OUT,MAX} \times 40\%} \quad (2)$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY7063 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

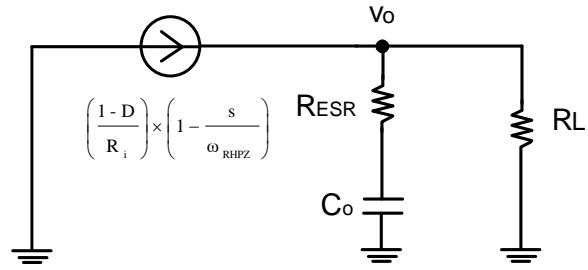
$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}} \right) \times I_{OUT,MAX} + \frac{V_{IN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L} \quad (3)$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR < 50mΩ to achieve a good overall efficiency.

Inductor vs. Output Capacitor:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. Care should be taken to minimize the loop area formed by C_{OUT} , and the OUT/GND pins. It's recommended to use an X5R or better grade ceramic capacitor with 10V rating and great than 22μF capacitance to decouple the high frequency current.

All continuous mode Boost converters have a right half plane zero (RHPZ) due to the inductor being removed from the output during charging. In a converter with current mode control, inner current feedback loop allows the switch, inductor and modulator to be lumped together into a small signal variable current source, shown as follows.



The power stage approximate transfer function is:

$$G_c(s) = \frac{(1-D) \times R_L}{R_i} \times \frac{\left(1 + \frac{s}{\omega_{ESR}}\right) \left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_p}} \quad (4)$$

Where

$$\omega_{ESR} = \frac{1}{R_{ESR} C_O} \quad (5)$$

$$\omega_p = \frac{1}{(R_{ESR} + R_L) \times C_O} \quad (6)$$

$$\omega_{RHPZ} = \frac{R_L}{L} \times \left(\frac{V_{IN}}{V_{OUT}} \right)^2 \quad (7)$$

As the equation 4 shows, the Boost convert with current mode control transfer function is consist of one ESR zero, one right half plane zero and one pole. Right half plane zero brings 20dB/decade gain increase, 90 degrees phase drop. So the bandwidth of the Boost converter MUST be lower than f_{RHPZ} .

As shown in equation 7, right half plane zero is depending on R_L , L and duty cycle. Larger inductor lead to lower f_{RHPZ} , so bandwidth should be designed lower than f_{RHPZ} .

Some low profile application may prefer to use the ceramic capacitor solution and some low cost application may use the Electrolytic capacitor to reduce the BOM cost.

Below is selection table based on different inductance and output capacitor.

Inductance vs. Output Capacitor Selection Table

Inductance		Capacitor	
Part Number	L(μH)	Part Number	C _{OUT} (μF)
SPM6530T-2R2M	2.2	C3216X5R1A226M	22μF/10V
SPM6530T-3R3M	3.3	C3216X5R1A226M	22μF/10V×2

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During the shutdown mode, the SY7063 shutdown current drops to lower than 1μA, driving the EN pin high (> 1.2V) will turn on the IC again.

Low Battery Detector Function-LBI/LBO

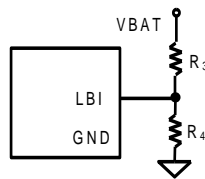
The low-battery detector function is used for monitoring the battery voltage and generating an error flag when the battery voltage drops below a user-set threshold voltage.

The function is active only when the device is enabled. When the device is disabled, LBO stays at high impedance. The detection threshold is 1.2V at LBI. During the normal operation, LBO stays at high impedance when the voltage applied at LBI is above the threshold. It is active low when the voltage at LBI goes below 1.2V.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 1.2V, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 20mV. If the low-battery detection circuit is not used, the LBI pin should be connected to the GND (or to the VBAT) and the LBO pin can be left unconnected. Do not leave the LBI pin floating.

R₃ and R₄ are designed to program the proper low battery threshold voltage. The voltage across R₄ is equal to the LBI voltage threshold that is generated on-chip, which has a value of 1.2V. The value of resistor R₃, depending on the desired minimum battery voltage VBAT, can be calculated as:

$$R_3 = \frac{V_{BAT} - 1.2V}{1.2V} R_4 \quad (8)$$



The output of the low battery monitor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on the LBI. The output requires a pull-up resistor with a recommended value of 100kΩ. The maximum voltage which is used for pulling up the LBO outputs should not exceed the output voltage of the DC/DC converter. If not used, the LBO pin can be left floating or tied to the GND.

Layout Design Consideration:

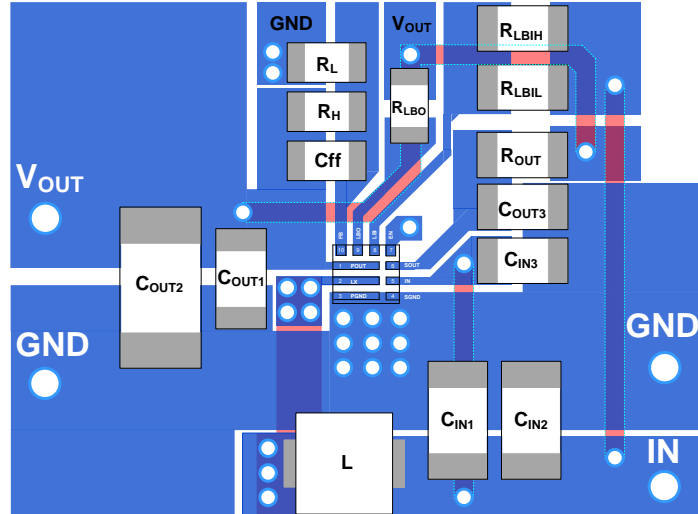
For the best efficiency and minimum noise problems, the following components should be placed close to the IC: C_{IN}, C_{OUT}, L, R₁ and R₂.

- 1) It is desirable to maximize the PCB copper area connecting to the PGND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly recommended.
- 2) C_{OUT} must be close with the pins P_{VOUT} and PGND. The loop area formed by C_{OUT} and the GND must be minimized.
- 3) To minimize the output decouple loop area, the LX trace is recommended to be routed on bottom or middle layer through via.
- 4) S_{VOUT} is the power supply pin for the internal control circuit. Don't connect to the P_{VOUT} pin directly. A 4.7μF ceramic capacitor is strongly recommended to decouple the S_{VOUT} pin to the SGND pin. Please use a jump wire to connect the S_{VOUT} pin to output capacitor side.
- 5) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.
- 6) The components R₁ and R₂ and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

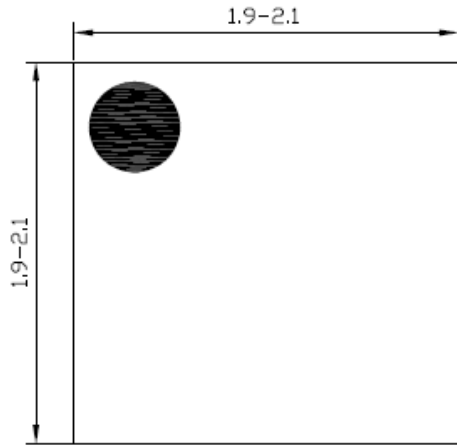


PCB Layout Suggestion

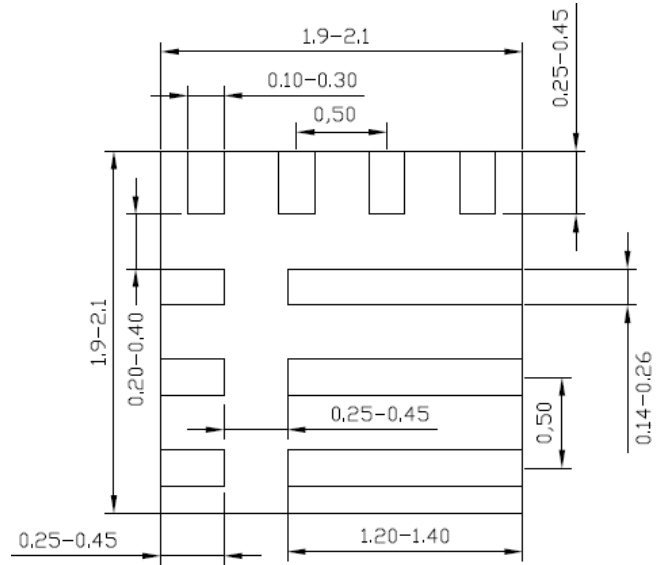
FB	LBO	LBI	EN
10	9	8	7
1	PVOUT		6
2	LX		5
3	PGND		4
			3
			2
			1
			0
			SVOUT
			IN
			SGND



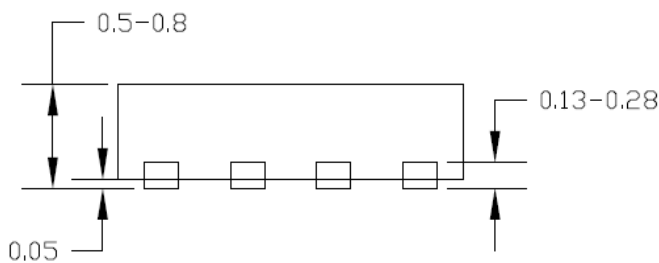
QFN2×2-10 Package Outline



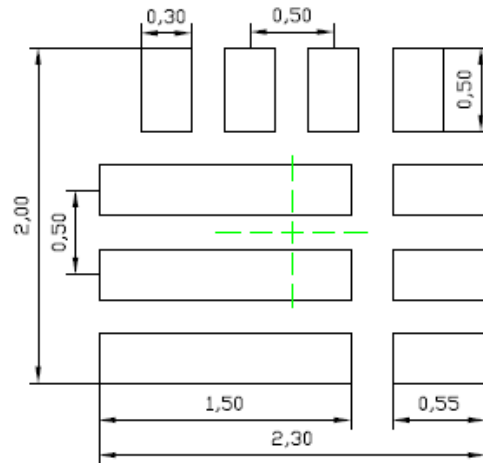
Top View



Bottom View



Side View



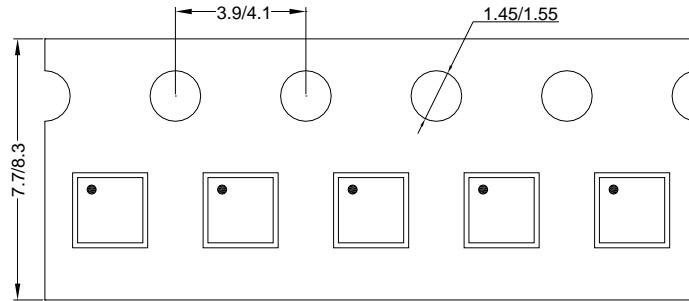
**Recommended PCB Layout
(Reference only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

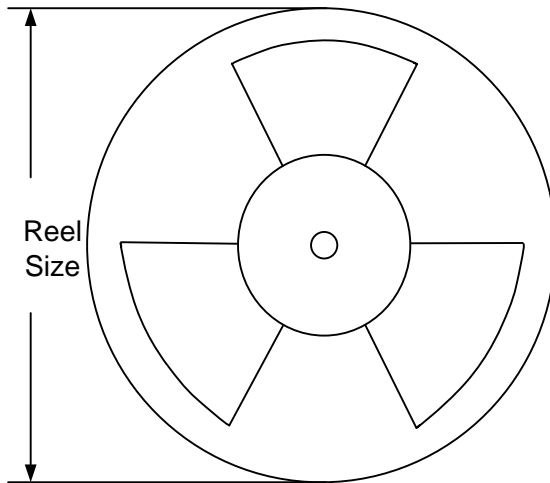
1. Taping orientation

QFN2×2



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2×2	8	4	7"	400	160	3000

3. Others: NA

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