SY6045B

High Performance, High Fidelity 20W Digital Audio-Power Amplifier

General Description

The SY6045B is a 2×20W, digital audio power amplifier for driving bridge-tied stereo speakers. One serial data input allows processing of up to two discrete audio channels and seamless integration to most digital audio processors. SY6045B is an I^2S slave device receiving all clocks from external sources.

The SY6045B has a mixer and Bi-Quad filters which can be used to accomplish essential audio signal processing functions like dynamic range control, loudness control, and parametric equalization.

Ordering Information

SY6045 □(□□)□
- └ Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6045BQHC	QFN6×6-40	

Applications

- LCD TV, LED TV or Monitor
- Digital Speaker, Bluetooth Speaker
- Sound bar

Features

- 2CH Stereo(20W×2BTL)
- 2.0 BTL Mode or PBTL Mode
- Support 4.5V to 28V PVDD Range
- 32bit Fixed-point DSP
- 32kHz to 96kHz Sample Rate Support (LJ/RJ/I^2S)
- I^2C Address Selection Pin
- Independent Channel Volume Controls with 48dB to Mute
- SDATA Generator (I^2S output)
- Two DC Blocking Filters
- 18 PEQs or 12 PEQs + 6 SPEQs each channel for Speaker Protection and Speaker Compensation
- 3 Bands Dynamic Range Control plus a Post Dynamic Range Control
- Four Types of Digital Filters with Different Roll-off
- Loudness Control
- Hard Clipper
- Power Level Meter
- 3-wire I^2S Digital Audio Interface without MCLK
- Thermal, Over-Current, Short-Circuit Protection and BQ/DRC Checksum
- Support Automatic Audio Sample Rate Detection

Typical Application

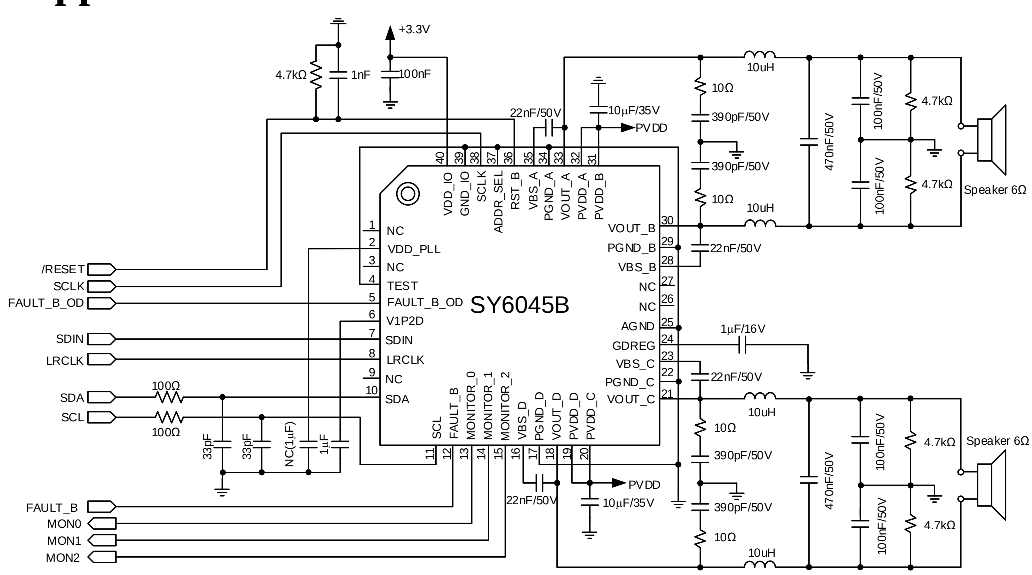
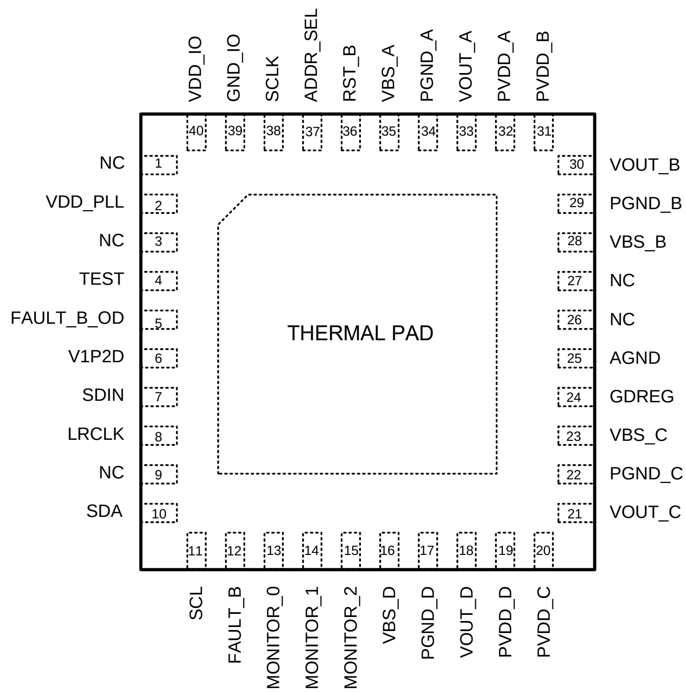


Figure 1. Typical Application Circuit

Pinout (top view)



(QFN6×6-40)

Top mark: **DNT** ***xyz*** (Device code: **DNT**, ***x=year code, y=week code, z= lot number code***)

Pin Name	**Pin Number**	**Type(1)**	**Termination(2)**	**Description**
VOUT_A	33	O		Half-bridge A output.
VOUT_B	30	O		Half-bridge B output.
VOUT_C	21	O		Half-bridge C output.
VOUT_D	18	O		Half-bridge D output.
PVDD_A	32	P		Power supply for half-bridge A.
PVDD_B	31	P		Power supply for half-bridge B.
PVDD_C	20	P		Power supply for half-bridge C.
PVDD_D	19	P		Power supply for half-bridge D.
VBS_A	35	P		High side supply offset voltage for half-bridge A.
VBS_B	28	P		High side supply offset voltage for half-bridge B.
VBS_C	23	P		High side supply offset voltage for half-bridge C.
VBS_D	16	P		High side supply offset voltage for half-bridge D
GDREG	24	P		Gate driver internal regulator output. This pin must not be used to drive external devices.
GND_IO	39	P		Analog 3.3V power supply ground.
NC	1,3,9,26,27			No Connection.
VDD_IO	40	P		3.3V analog power supply.
ADDR_SEL	37	DI	Pull down	I^2C address selection pin.
V1P2D	6	P		Internal regulated 1.2V digital power supply for digital core. This pin must not be used to power external devices.

VDD_PLL	2	P		Internal regulated 1.2V digital power supply for PLL. This pin must not be used to power external devices.
FAULT_B	12	DI	Pull up	Pull this pin low to turn off the PWM signal path.
FAULT_B_OD	5	DO	Pull up	Output internal power-stage errors.
LRCLK	8	DI	Pull down	Serial audio data left or right clock input.
SCLK	38	DI	Pull down	Serial audio data bit clock input.
SDIN	7	DI	Pull down	Serial audio data input.
SDA	10	DIO	Pull up	I^2C serial data input or output.
SCL	11	DI	Pull up	I^2C serial clock input.
MONITOR_0	13	DO	Pull down	Monitoring signal out from processor block / I2S output.
MONITOR_1	14	DO	Pull down	Monitoring signal out from processor block / I2S output.
MONITOR_2	15	DO	Pull down	Monitoring signal out from processor block / I2S output.
RST_B	36	DI	Pull up	Logic low to this pin to reset the system. When reset is pulled low, DAP restores to its default conditions, and places the PWM in the hard mute state.
TEST	4	DI	Pull down	Test pin.
AGND	25	P		Power stage analog ground.
PGND_A	34	P		Power ground for half-bridge A.
PGND_B	29	P		Power ground for half-bridge B.
PGND_C	22	P		Power ground for half-bridge C.
PGND_D	17	P		Power ground for half-bridge D.

Note: (1) Type: A =analog; D =digital; P =power/ground/decoupling; I =input; O =output; IO=inout
(2) All pull-ups and pull-downs are weak.

Block Diagram

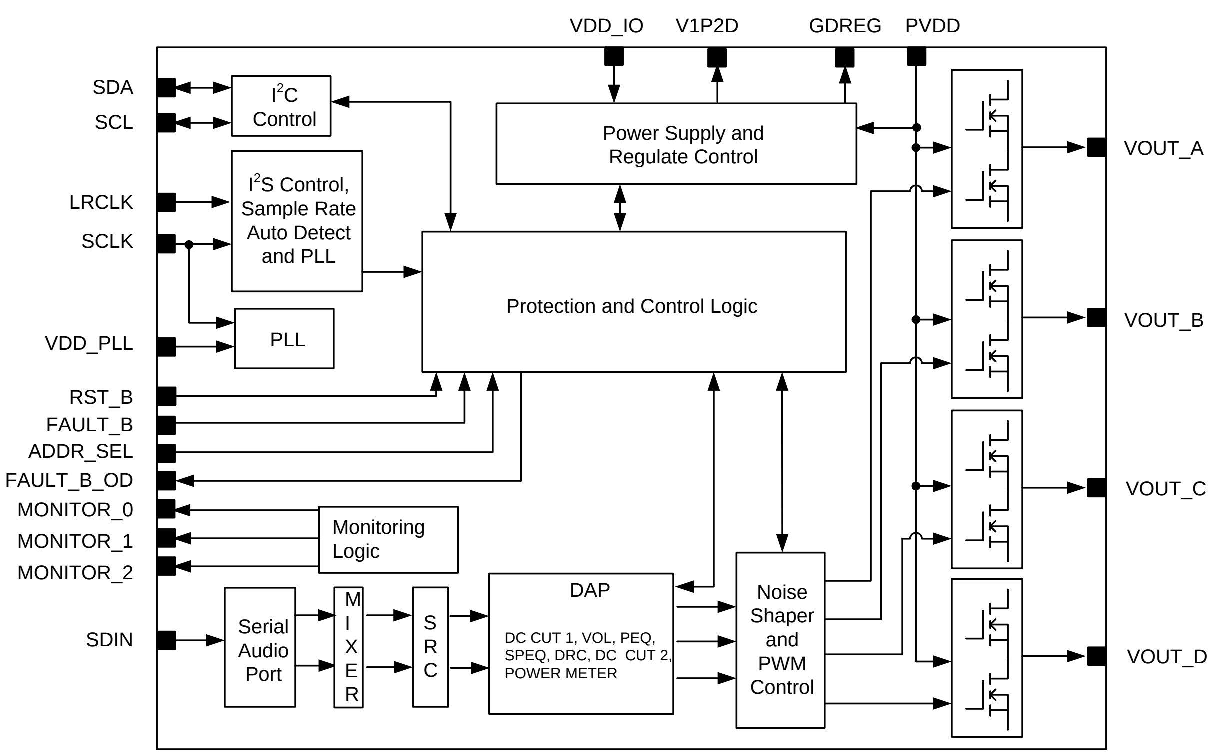


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

VDD_IO, Power Supply for Digital Interface I/O -- -0.3V to 4.5V
PVDD, Half-bridge Supply Voltage (Note 2) -- -0.3V to 30V
Digital Input -- -0.5V to (VDD_IO+0.5) V
VOUT_x -- 30V
GDREG --- -0.5V to 4V
VBS_x to VOUT_x -- -0.5V to 4V
Package Thermal Resistance (Note 3)

θ_{JA} --- 23°C/W
θ_{JC} (top) -- 13.5°C/W
θ_{JC} (bottom) --- 2°C/W
θ_{JB} --- 10.5°C/W
ψ_{JT} -- 0.9°C/W

Junction Temperature Range -- -10°C to 150°C
Storage Temperature Range -- -40°C to 125°C

Recommended Operating Conditions

VDD_IO, Power Supply for Digital Interface I/O -- 3.3V
PVDD, Half-bridge Supply Voltage --- 4.5V to 28V
$R_{L(BTL)}$, Load Impedance(BTL) --- 8Ω
$R_{L(PBTL)}$, Load Impedance(PBTL) -- 4Ω
Operating Ambient Temperature Range --- -10°C to 85°C
Operating Junction Temperature Range -- -10°C to 125°C

PWM Operation Conditions

Parameter	Test Conditions	Value	Unit
Output Sample Rate	44.1kHz data rate	352.8	kHz
	32/48/96kHz data rate	384	

Electrical Characteristics

DC Characteristics(Note 4)

(T_A=25°C, PVDD_x=18V, VDD_IO=3.3V, R_L=8Ω, BTL Ternary Mode, f_S=48 kHz, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PVDD	Half-bridge Supply Voltage		4.5		28	V
VDD_IO	Power supply for digital interface I/O		3		3.6	V
GDREG	Gate Drive Supply		3.1	3.3	3.5	V
V_{IH}	High Level Input Voltage	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK	2			V
V_{IL}	Low Level Input Voltage	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			0.8	V
I_{IL}	Low Level Input Current	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			75	μA
I_{IH}	High Level Input Current	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			75	μA
I_{VDD_IO}	Digital Supply Current	Normal (No Input, No Load)		8		mA
		Reset (RST_B=low, FAULT_B=high)		1.6	2.3	
I_{PVDD}	Power Supply Current	Normal (No Input, No Load)		27		mA
		Reset (RST_B=low, FAULT_B=high)		0.6	1.5	
Power MOSFET						
$R_{DS(on)}$	High Side Drain-to-source Resistance	T_j=25°C, includes metallization resistance		125		mΩ
	Low Side Drain-to-source Resistance			125		mΩ
I/O Protection						
V_{UVP}	PVDD Falling		3	3.6		V
	PVDD Rising			4.0	4.45	
OVTP(Note 4)	Over Temperature Protection			150		°C
$OVTP_{HYST}$ (Note 4)	Over Temperature Protection Hysteresis			30		°C
I_{OVC}(Note 4)	Over Current Protection			5		A

AC Characteristics(Note4)

(T_A=25°C, BTL ternary mode, f_S=48 kHz, C_{VBS}=22nF, audio frequency=1 kHz, AES17 filter, snubber=3.3Ω+390pF, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_O	Output Power	BTL Mode, PVDD=12V, R_L=8Ω, 1%THD+N		7.5		W
		BTL Mode, PVDD=12V, R_L =8Ω, 10%THD+N		9.3		
		BTL Mode, PVDD=12V, R_L=6Ω, 1%THD+N		9.4		
		BTL Mode, PVDD=12V, R_L=6Ω, 10%THD+N		11.6		
		BTL Mode, PVDD=13.2V, R_L=6Ω, 1%THD+N		11.3		
		BTL Mode, PVDD=13.2V, R_L=6Ω,10%THD+N		13.9		
		BTL Mode, PVDD=18V, R_L=8Ω, 1%THD+N		17		
		BTL Mode, PVDD=18V, R_L=8Ω, 10%THD+N		20.9		
		BTL Mode, PVDD=18V, R_L=6Ω, 1%THD+N		20.8		
		BTL Mode, PVDD=18V, R_L=6Ω, 10%THD+N		25.6		
		BTL Mode, PVDD=24V, R_L=8Ω, 1%THD+N		29.8		

		BTL Mode, PVDD=24V, R_L=8Ω, 10%THD+N		36.7		
		PBTL Mode, PVDD=12V, R_L=4Ω,1%THD+N		14.7		
		PBTL Mode, PVDD=12V, R_L=4Ω,10%THD+N		18.3		
		PBTL Mode, PVDD=18V, R_L=4Ω,1%THD+N		32.8		
		PBTL Mode, PVDD=24V, R_L=4Ω,1%THD+N		57.4		
THD+N	Total Harmonic Distortion and Noise	PVDD=12V , R_L=8Ω , P_O=1W		0.032		%
		PVDD=13.2V , R_L=6Ω , P_O=1W		0.066		
		PVDD=18V , R_L=8Ω , P_O=1W		0.041		
		PVDD=20V , R_L=6Ω , P_O=1W		0.069		
		PVDD=24V , R_L=8Ω , P_O=1W		0.027		
V_n	Output Integrated Noise (rms)	PVDD=12V , R_L=8Ω , A-weighted		59		μV
		PVDD=13.2V , R_L=6Ω , A-weighted		66		
		PVDD=18V, R_L=8Ω, A-weighted		94		
		PVDD=20V , R_L=6Ω , A-weighted		105		
		PVDD=24V, R_L=8Ω, A-weighted		112		
CT	Crosstalk	PVDD=20V, P_o=1W , f =1kHz		85		dB
SNR	Signal to Noise Ratio	PVDD=12V , R_L=8Ω , f=1kHz, Maximum power at THD+N <1%,		101		dB
		PVDD=13.2V , R_L=8Ω , f=1kHz, Maximum power at THD+N <1%,		101		
		PVDD=18V , R_L=8Ω , f=1kHz, Maximum power at THD+N <1%,		101		
		PVDD=24V , R_L=8Ω , f=1kHz, Maximum power at THD+N <1%,		101		

Note 1: Stresses beyond the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: DC voltage rating could be derated a little according to the possible switching spike on switching node if the snubber is not appropriate enough.

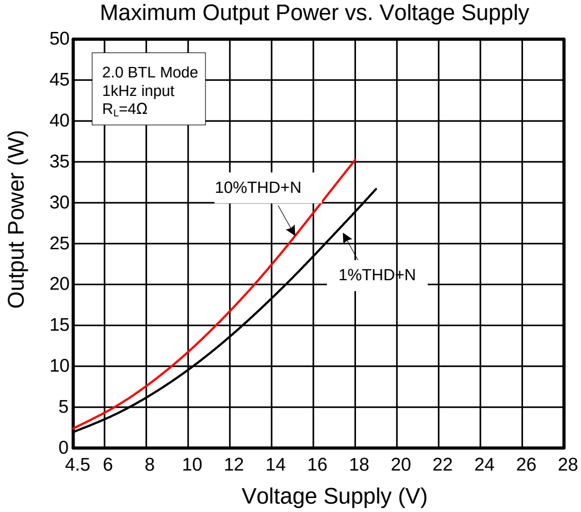
Note 3: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layer thermal conductivity test board with thermal vias in accordance with JESD51-5,-7, other thermal resistance data acquired followed JESD51-8,-14.

Note 4: Typical value tested on demonstration board is guaranteed by design.

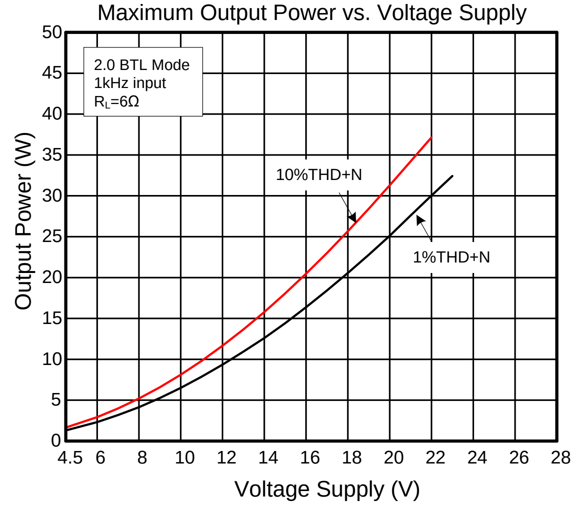
Typical Performance Characteristics

(All measurements with snubber = 3.3Ω+390pF.)

Maximum Output Power vs. Voltage Supply



Maximum Output Power vs. Voltage Supply



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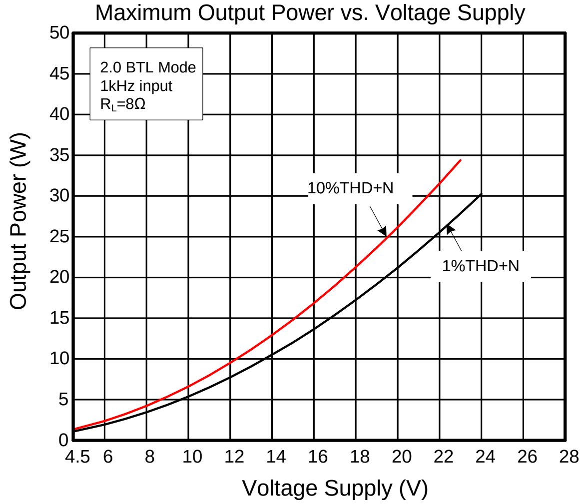
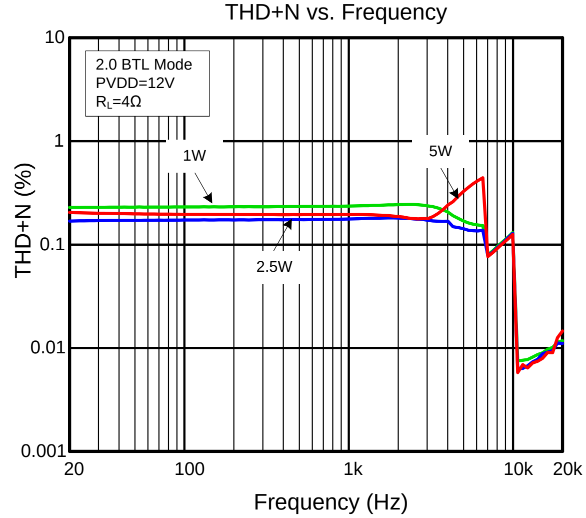


THD+N vs. Frequency



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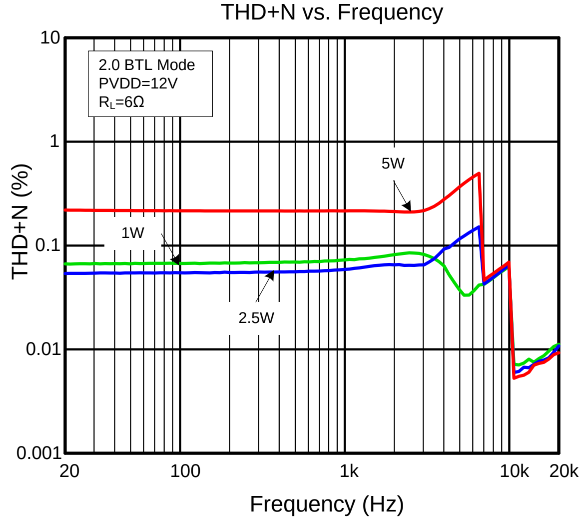

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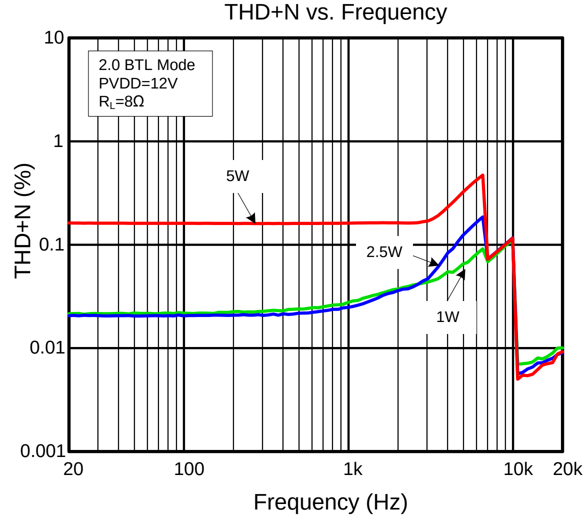

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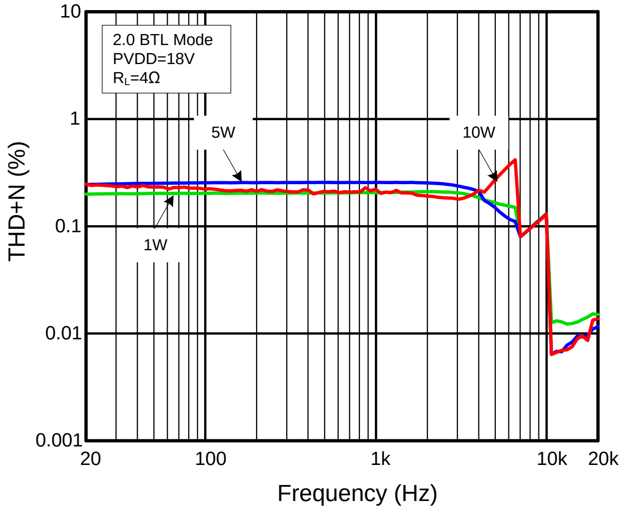
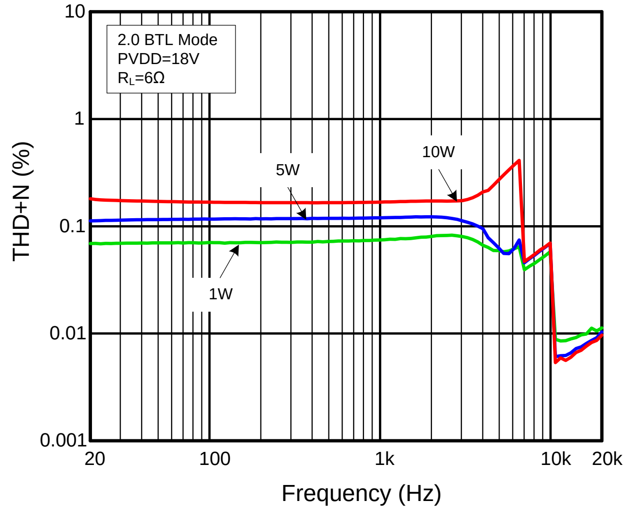
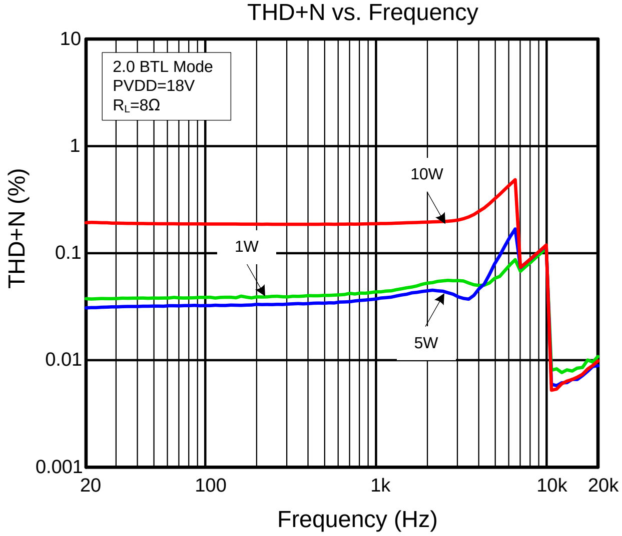


THD+N vs. Frequency



THD+N vs. Frequency



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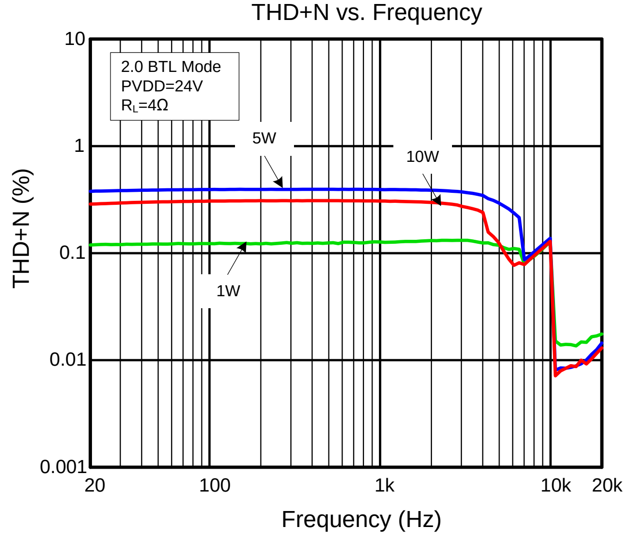

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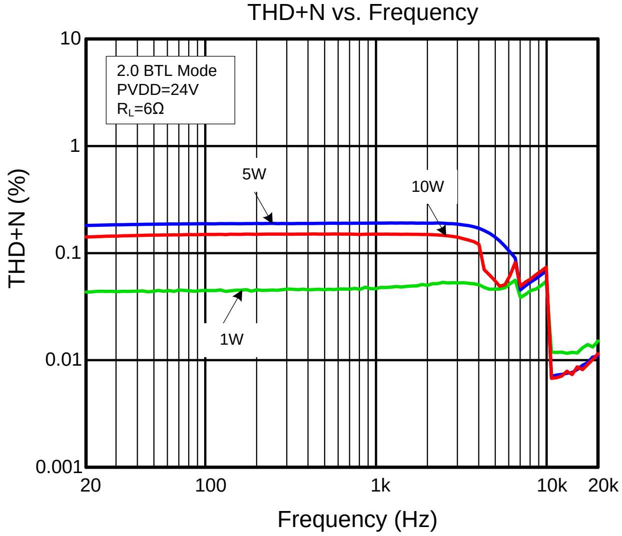
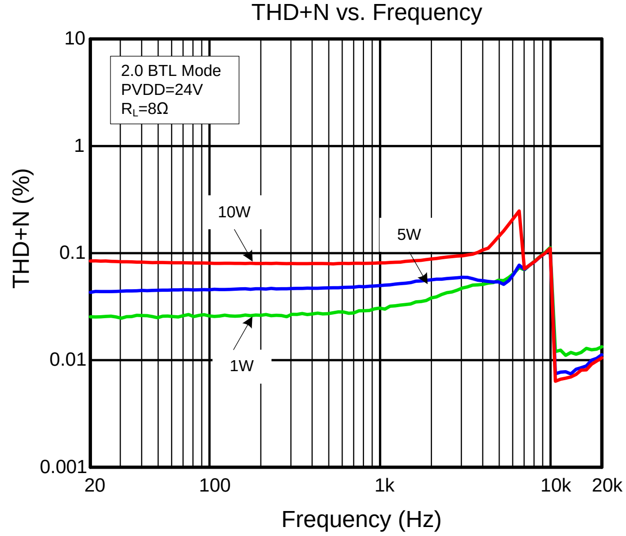
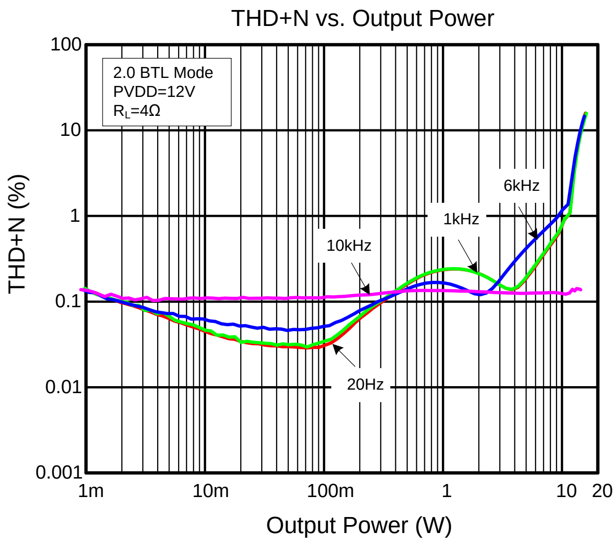
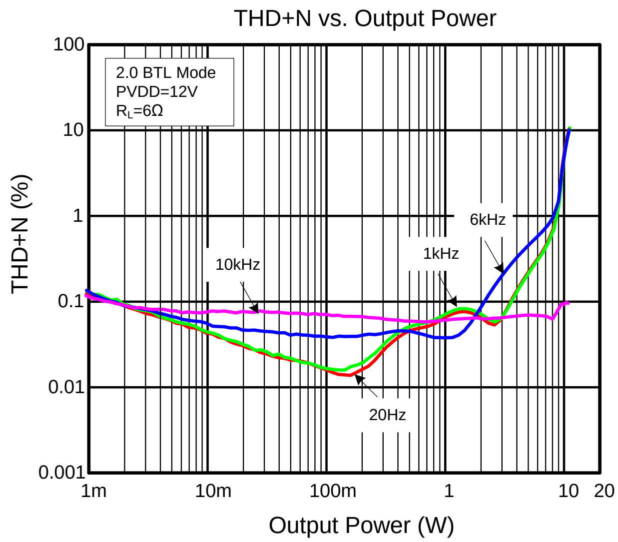


THD+N vs. Frequency




THD+N vs. Output Power
2.0 BTL Mode
PVDD=12V
R_L=4Ω
THD+N (%)
Output Power (W)
100
10
1
0.1
0.01
0.001
1m
10m
100m
1
10
20
6kHz
1kHz
10kHz
20Hz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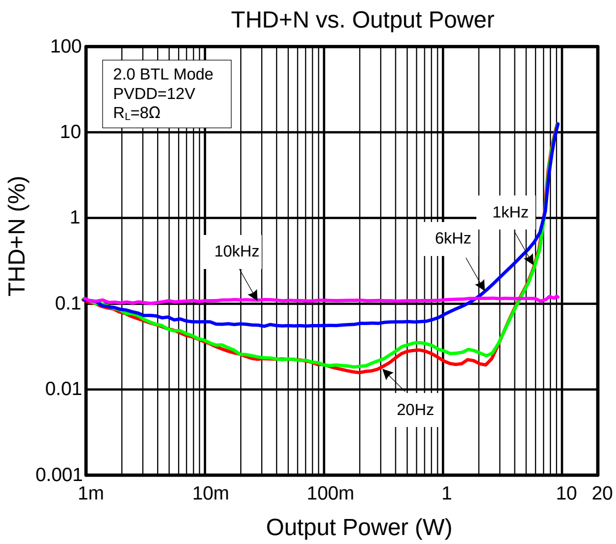
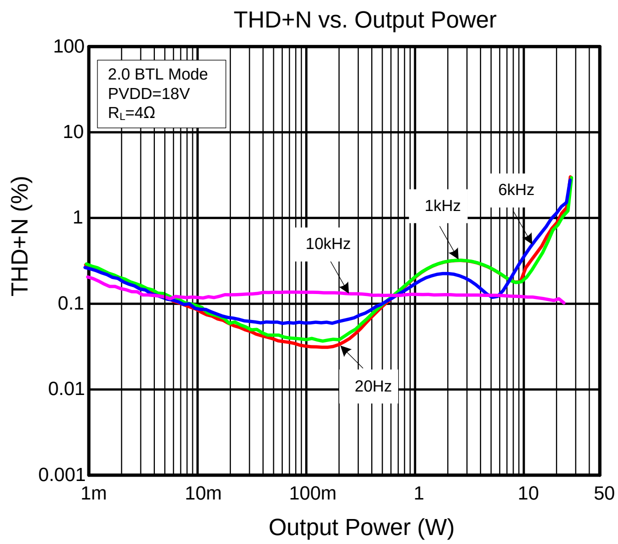
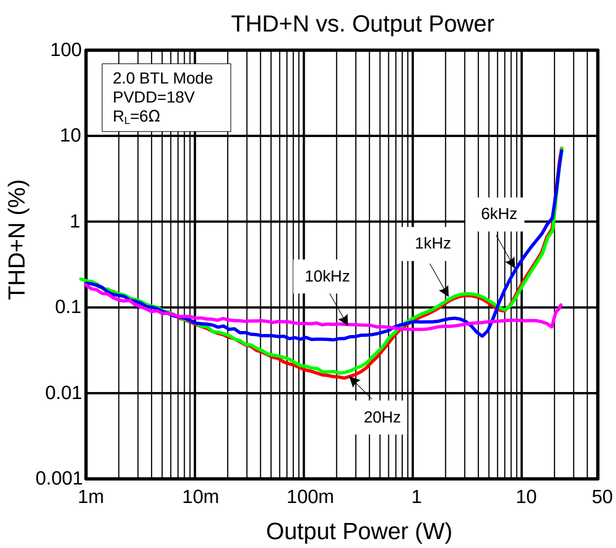
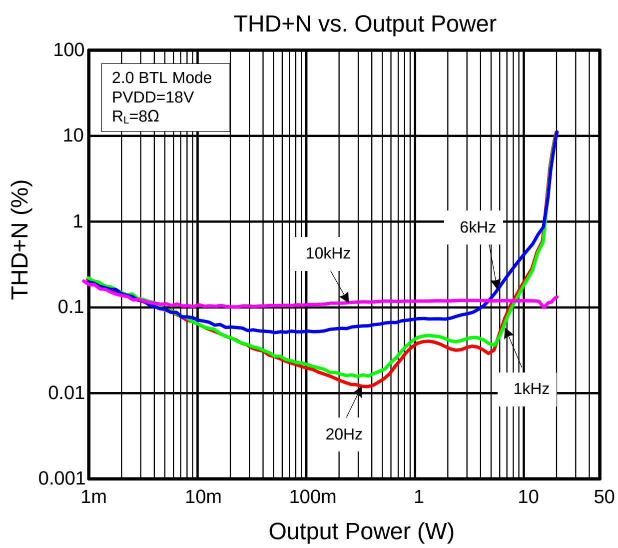
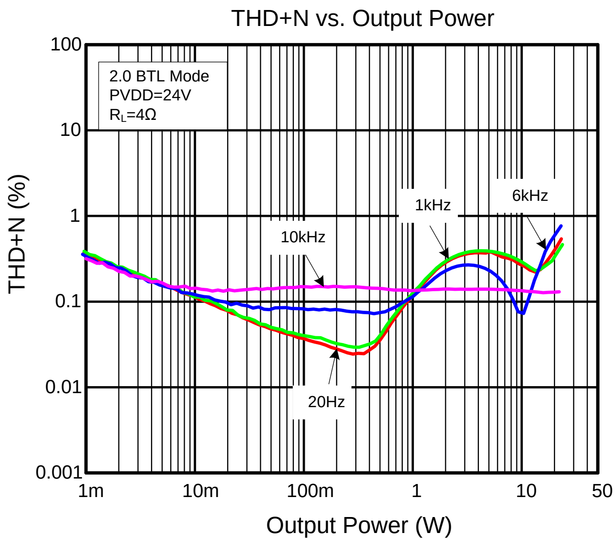
PVDD=12V
R_L=6Ω
THD+N (%)
Output Power (W)
100
10
1
0.1
0.01
0.001
1m
10m
100m
1
10
20
6kHz
1kHz
10kHz
20Hz

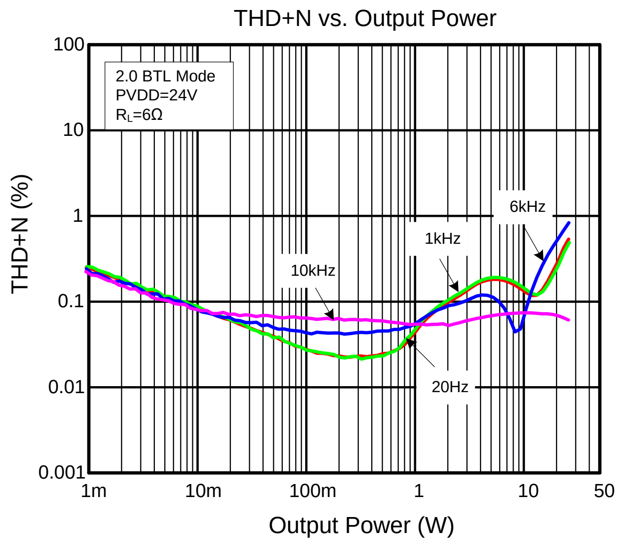

THD+N vs. Output Power
2.0 BTL Mode
PVDD=12V
R_L=8Ω
THD+N (%)
Output Power (W)
100
10
1
0.1
0.01
0.001
1m
10m
100m
1
10
20
1kHz
6kHz
10kHz
20Hz

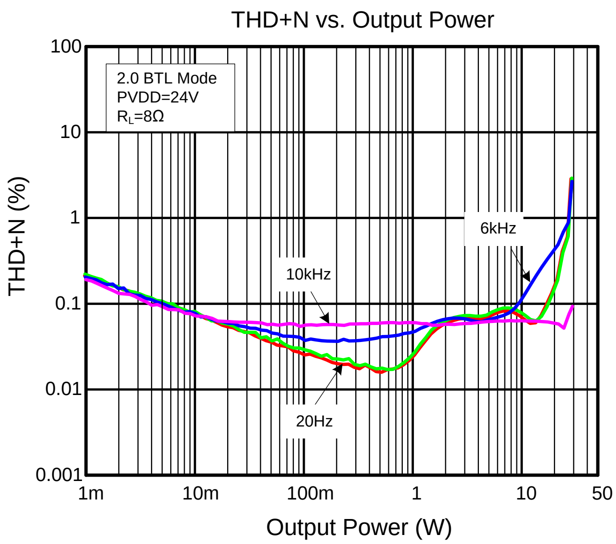

THD+N vs. Output Power
2.0 BTL Mode
PVDD=18V
R_L=4Ω
THD+N (%)
Output Power (W)
100
10
1
0.1
0.01
0.001
1m
10m
100m
1
10
50
6kHz
1kHz
10kHz
20Hz

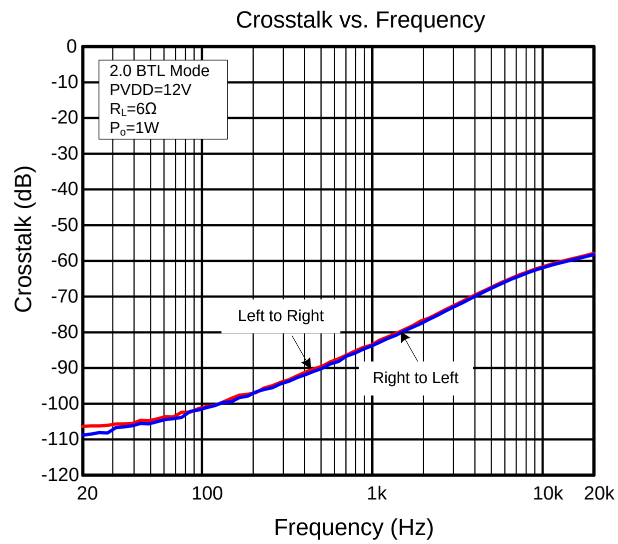

THD+N vs. Output Power
2.0 BTL Mode
PVDD=18V
R_L=6Ω
THD+N (%)
Output Power (W)
100
10
1
0.1
0.01
0.001
1m
10m
100m
1
10
50
6kHz
1kHz
10kHz
20Hz

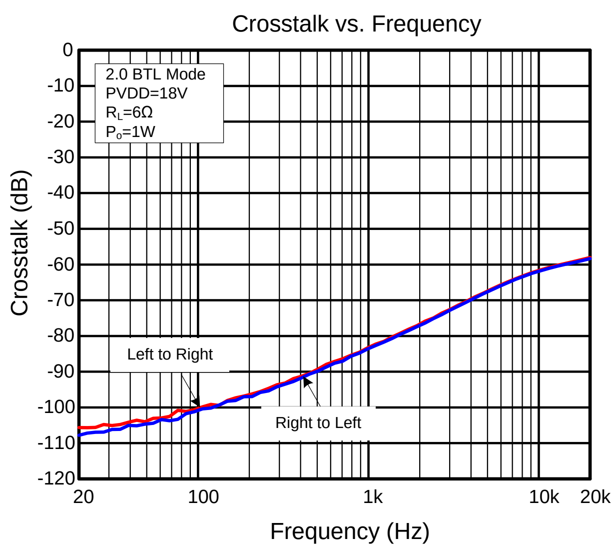

THD+N vs. Output Power
2.0 BTL Mode
PVDD=18V
R_L=8Ω
THD+N (%)
Output Power (W)
100
10
1
0.1
0.01
0.001
1m
10m
100m
1
10
50
6kHz
10kHz
1kHz
20Hz

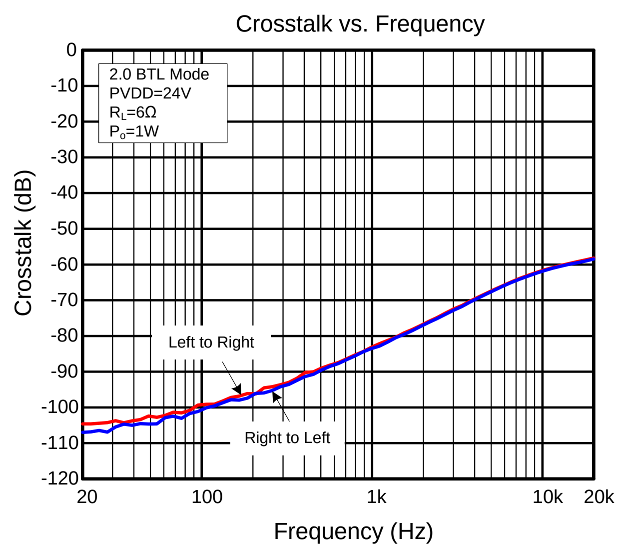

THD+N vs. Output Power
2.0 BTL Mode
PVDD=24V
R_L=4Ω
THD+N (%)
100
10
1
0.1
0.01
0.001
1m
10m
100m
1
10
50
Output Power (W)
1kHz
6kHz
10kHz
20Hz

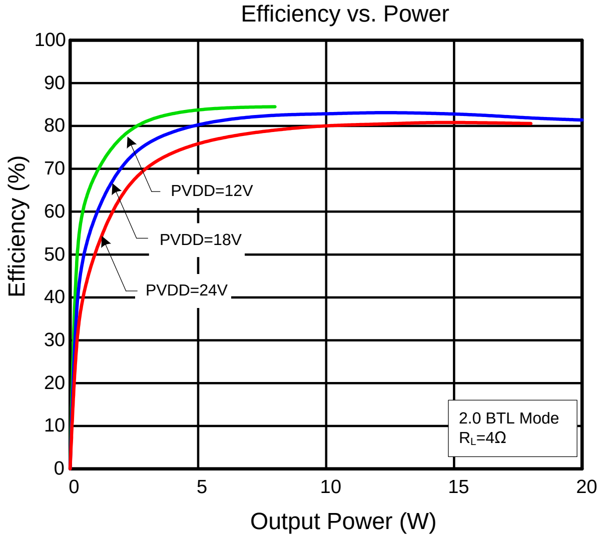

THD+N vs. Output Power
2.0 BTL Mode
PVDD=24V
R_L=6Ω
THD+N (%)
100
10
1
0.1
0.01
0.001
1m
10m
100m
1
10
50
Output Power (W)
6kHz
1kHz
10kHz
20Hz

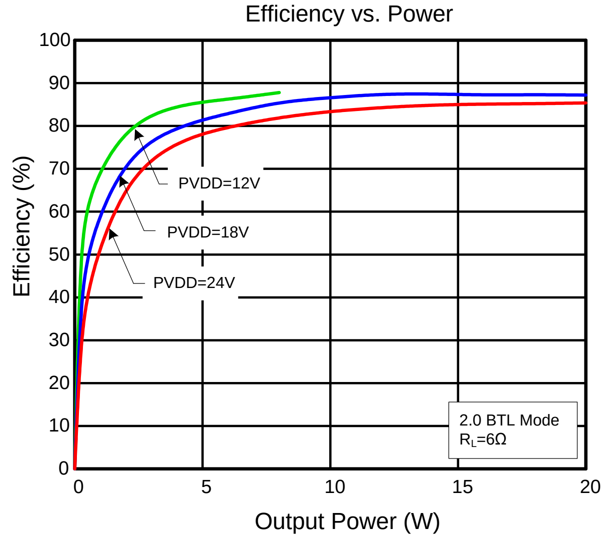

THD+N vs. Output Power
2.0 BTL Mode
PVDD=24V
R_L=8Ω
THD+N (%)
100
10
1
0.1
0.01
0.001
1m
10m
100m
1
10
50
Output Power (W)
6kHz
10kHz
20Hz

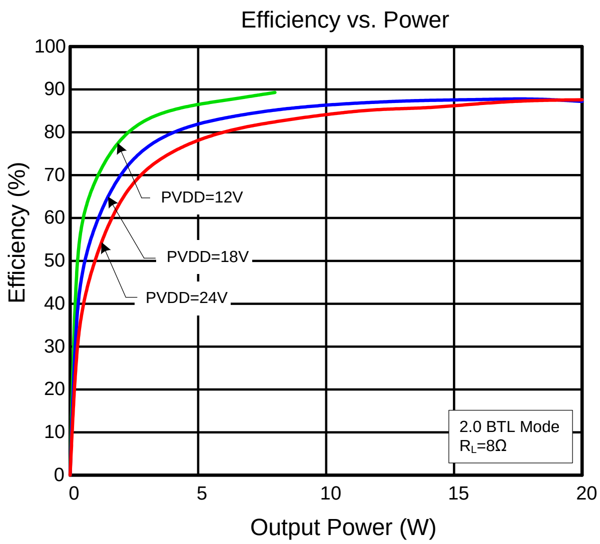

Crosstalk vs. Frequency
2.0 BTL Mode
PVDD=12V
R_L=6Ω
P_o=1W
Crosstalk (dB)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
20
100
1k
10k
20k
Frequency (Hz)
Left to Right
Right to Left


Crosstalk vs. Frequency
2.0 BTL Mode
PVDD=18V
R_L=6Ω
P_o=1W
Crosstalk (dB)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
20
100
1k
10k
20k
Frequency (Hz)
Left to Right
Right to Left


Crosstalk vs. Frequency
2.0 BTL Mode
PVDD=24V
R_L=6Ω
P_o=1W
Crosstalk (dB)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
20
100
1k
10k
20k
Frequency (Hz)
Left to Right
Right to Left


Efficiency vs. Power
Efficiency (%)
Output Power (W)
PVDD=12V
PVDD=18V
PVDD=24V
2.0 BTL Mode
RL=4Ω


Efficiency vs. Power
Efficiency (%)
Output Power (W)
PVDD=12V
PVDD=18V
PVDD=24V
2.0 BTL Mode
RL=6Ω


Efficiency vs. Power
Efficiency (%)
Output Power (W)
PVDD=12V
PVDD=18V
PVDD=24V
2.0 BTL Mode
RL=8Ω

I²C Serial Control Port Operation

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL frequency	No wait states		400	kHz
t_r	SCL and SDA rise time			300	ns
t_f	SCL and SDA fall time			300	ns
t_{WH}	SCL high duration time		0.6		µs
t_{WL}	SCL low duration time		1.3		µs
t_{S1}	SDA to SCL setup time		100		ns
t_{h1}	SCL to SDA hold time		0		ns
t_{buf}	Free time between stop and start condition		1.3		µs
t_{S2}	SCL to start condition		0.6		µs
t_{h2}	Start condition to SCL hold time		0.6		µs
t_{S3}	SCL to stop condition		0.6		µs
C_{Load}	Load capacitor for each bus line			400	pF

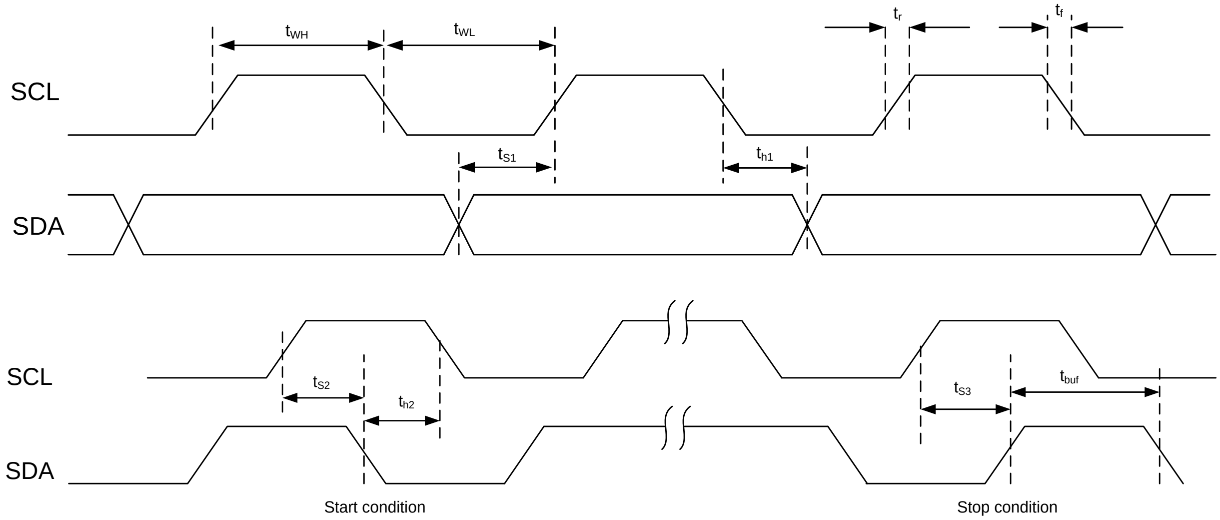


Figure 3. I²C Timing Diagram

Reset Timing (RST_B)

Symbol	Parameter	Min	Typ	Max	Unit
t_{WRST}	RESET active pulse duration	100			µs
t_{delay_I2C}	Enable I²C duration time			0.1	ms

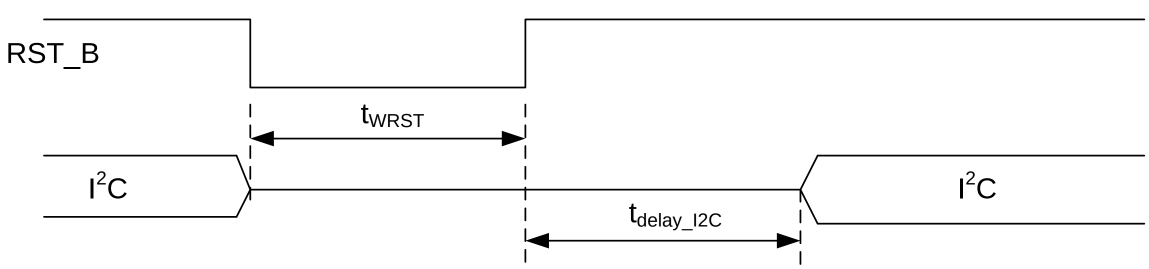


Figure 4. Reset Timing Diagram

Notes: 1. RST_B is held low for at least 100 us after VDD_IO has reached 3V on power up.

Serial Audio Ports Slave Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency	C_{load}=30pF	2.048		6.144	MHz
t_{S4}	LRCLK to SCLK rising edge setup time		10			ns
t_{h3}	LRCLK FROM SCLK rising edge hold time		10			ns
t_{S5}	SDIN to SCLK rising edge setup time		10			ns
t_{h4}	SDIN from SCLK rising tome hold time		10			ns
f_{LRCLK}	LRCLK frequency		32	48	96	kHz
	SCLK duty cycle		40%	50%	60%	
	LRCLK duty cycle		40%	50%	60%	
t_{edge}	LRCLK edge with respect to the falling edge of SCLK		-1/4		1/4	SCLK period
t_{rs}/t_{fs} (Note 1)	Rise/fall time for SCLK/LRCLK				1/8	SCLK period

Note 1: Rise time refers to the time it takes for the leading edge of a pulse to rise from its minimum to its maximum value. Rise time is typically measured from 10% to 90% of the value. Conversely, for fall time.

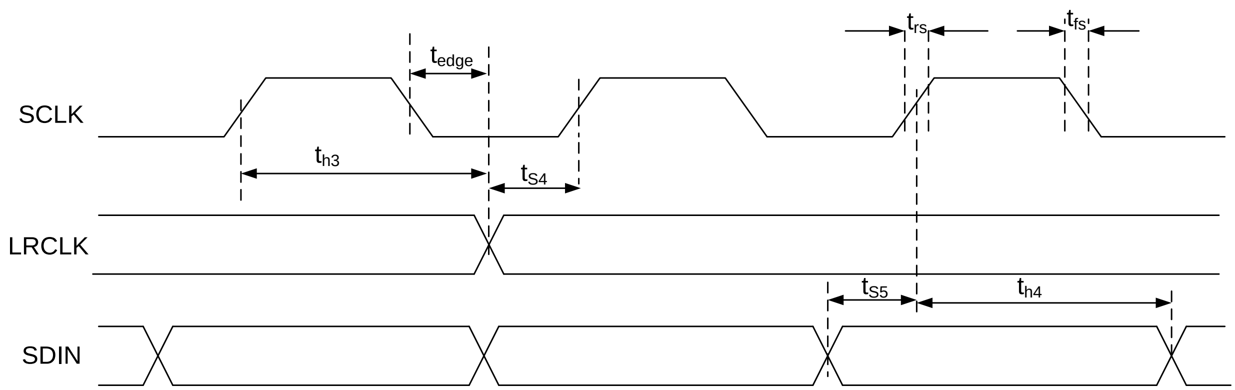


Figure 5. I²S Timing Diagram

Detailed Description and Theory of Operation

Under Voltage Protection and Power on Reset

When power on, the Power on Reset circuit resets the overload circuit and ensures that all circuits are fully operational when PVDD and AVDD supply voltage reach 4.0V and 2.7V respectively. A voltage drops below the UVP threshold on AVDD or PVDD results in all half bridge outputs being set in the high impedance state, and the FAULT_B_OD being set to low.

Clock, Auto Detection and PLL

This device is a slave only device. The digital audio processor supports all the sample rates and SCLK rates that are defined in the clock control register.

The DAP only supports a 1fs LRCLK. The clock section uses SCLK or the internal oscillator clock (when SCLK is unstable, out of range, or absent) to produce the internal clock running at 512 times the PWM switching frequency. The sample rate can be set by external MCU as well as auto-detected by the DAP. If bit 4 of register 0x00 is set to 1, the sample rate should be configured by MCU. 32kHz, 44.1kHz/48kHz and 96kHz can be set by programming Bit[3:2] of register 0x00. If bit 4 of register 0x00 is set to 0, the DAP can auto detect the sample rate. The detected sample rate can be read back from the bit[7:6] of register 0x00. For example, if the sample rate is changed from 48kHz to 96kHz, the setting of PLL will be auto configured and the DAP clock and PWM frequency keeps no change.

The device has robust clock error handing that uses the built-in trimmed oscillator clock to quickly detect changes or errors. Once the system detects a clock change or error, it will mute the audio and then force PLL to limp using the internal oscillator as a reference clock. Once the clock is stable, the system will revert to normal operation. During this operation, the default volume will be restored in a single step (also called hard unmute). The ramp process can be programmed to ramp back slowly (also called soft unmute) as defined in volume register (0x06).

Serial Data Interface

Serial data is input on SDIN. The PWM outputs are derived from SDIN. The DAP accepts serial data in 16, 18, 20, or 24bit left justified, right justified, and I^2S serial data formats.

PWM Section

The device PWM section accepts 24bit PCM data from DAP and output two BTL PWM audio output channels. The PWM section has an adjustable maximum modulation limit of 96.1% to 98.2%.

Serial Interface Control and Timing

The I^2S mode is set by writing to register 0x15.

I^2S Timing

I^2S uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A clock running at $32f_s/48f_s/64f_s$ is used to clock in data. There is a delay of one bit clock from the time the LRCLK changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of clock. The DAP masks unused trailing data bit positions.

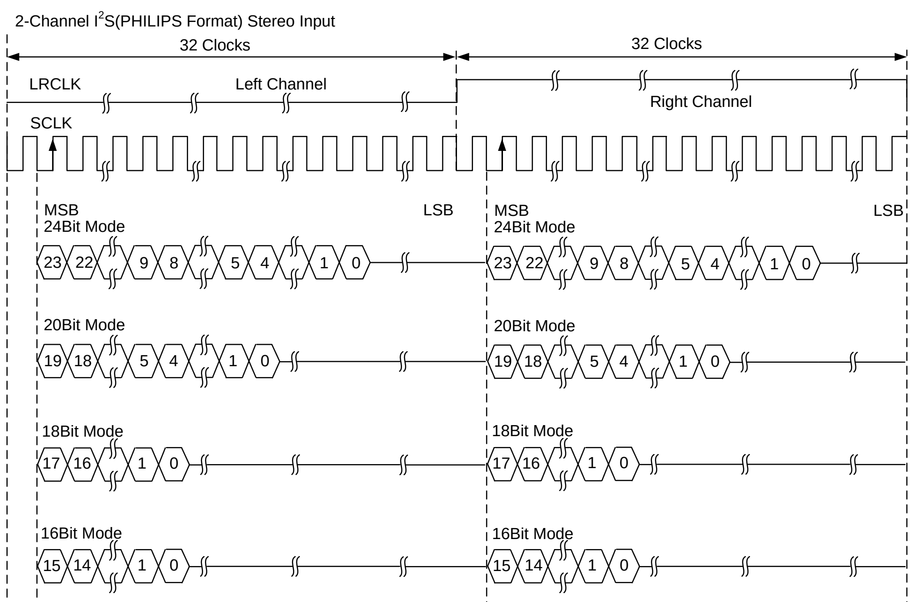


Figure 6. I^2S $64f_s$ Format

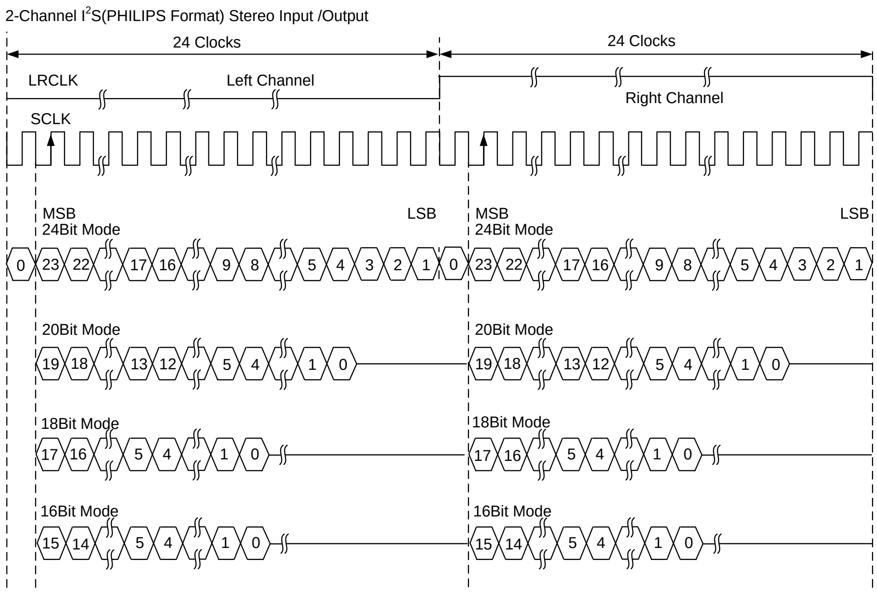


Figure 7. I^2S 48f_s Format

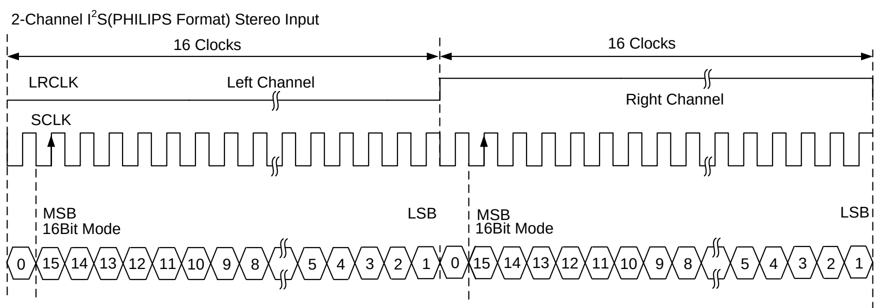


Figure 8. I^2S 32f_s Format

Left Justified

Left Justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A clock running at $32f_s/48f_s/64f_s$ is used to clock in data. The first bit of data on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of clock. The DAP masks unused trailing data bit positions.

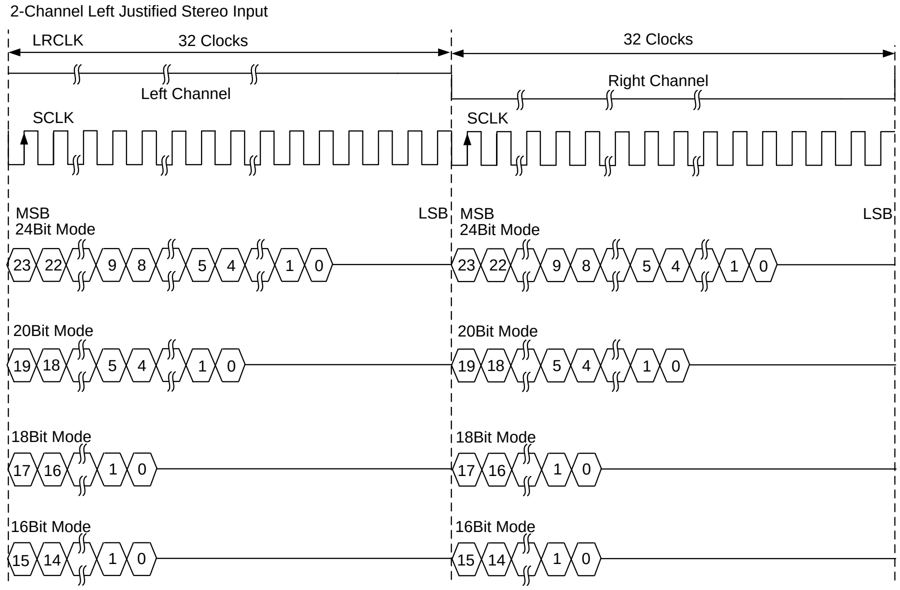


Figure 9. Left Justified 64f_s Format

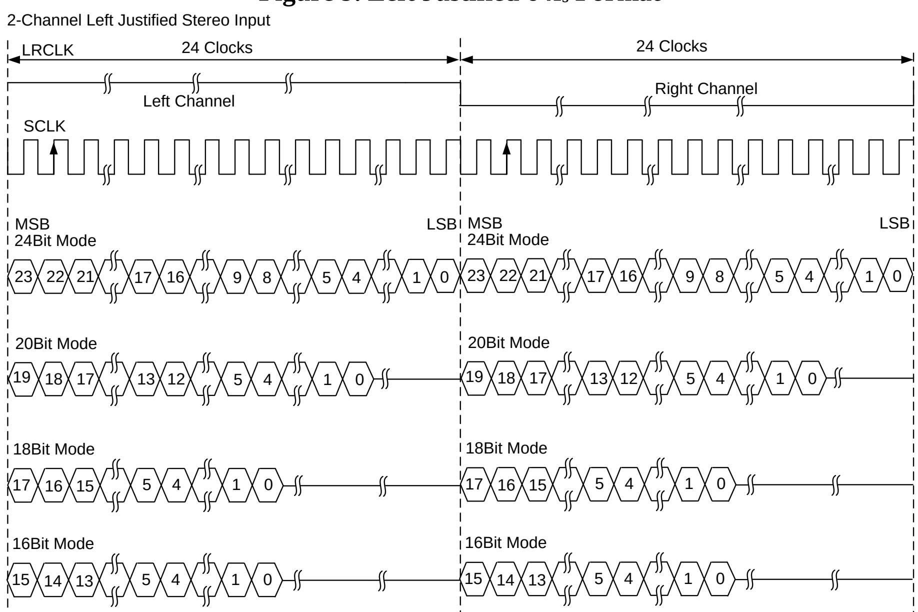


Figure 10. Left Justified 48f_s Format

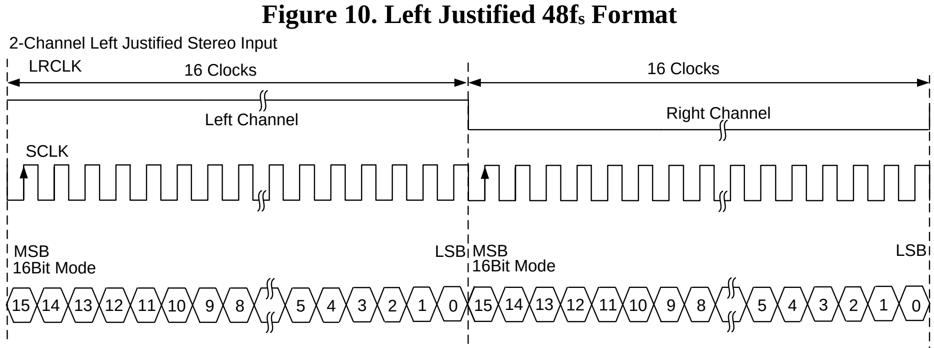


Figure 11. Left Justified 32f_s Format

Right Justified

Right Justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A clock running at $32f_s/48f_s/64f_s$ is used to clock in data. The first bit of data on the data 8bit clock periods after LRCLK toggles. The data is written MSB first and is valid on the rising edge of clock. The DAP masks unused trailing data bit positions.

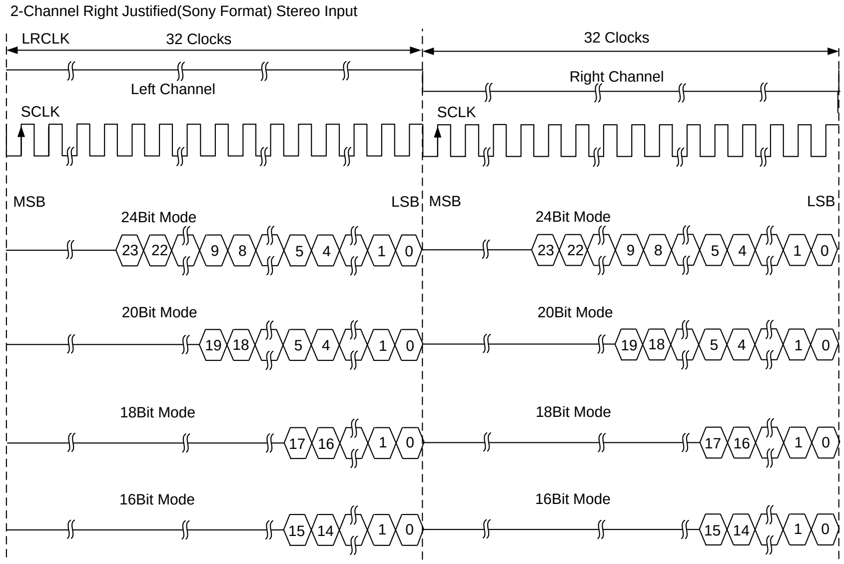


Figure 12. Right Justified $64f_s$ Format

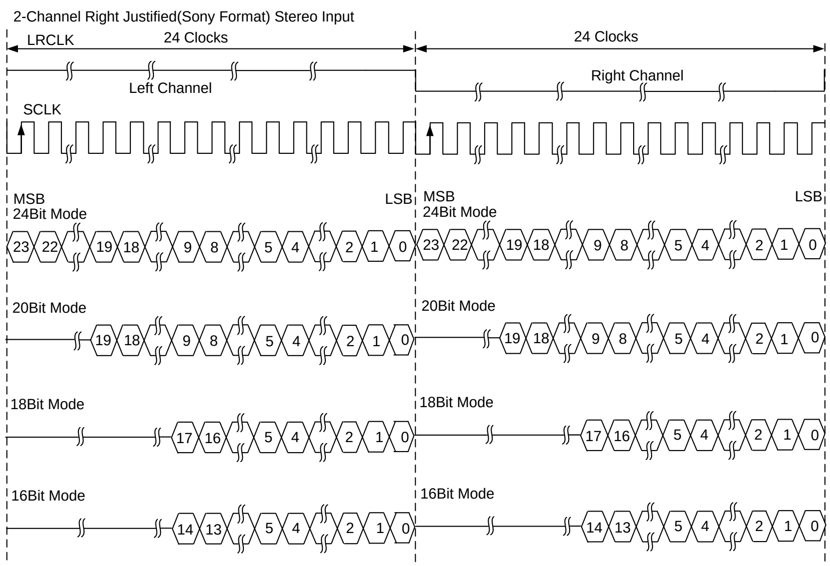


Figure 13. Right Justified $48f_s$ Format

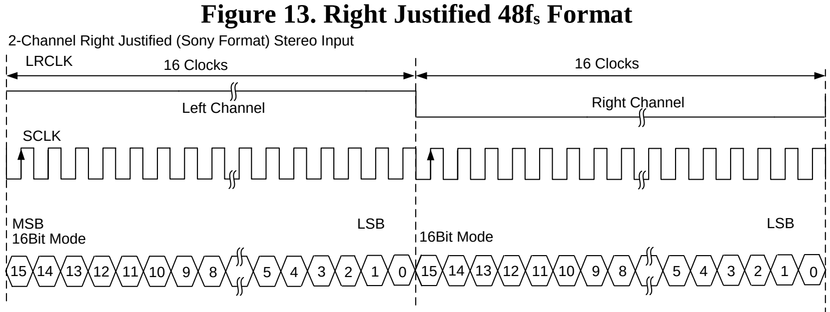


Figure 14. Right Justified $32f_s$ Format

I²C Serial Control Interface

The device DAP has a bidirectional I²C interface that compatible with the I²C bus protocol and supports both 100kHz and 400kHz data transfer rates for single and multiple byte write and read operations. The device does not support a multi-master bus or wait state insertion. The I²C control is used to program the registers of the device and to read device status. The device performs all I²C operations without I²C wait cycles.

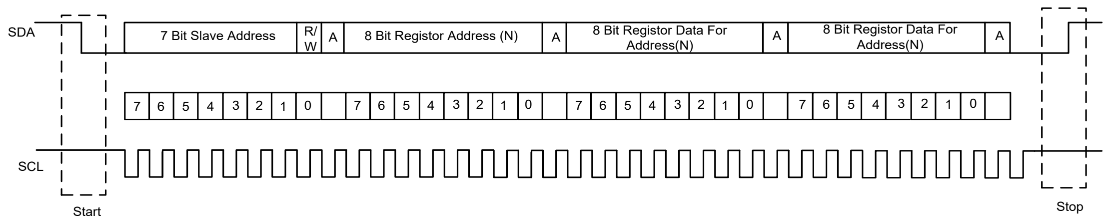


Figure 15. Typical I²C Sequence

There can be only one master device on the same I²C bus, but multi slave devices can be connected in. Every slave device has its own slave address. The master must send a 7 bit target slave address byte plus an R/W bit in the lowest. The lowest bit (the R/W bit) defines whether write(1'b0) to the slave device or read(1'b1) from the slave device. The SY6045B will response an acknowledge signal with the slave address 7'b0101010 if the ADDR_SEL is pulled down or 7'b0101011 if the ADDR_SEL pin is pulled up. So the first byte will be 8'b01010100 (0x54) or 8'b01010110(0x56) when the data are written to the SY6045B.

ADDR_SEL pin	I²C address
Low	0x54
High	0x56

I²C Device Address Change Procedure

Write to device address change enable register, 0xF8 with value of 0xF9 A5 A5A5. Write to device register 0xF9 with a value of 0x0000 00XX , where XX is the new address. Any write after that should use the new device address XX.

Single and Multiple Byte Transfers

The I²C serial control interface supports both single byte and multiple read/write operations for sub addresses 0x00 to 0xFF. However, for the addresses 0x20 to 0xFF, the serial control interface supports single byte or multiple byte read/write operations.

During multiple byte read operations, the DAP responds with data, a byte at a time, starting at the sub address assigned, as long as the master device continues to response with acknowledges. If a particular sub address does not contain 8*N bits, the unused bits are read as logic 0.

During multiple byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific sub address. For example, if a write command is received for a biquad sub address, the DAP expects to receive five 32bit words. If fewer than five 32 bits data words have been received when a stop command (or another start command) is received, the data received is discarded.

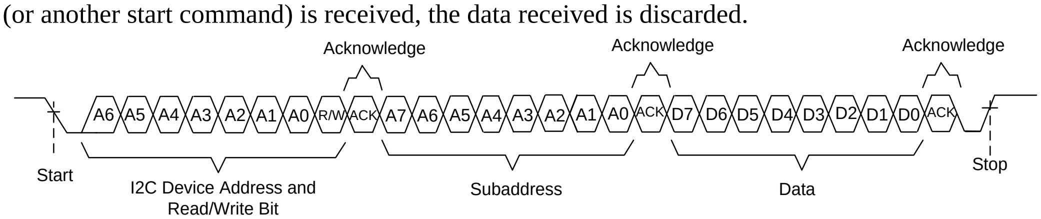


Figure 16. Single Byte Write Transfer

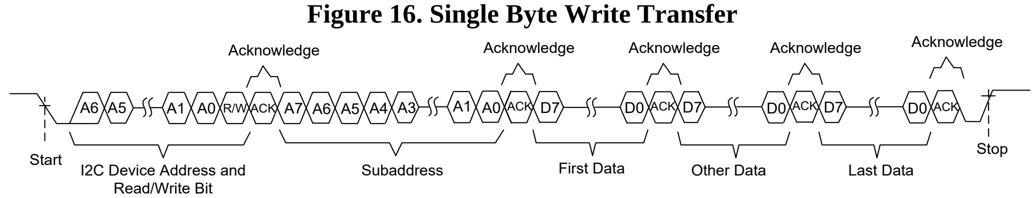


Figure 17. Multiple-Byte Write Transfer

Single Byte Write Transfer

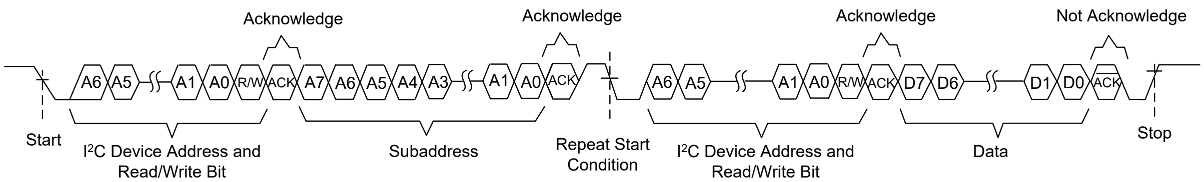


Figure 18. Single Byte Read Transfer

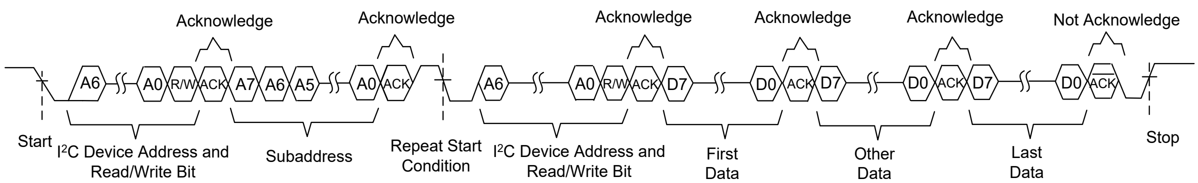


Figure 19. Multiple-Byte Read Transfer

SDATA Generator

SY6045B has 3 monitor pins which can be defined to output SDATA signal, which can be defined prior or after audio signal processing. Refer to table 1 to set the register to decide which monitor to output SDATA signal.

SDATA Generator (Sdata out)	Register value of 0x17	Register value of 0x18	
	00H	0XH	X0H
	Sdata out => Monitor 0 pin	Sdata out => Monitor 1 pin	Sdata out => Monitor 2 pin

Table 1. SDATA Generator Control

Power Meter

The power meter measures signal's energy of internal, which can be used to study the power profile. It can be configured by sending value of energy through register address 0x97 and parts of 0x98. Read the 10-bits value in dB through register address 0x58 while read the 23-bits linear value through register address 0x99.

Output Mode and MUX Selection

The device supports two output modes including BTL and PBTL. In BTL mode, the bit 1 of register 0x1E should be set to 1'b0. It also supports parallel BTL mode with VOUT_A / VOUT_B (and VOUT_C / VOUT_D) connected before the LC filter. The bit 1 of register 0x1E should be set 1'b1 to configure the PBTL mode. If an over current or short condition is detected in either half bridge, all of bridges will be turned off.

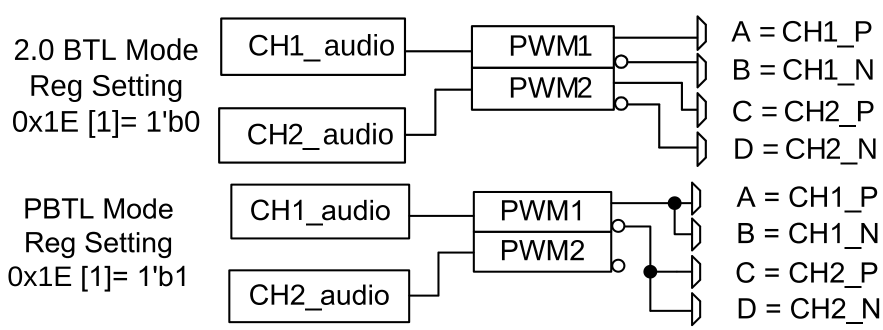


Figure 20. Output Mode and MUX Selection

MIXER

The sound mixer function is available in SY6045B. There are 4 mixer gain coefficients named M11, M12, M21 and M22, which can weight the two channel inputs to the two channel outputs by the their register setting as the following equation.

$$CH1\_OUT=M11*CH1\_IN+M12*CH2\_IN$$

CH2_OUT=M21*CH1_IN+M22*CH2_IN

The 4 mixer gains are stored as dB value, they can be set in register 0x5F, and table 4 lists the relationship between index and dB value.

Mixer Gain			
Index	dB	Index	dB
3F	18	1F	-4
3E	17	1E	-4.5
3D	16	1D	-5
3C	15	1C	-5.5
3B	14	1B	-6
3A	13	1A	-7
39	12	19	-8
38	11	18	-9
37	10	17	-10
36	9	16	-11
35	8	15	-12
34	7	14	-13
33	6	13	-14
32	5.5	12	-15
31	5	11	-16
30	4.5	10	-17
2F	4	0F	-18
2E	3.5	0E	-19
2D	3	0D	-20
2C	2.5	0C	-21
2B	2	0B	-22
2A	1.5	0A	-23
29	1	09	-24
28	0.5	08	-25
27	0	07	-26
26	-0.5	06	-27
25	-1	05	-28
24	-1.5	04	-29
23	-2	03	-30
22	-2.5	02	-31
21	-3	01	-32
20	-3.5	00	mute

Table 2. Mixer Gain

Pre-Processing

32 Bits 6.26 Number Format

All filter coefficients are 32bit coefficients using a 6.26 number format. 6.26 number format means that there are 6 bit to the left of the decimal point and 26 bits to the right of the decimal point.

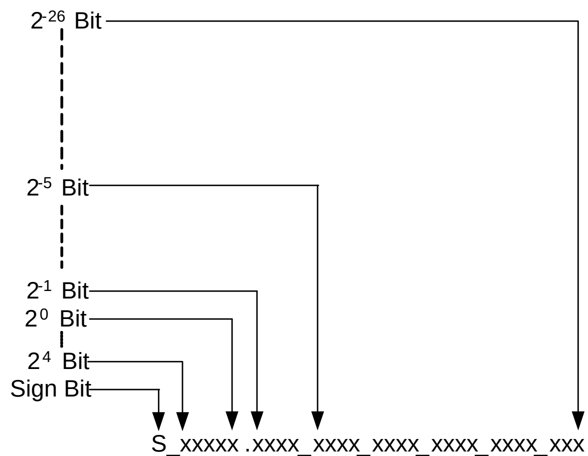


Figure 21. 6.26 Number Format

If the most significant sign bit is logic 0, then the number is a positive number, the weighting shown yields the correct number.

If the most significant sign bit is logic 1, then the number is a negative number. Every bit must be inverted, then add 1 to the result, and then the weighting shown in Figure 22.

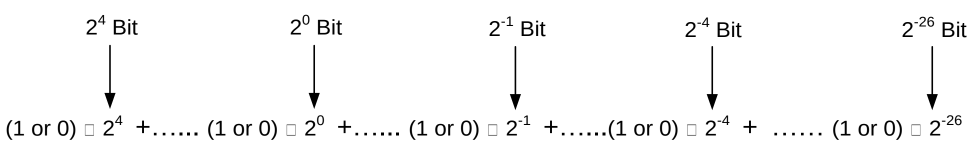


Figure 22. Conversion weighting Factors—6.26 Format to Floating Point

Gain coefficients, entered via I^2C bus, must be entered as 32 bits binary numbers.

BiQuad Structure

Each BiQuad has a 2nd IIR filter structure and has three coefficients on the direct path (b_0, b_1, b_2) and 2 coefficients on feedback path (a_1, a_2) as shown in the diagram.

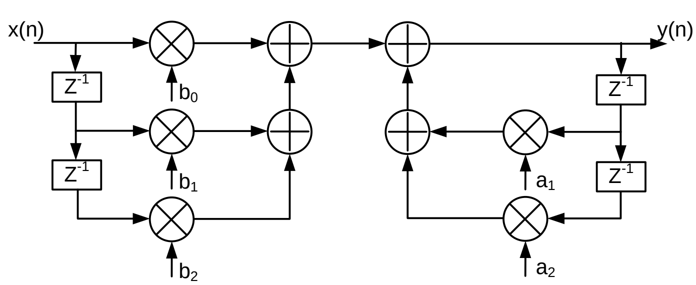


Figure 23. Bi-Quad Filter Structure

There are eighteen Bi-Quad filters linked serially in one channel. The Bi-Quad filters can be configured differently for each filter. The BQ coefficients can be separated for the two channels. To download the BQ coefficient to SY6045B, set bit 0 of register 0x03 first, then select the channel in register 0x03. BQn(n is from 0 to 17) of channel 1 and channel 2 can be separately enabled or disabled. For example, BQ1 of channel 1 is enabled while BQ1 of channel 2 is disabled. As shown in Figure 23, first three filters can be configured as loudness control with loudness gain, and last four filters can be configured as SPEQ with SPEQ control.

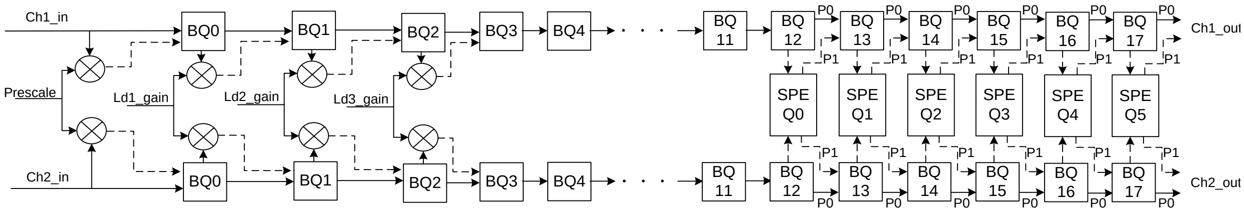


Figure 24. Bi-Quad Filter Chain

Filter coefficients are 32bit binary numbers and can be downloaded through I^{2}C interface. Write actual coefficient values to 20 register addresses in the range from 0x2F to 0x4D to download Bi-Quad filter coefficients to SY6045B. Refer to table 3. The amount of bytes for each register address is variable. For example, 20 bytes are for a BQ filter while 4 bytes are for the Pre-scaler.

The enable/disable operation of these Bi-Quad filters can be made by configuring the bits in register addresses of 0x25~0x2A. When BQn(n from 10 to 17) is configured as SPEQ or SPEQ Limit in register 0x29 and 0x2A, the BQn of both channels are functional as SPEQ or SPEQ Limit together, which can't be separately enabled or disabled for each channel. When BQn is configured as EQn, the EQn can be separately enabled or disabled for each channel.

I^{2}C address	0x2F	0x30	0x31	0x32	0x33
byte count	20	20	20	20	20
description	BQ0 of CH1/2	BQ1 of CH1/2	BQ2 of CH1/2	BQ3 of CH1/2	BQ4 of CH1/2
I^{2}C address	0x34	0x35	0x36	0x37	0x38
byte count	20	20	20	20	20
description	BQ5 of CH1/2	BQ6 of CH1/2	BQ7 of CH1/2	BQ8 of CH1/2	BQ9 of CH1/2
I^{2}C address	0x39	0x3A	0x3B	0x3C	0x3D
byte count	20	20	20	20	20
description	BQ10 of CH1/2	BQ11 of CH1/2	BQ12 of CH1/2	BQ13 of CH1/2	BQ14 of CH1/2
I^{2}C address	0x3E	0x3F	0x40	0x41	0x42
byte count	20	20	20	12	12
description	BQ15 of CH1/2	BQ16 of CH1/2	BQ17 of CH1/2	Coefficients of SPEQ0	Coefficients of SPEQ1
I^{2}C address	0x43	0x44	0x45	0x46	0x4D
byte count	12	12	12	12	12
description	Coefficients of SPEQ2	Coefficients of SPEQ3	Coefficients of SPEQ4	Coefficients of SPEQ5	Loudness Gain

Table 3. Address of Coefficients for Bi-Quad Filter Chain

Loudness Control

The frequency characteristics can be compensated in low volume level to fit the acoustic characteristics of human ears with Loudness control. The three coefficient of loudness can be downloaded through writing the 12 bytes of the register 0x4D. Four bytes are for one BQ loudness gain. The loudness gain values are shared for both channel 1 and channel 2.

Register Address 0x4D	byte count 12	bits[95:64]	3’b000,ld3_gain[28:0]
		bits[63:32]	3’b000,ld2_gain[28:0]
		bits[31:0]	3’b000,ld1_gain[28:0]

Table 4. Loudness Gain

Super Parametric Equalizer

The frequency characteristics based on input signal level can be compensated to ingratiate the acoustic characteristics of human ears with SPEQ function.

There are a Bi-Quad filter coefficient and three additional coefficients for SPEQ. The three additional coefficients are related to gain and threshold. The Bi-Quad filter coefficient can be downloaded through writing 0x3B~0x40. The three additional coefficients can be downloaded through writing the 12 bytes of the register 0x41~0x46. There are four bytes for one coefficient. The SPEQ coefficients are shared for both channel 1 and channel 2.

It can be configured as SPEQ Limit function as well. The frequency characteristics at some frequency point can’t be limited to no more than the threshold with SPEQ Limit function. The way to download the coefficient is the same as SPEQ.

Volume & Dynamic Range Control

Volume Control

The volume register 0x07, 0x08, and 0x09 correspond to master volume, channel 1 volume, and channel 2 volume.
Master Volume Control
Master volume – 0x07 (default is mute, 0x00)

Step	Range
0.5 dB	0 ~ -126 dB

Table 5. Master Volume Steps

Channel Volume Control
Channel-1 volume – 0x08 (default is 0 dB, 0x9F)
Channel-2 volume – 0x09 (default is 0 dB, 0x9F)

Step	Range
0.5 dB	+48 ~ -79 dB

Table 6. Channel Volume Steps

Volume Fine Control and offset

Fine control for volume is +0.125dB step up to maximum +7.875dB boost. Step size is 0.125dB. It has high accurate step size and provides an offset gain for the channel volume and master volume.

Step	Range
0.125 dB	0 ~ +7.875 dB

Table 7. Volume Fine Control Steps

Mute and Soft Volume Change

The chip enters mute state by setting soft mute flag of register Address 0x06. 0x06[3] is master mute flag for both left channel and right channel. 0x06[0] is individually mute flag for left channel while 0x06[1] is individually mute flag for right channel. With soft mute, the volume gradually increases or decreases when mute is turned off or on respectively.

Dynamic Range Control

The DRC scheme has 4 DRC blocks, of which one ganged DRC for the high-band left/right channels, one ganged DRC for the mid-band left/right channels, one ganged DRC for the low-band left/right channels, and one DRC for the mixer output of DRC1, DRC2 and DRC3.

SY6045B has advanced algorithm taking input signal level, volume and threshold for dynamic gain of DRC, which provides powerful and balanced excellent sound experience

There are serveral 16 BQs for all of DRC bands, and the amplitude of each DRC output can be adjusted by corresponding gain control. The outputs of three bands DRC are mixed and followed by DRC4 which produces the output data with the fully controlled dynamic range. For detailed setting of the DRC registers, please refer to the system register addresses in Table 8.

I^2C address	0x47	0x48	0x49	0x4A	0x4B	0x4C	0x4D	0x4E
byte count	20	20	20	20	20	20	20	20
description	BQ0 of DRC	BQ1 of DRC	BQ2 of DRC	BQ3 of DRC	BQ4 of DRC	BQ5 of DRC	BQ6 of DRC	BQ7 of DRC
I^2C address	0x4F	0x50	0x51	0x52	0x53	0x54	0x55	0x56
byte count	20	20	20	20	20	20	20	20
description	BQ8 of DRC	BQ9 of DRC	BQ10 of DRC	BQ11 of DRC	BQ12 of DRC	BQ13 of DRC	BQ14 of DRC	BQ15 of DRC

Table 8. Coefficient Register Map for Dynamic Range Control

The DRC input/output diagram is shown in Figure 25.

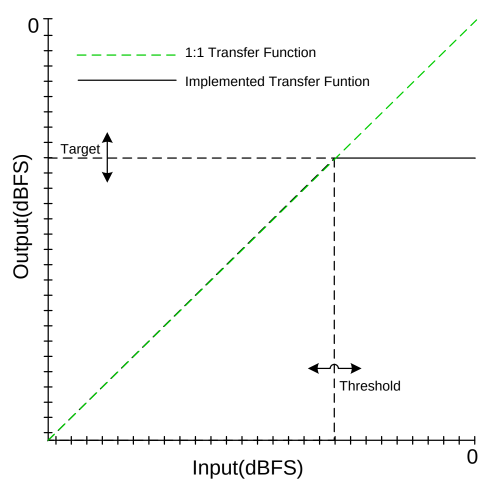


Figure 25. Dynamic Range Control

DC Protection

The system from outputting DC signal can cause a speaker unit burnt. There are two special DC blocking filters integrated inside SY6045B to remove the DC component, the cut off frequency is less than 1Hz.

A PWM DC detector is also employed. When there is a DC component in the output, it sets PWM DC error flag of address 0x02 to high. The external controller may monitor this error flag and reset the chip by writing register 0x0F to assert a soft reset. The threshold of PWM DC detection at address 0x19 can be set to decide the level of DC monitoring for both Ternary and BD mode.

Memory Checksum

There are EQ and DRC coefficients checksum functions in SY6045B. It will calculate the EQ checksum data and DRC checksum data after the coefficients are written into the RAM. If the checksum key from internal checksum block is the same as the checksum key register value which is written by user, it can pass. If not, it will report PBQ checksum error or DRC checksum error. The coefficients are stored in 32-bit units, so the checksum key is also 32 bit. The reference value of memory checksum is the bitwise XOR of all EQ coefficients or DRC coefficients.
The checksum key registers are 0x9A(EQ checksum key of Channel 1), 0x9B(DRC checksum key) and 0x9C(EQ checksum key of channel 2).

The checksum key is calculated by the following equation.

bq_ch1_checksum_key[31:0]=bq0_b0[31:0]^bq0_b1[31:0]^ bq0_b2[31:0]^ bq0_a1[31:0]^ bq0_a2[31:0]^……
^bq17_b0[31:0]^bq17_b1[31:0]^bq17_b2[31:0]^bq17_a1[31:0]^bq17_a2[31:0]^speq0_th[31:0]^speq0_coef1[31:0]
^ …speq0_coef2[31:0]^……^ speq5_th[31:0]^ speq5_coef1[31:0]^ speq5_coef2[31:0];

bq_ch2_checksum_key[31:0]=bq0_b0[31:0]^bq0_b1[31:0]^bq0_b2[31:0]^bq0_a1[31:0]^bq0_a2[31:0]^……^
bq17_b0[31:0] ^ bq17_b1[31:0]^ bq17_b2[31:0]^ bq17_a1[31:0]^ bq17_a2[31:0];

drc_checksum_key[31:0]=drc_bq0_b0[31:0]^drc_bq0_b1[31:0]^drc_bq0_b2[31:0]^drc_bq0_a1[31:0]^drc_bq0_a1[
31:0]^……^drc_bq15_b0[31:0]^drc_bq15_b1[31:0]^drc_bq15_b2[31:0]^drc_bq15_a1[31:0]^drc_bq15_a1[31:0]^l
d1_gain[31:0]^ld2_gain[31:0]^ ld3_gain[31:0];

Recommended Command Sequences

Power up & Initialization Sequence

1) Ramp up VDD_IO to at 3.3V and ramp PVDD to at least 4.5V. There is no sequence requirement between VDD_IO and PVDD when ramping up.
2) Drive SCLK to its desired state, drive RST_B=0 at least 0.1ms, then drive RST_B=1, and wait at least 0.5ms.
3) Configure the DAP via I^2C
4) Configure remaining registers
5) Exit shutdown (0x22=0x00).

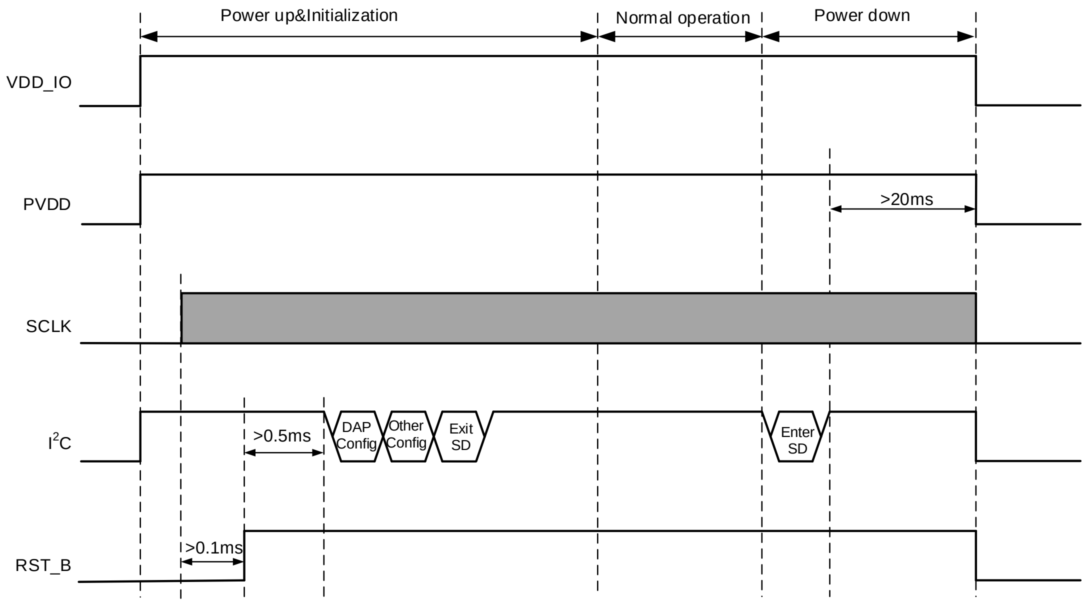


Figure 26. Recommended Command Sequence

Power down Sequence

1) Enter shutdown (0x22=0x30).
2) Wait at least 20 ms
3) Ramp down VDD_IO and PVDD. There is no sequence requirement between VDD_IO and PVDD when ramping down.

APPENDIX

Configuration Register Table

Addr 0x00: Clock control register

Bit	7	6	5	4	3	2	1	0
Name	BS	X		FCME	FRC		FRD	

Name	Label	Type	Default	Description
FRD	fs_rate_det	R	2'b10	Sample rate detected: 2'b00: 32kHz 2'b01: 96kHz 2'b10: 44.1kHz/48kHz 2'b11: reserved
FRC	fs_rate_cnfg	RW	2'b10	Sample rate configured: 2'b00: 32kHz 2'b01: 96kHz 2'b10: 44.1kHz/48kHz 2'b11: reserved If fs_cnfg_manual_en is set to 1, the two bits are valid to configure I^2S sample rate.
FCME	fs_cnfg_manual_en	RW	1'b1	1'b0: auto detect I^2S sample rate 1'b1: configured I^2S sample rate by MCU
BS	brt_sel	RW	1'b0	1'b0:48KHz (in case of pll_ref_clk = osc_clk) 1'b1:44.1KHz (in case of pll_ref_clk = osc_clk)

Addr 0x01: Device Id register

Bit	7	6	5	4	3	2	1	0
Name	DIR							

Name	Label	Type	Default	Description
DIR	dev_id_reg	R	8'h25	Identification Code 0x25: SY6045B

Addr 0x02: Error status register

Bit	7	6	5	4	3	2	1	0
Name	PCE	DRC_CE	SCLKE	LRCLKE	PWM_DE	SF	OCF	OTF

Name	Label	Type	Default	Description
OTF	otuv_fault	RW	1'b0	1'b0: normal; 1'b1: over temperature or under voltage is detected
OCF	oc_fault	RW	1'b0	1'b0: normal; 1'b1: over current is detected
SF	short_fault	RW	1'b0	1'b0: normal; 1'b1: short is detected
PWM_DE	pwm_dc_error	RW	1'b0	1'b0: normal; 1'b1: PWM DC detected
LRCLKE	lrclk_err	RW	1'b0	1'b0: normal; 1'b1: LRCLK error
SCLKE	sclk_err	RW	1'b0	1'b0: normal; 1'b1: SCLK error
DRC_CE	drc_check_error	RW	1'b0	1'b0: normal; 1'b1: DRC checksum error
PCE	pbq_check_error	RW	1'b0	1'b0: normal; 1'b1: BQ checksum error

Addr 0x03: System control register 1

Bit	7	6	5	4	3	2	1	0
Name	DSP_FRE	DSP_SRE	RBCCS	DC_SRE	DFER	RCE1	RCE2	IACRE

Name	Label	Type	Default	Description
IACRE	i2c_access_coef_ram_en	RW	1'b1	1'b0: DAP access to register 0x2F~0x57 (RAM) 1'b1: I^2C bus access to register 0x2F~0x57(RAM)
RCE2	ram_ch2_en	RW	1'b1	1'b1: I^2C write ch2 ram on 1'b0: I^2C write ch2 ram off
RCE1	ram_ch1_en	RW	1'b1	1'b1: I^2C write ch1 ram on 1'b0: I^2C write ch1 ram off
DFER	dsp_fade_en_reg	RW	1'b1	1'b0:Fade disabled, volume changes immediately 1'b1:Fade enabled, volume changes fades between old/new value
DC_SRE	dc_soft_reset_en	RW	1'b1	Enable or Disable the soft reset of the hole chip 1'b0:DC Soft Reset Disabled 1'b1:DC Soft Reset Enabled
RBCCS	rd_bq_coef_channel_sel	RW	1'b0	1'b0:read bq coef of channel 1 1'b1:read bq coef of channel 2
DSP_SRE	dsp_soft_reset_en	RW	1'b1	Enable or Disable the soft reset of dsp data flow——Write bit "1" to register 0x0F bit[4] 1'b0:Write register 0x0F bit[4] won't trigger DSP Soft Reset 1'b1:Write register 0x0F bit[4] will trigger DSP Soft Reset
DSP_FRE	dsp_force_reset_en	RW	1'b0	1'b0: Shutdown the speaker won't trigger the reset of dsp data flow. 1'b1: When speaker shutdown, dsp data flow will be reset automatically.

Addr 0x04: System control register 2

Bit	7	6	5	4	3	2	1	0
Name	DOSE	AURE	DEPRE	EQ_E	DEPOST	ME	PE	LE

Name	Label	Type	Default	Description
LE	loudness_en	RW	1'b0	enable loudness: 1'b0: disable; 1'b1: enable
PE	pm_en	RW	1'b1	enable power meter: 1'b0: disable; 1'b1: enable
ME	mixer_en mixer_en	RW	1'b1	enable mixer: 1'b0: disable; 1'b1: enable
DEPOST	dc_en_post	RW	1'b1	Post DC blocking enable. 1'b0: disable; 1'b1: enable
EQ_E	eq_enable	RW	1'b1	eq, speq, enable or not: 1'b0: disable; 1'b1: enable
DEPRE	dc_en_pre	RW	1'b0	Pre DC blocking enable: 1'b0: disable; 1'b1: enable
AURE	avdd_uv_rst_en_reg	RW	1'b0	AVDD under voltage will trigger a global reset or not 1'b0: won't trigger a global reset; 1'b1: trigger a global reset;
DOSE	dyn_off_speq_en	RW	1'b1	When write "1" to register 0x03 bit[0] to enable I^2C access coef ram, turn off speq simultaneously; 1'b0: turn off speq at the same time; 1'b1: won't turn off speq;

Addr 0x05: System control register 3

Bit	7	6	5	4	3	2	1	0
Name	DLL					SRS		ASMR

Name	Label	Type	Default	Description
ASMR	a_sel_mode_reg	RW	1'b0	1'b0:when reset release, i2c device addr was fixed by addr_sel. 1'b1:when addr_sel configured as input, i2c device address could be changed according to addr_sel in any moment.
SRS	sold_rate_sel[1:0]	RW	2'b10	When speaker poweron, select the cost time of detecting open load/short load (if the detection eabled). 2'b00:73.6ms; 2'b01:147.2ms; 2'b10:294.4ms; 2'b11:588.5ms.
DLL	delay_line_lgth[4:0]	RW	5'h0f	Length of DRC delay line 0~20 samples.

Addr 0x06: Soft mute register

Bit	7	6	5	4	3	2	1	0
Name	X		MSEN	HSU	DMMR	X	DDMRR	DDMLR

Name	Label	Type	Default	Description
DDMLR	dsp_dvol_mute_l_reg	RW	1'b0	1'b0:soft unmute channel 1 1'b1:soft mute channel 1
DDMRR	dsp_dvol_mute_r_reg	RW	1'b0	1'b0:soft unmute channel 2 1'b1:soft mute channel 2
DMMR	dsp_mvol_mute_reg	RW	1'b0	1'b0:master unmute 1'b1:master mute
HSU	hard_soft_umute	RW	1'b1	1'b0:soft unmute on recovery from clock error 1'b1:hard unmute on recovery from clock error
MSEN	i2c_access_ram_mute_stby_en	RW	1'b1	1'b0: Disable 1'b1: Enable

Addr 0x07: Master volume

Bit	7	6	5	4	3	2	1	0
Name	MV							

Name	Label	Type	Default	Description
MV	mas_vol[7:0]	RW	8’h00	8'h00~8'h02: Soft mute; 8'h03: -126dB; 8'hFF: 0dB; step: 0.5dB

Addr 0x08: Channel 1 volume

Bit	7	6	5	4	3	2	1	0
Name	VOLCH1							

Name	Label	Type	Default	Description
VOLCH1	dsp_dvol_l[7:0]	RW	8'h9F	8'h00: mute; 8'h01: -79dB; 8'h9F: 0dB; 8'hFF: 48dB; step: 0.5dB

Addr 0x09: Channel 2 volume

Bit	7	6	5	4	3	2	1	0
Name	VOLCH2							

Name	Label	Type	Default	Description
VOLCH2	dsp_dvol_r[7:0]	RW	8'h9F	8'h00: mute; 8'h01: -79dB; 8'h9F: 0dB; 8'hFF: 48dB; step: 0.5dB

Addr 0x0B: VOL_FTUNE

Bit	7	6	5	4	3	2	1	0
Name	X		VOLFT					

Name	Label	Type	Default	Description
VOLFT	vol_fine_tune[5:0]	RW	6'h00	Volume offset and fine tune. 6'h00~6'h3f: 0dB~+7.875dB. step: 0.125dB.

Addr 0x0F: Soft Reset Register

Bit	7	6	5	4	3	2	1	0
Name	X			DSPRST	X			DCRST

Name	Label	Type	Default	Description
DCRST	dc_soft_reset	RW	1'b0	Write this bit 1, will reset the whole chip. The bit will be automatically cleared to 1'b0 after DC soft reset is asserted.
DSPRST	dsp_reset	RW	1'b0	When register 0x03 bit[6] set “1”， dsp data flow soft reset is enable, then write this bit 1, will reset the dsp data process flow. “dsp_force_reset_en” from register 0x03 will affect the reset flow.

Addr 0x10: Modulation limit register

Bit	7	6	5	4	3	2	1	0
Name	PWMMIN				PWMMAX			

Name	Label	Type	Default	Description
PWMMAX	pwm_mod_limt_max [3:0]	RW	4'h7	PWM modulation frequency is 384kHz set FULL = 512(384kHz); 4'h0: max = FULL-2; 4'h1: max = FULL-3; 4'h2: max = FULL-4; 4'h3: max = FULL-5; 4'h4: max = FULL-6; 4'h5: max = FULL-7; 4'h6: max = FULL-8; 4'h7: max = FULL-9; 4'h8: max = FULL-10; 4'h9: max = FULL-11; 4'ha: max = FULL-12; 4'hb: max = FULL-13; 4'hc: max = FULL-14; 4'hd: max = FULL-16; 4'he: max = FULL-18; 4'hf: max = FULL-20;

PWMMIN	pwm_mod_limt_min[3:0]	RW	4'h7	PWM modulation frequency is 384kHz 4'h0: min = 2; 4'h1: min = 3; 4'h2: min = 4; 4'h3: min = 5; 4'h4: min = 6; 4'h5: min = 7; 4'h6: min = 8; 4'h7: min = 9; 4'h8: min =10; 4'h9: min =11; 4'ha: min =12; 4'hb: min =13; 4'hc: min =14; 4'hd: min =16; 4'he: min =18; 4'hf: min = 20;

Addr 0x11: PWM A Channel delay

Bit	7	6	5	4	3	2	1	0
Name	PWMPD1							

Name	Label	Type	Default	Description
PWMPD1	pwm_phaseoffset1 [7:0]	RW	8'h00	Add an offset delay to PWM_CH1P , -128(lead 128 cycles) ~127(lag 127 cycles), 80H(-128)->FF(-1)->00(0)->7F(127) Step: 5.1ns 48khz base rate, 5.536ns 44.1khz base rate

Addr 0x12: PWM B Channel delay

Bit	7	6	5	4	3	2	1	0
Name	PWMPD2							

Name	Label	Type	Default	Description
PWMPD2	pwm_phaseoffset2 [7:0]	RW	8'h00	Add an offset delay to PWM_CH1N ,-128(lead 128 cycles) ~127(lag 127 cycles), 80H(-128)->FF(-1)->00(0)->7F(127) Step: 5.1ns 48khz base rate, 5.536ns 44.1khz base rate

Addr 0x13: PWM C Channel delay

Bit	7	6	5	4	3	2	1	0
Name	PWMPD3							

Name	Label	Type	Default	Description
PWMPD3	pwm_phaseoffset3 [7:0]	RW	8'h00	Add an offset delay to PWM_CH2P , -128(lead 128 steps) ~127(lag 127 steps), 80H(-128)->FF(-1)->00(0)->7F(127) Step: 5.1ns 48khz base rate, 5.536ns 44.1khz base rate

Addr 0x14: PWM D Channel delay

Bit	7	6	5	4	3	2	1	0
Name	PWM_PD4							

Name	Label	Type	Default	Description
PWM_PD4	pwm_phaseoffset4 [7:0]	RW	8'h00	Add an offset delay to PWM_CH2N , -128(lead 128 cycles) ~127(lag 127 cycles), 80H(-128)->FF(-1)->00(0)->7F(127) Step: 5.1ns 48khz base rate, 5.536ns 44.1khz base rate

Addr 0x15: I^{2}S Control

Bit	7	6	5	4	3	2	1	0
Name	X	I2S_SI	I2S_LI	I2S_en	I2S_FMT		I2S_BIT	

Name	Label	Type	Default	Description
I2S_BIT	i2s_vbits	RW	2'b00	2'b00: 24bits; 2'b01: 20bits 2'b10: 18bits; 2'b11: 16bits
I2S_FMT	i2s_fmt	RW	2'b00	2'b00: I2S; 2'b01: LJ 2'b10: RJ; 2'b11: Reserved
I2S_en	i2s_en	RW	1'b1	0:disable 1: enable
I2S_LI	i2s_lr_polarity	RW	1'b0	1'b0: not invert LRCLK; 1'b1: invert LRCLK
I2S_SI	i2s_sclk_inv	RW	1'b0	1'b0: not invert SCLK; 1'b1: invert SCLK

Addr 0x16: DSP Control Register1

Bit	7	6	5	4	3	2	1	0
Name	FRS			DSP_FTS		CH1_en	CH2_en	X

Name	Label	Type	Default	Description
CH2_en	ch2_en	RW	1'b1	Enable channel 2: 1'b0 disable; 1'b1: enable.
CH1_en	ch1_en	RW	1'b1	Enable channel 1: 1'b0 disable; 1'b1: enable.
DSP_FTS	dsp_fade_time_sel	RW	2'b00	2'b00: default, x1, about 8ms; 2'b01: x2; 2'b10: x4; 2'b11: x8.
FRS	fir_rolloff_sel	RW	3'b000	FIR interpolation filter select, different setting has different passband, stopband, passband ripple and stop band attenuation. Default 3'b000.

Addr 0x17: Monitor Pin configured Register1

Bit	7	6	5	4	3	2	1	0
Name	mon0_en	mon1_en	mon2_en	SD_L	MON0			

Name	Label	Type	Default	Description
MON0	monitor0_cfg[3:0]	RW	4'h0	4'h0: i2s_data_out; 4'h1: pwm_out_a; 4'h2: pwm_out_b; 4'h3: pwm_out_c; 4'h4: pwm_out_d; 4'h5: stbyb; 4'h6: fault_clr_ready;

				4'h7: pll_locked; 4'h8: fault_otuv; 4'h9: a2d_osc_clk; 4'ha: pll_div32; 4'hb: fault_pin_stat; 4'hc: fault_short; 4'hd: avdd_uv; 4'he: shdwb; 4'hf: fault_oc.
SD_L	sda_out_loc	RW	1'b0	I^2S data out selection. 1: select audio data prior to processing. 0: select data behind prcossing.
mon2_en	monitor2_en	RW	1'b0	enable monitor2. 1'b0: disable; 1'b1: enable.
mon1_en	monitor1_en	RW	1'b0	enable monitor1. 1'b0: disable; 1'b1: enable.
mon0_en	monitor0_en	RW	1'b0	enable monitor0. 1'b0: disable; 1'b1: enable.

Addr 0x18: Monitor Pin configured Register2

Bit	7	6	5	4	3	2	1	0
Name	M1C				M2C			

Name	Label	Type	Default	Description
MON2	monitor2_cfg[3:0]	RW	4'h0	4'h0: i2s_data_out; 4'h1: pwm_out_a; 4'h2: pwm_out_b; 4'h3: pwm_out_c; 4'h4: pwm_out_d; 4'h5: stbyb; 4'h6: fault_clr_ready; 4'h7: pll_locked; 4'h8: fault_otuv; 4'h9: a2d_osc_clk; 4'ha: pll_div32; 4'hb: fault_pin_stat; 4'hc: fault_short; 4'hd: avdd_uv; 4'he: shdwb; 4'hf: fault_oc.
MON1	Monitor1_cfg[3:0]	RW	4'h0	4'h0: i2s_data_out; 4'h1: pwm_out_a; 4'h2: pwm_out_b; 4'h3: pwm_out_c; 4'h4: pwm_out_d; 4'h5: stbyb; 4'h6: fault_clr_ready; 4'h7: pll_locked; 4'h8: fault_otuv; 4'h9: a2d_osc_clk; 4'ha: pll_div32; 4'hb: fault_pin_stat; 4'hc: fault_short; 4'hd: avdd_uv; 4'he: shdwb; 4'hf: fault_oc.

Addr 0x19: PWM Direct Current Threshold

Bit	7	6	5	4	3	2	1	0
Name	X	ODFE	AFOE	FBC	TH			

Name	Label	Type	Default	Description
TH	threshold_sel[3:0]	RW	4'h5	When enable PWM DC detection, the signal transient level of both left and right channel output is monitored for each pwm cycle. If the transient level is larger than the threshold for more than 500ms, a DC component is detected on PWM output. The threshold can be set as following, step is 1% of full scale PWM output: 4'h0:1% ; 4'h1:2%; …… 4'hf: 15%.
FBC	fault_b_ctrl	RW	1'b0	Fault_B control method. 1'b0: when fault_b is asserted, high level of fault_b will be active when detected by the window set in 0x1B; 1'b1: when fault_b is asserted, high level of fault_b will be active directly.
AFOE	adr_faultb_output_en	RW	1'b0	1'b0: input addr_sel ; 1'b1: output fault_b.
ODFE	open_drain_faultb_en	RW	1'b0	control open drain faultb: 1'b0: disable; 1'b1: enable.

Addr 0x1B: Short Control Register

Bit	7	6	5	4	3	2	1	0
Name	STE	FCI			SPE	RI		

Name	Label	Type	Default	Description
RI	retry_interval	RW	3'b101	3'd0: 100ms; 3'd1: 200ms; 3'd2: 400ms; 3'd3: 600ms; 3'd4: 800ms; 3'd5: 1second; 3'd6: 2second; 3'd7: 4second.
SPE	second_phase_en	RW	1'b1	1'b0: disable; 1'b1: enable.
FCI	fault_clr_interval	RW	3'b011	3'd2: 2ms; 3'd3: 4ms; 3'd4: 8ms; 3'd5: 16ms; 3'd6: 32ms; Others: 4ms.
STE	short_try_en	RW	1'b1	When short is detected after power on, enable check that if the pin short to PVDD or ground. 1'b1: enable; 1'b0: disable.

Addr 0x1C: Fault Output Time

Bit	7	6	5	4	3	2	1	0
Name	X				BKND			

Name	Label	Type	Default	Description
BKND	bknd[3:0]	RW	4'h2	After pad_adr_fault_b is configured as output, any fault of oc, otuv, avdd_uv, short, and short load, will trigger pad_adr_fault_b output a negative pulse; the pulse width has a lower limit. If the fault release earlier than the lower limit time, pad_adr_fault_b will release at the lower limit time, else it will release togather with these faults 4'h2: 299ms; 4'h3: 499ms; 4'h4: 598ms; 4'h5: 748ms; 4'h6: 898ms; 4'h7: 1047ms; 4'h8: 1197ms; 4'h9: 1346ms; others: 1496ms;

Addr 0x1E: Operation Mode

Bit	7	6	5	4	3	2	1	0
Name	X					PBTL_DE	PBTL_en	TM_en

Name	Label	Type	Default	Description
TM_en	ternary_mode_en	RW	1'b1	1'b0: Reserved Mode; 1'b1: Ternary Mode;
PBTL_en	pbtl_en	RW	1'b0	1'b0: btl mode; 1'b1: pbtl mode
PBTL_DE	pbtl_digital_en	RW	1'b1	Enable the digital die of re-selecting the output from PWMA~D to work as pbtl mode 1‘b0: disable; 1'b1: enable

Addr 0x1F: Checksum Control Register

Bit	7	6	5	4	3	2	1	0
Name	X					PDDE	PCE	DCE

Name	Label	Type	Default	Description
DCE	drc_checksum_en	RW	1'b0	1'b0: disable; 1'b1: check the DRC coefficient part of memory (from 0x47 to 0x57).
PCE	pbq_checksum_en	RW	1'b0	1'b0: disable; 1'b1: check the PBQ coefficient part of memory , channel 1 & 2 independently (from 0x2f to 0x46 of channel 1 ram, from 0x2f to 0x40 of channel 2 ram).
PDDE	pwm_dc_det_en	RW	1'b0	1'b0: disable the DC detection on PWM; 1'b1: enable the DC detection.

Addr 0x20: Input MUX Register

Bit	7	6	5	4	3	2	1	0
Name	CSS		X					

Name	Label	Type	Default	Description
CSS	ch_src_sel[1:0]	RW	2'b00	2'b00:I^{2}S Left channel data for ch1, right channel data for ch2; 2'b01:I^{2}S right channel data for ch1, left channel data for ch2; 2'b10: (right + left)/2 for ch1 and ch2; 2'b11:data = 0.

Addr 0x21: DSP Control register2

Bit	7	6	5	4	3	2	1	0
Name	DAL			DAE	DC1AF	DC2AF	X	

Name	Label	Type	Default	Description
DC2AF	dsp_ch2_amute_flag	R	1'b0	DSP right channel auto mute flag, read only.
DC1AF	dsp_ch1_amute_flag	R	1'b0	DSP left channel auto mute flag, read only.
DAE	dsp_amute_en	RW	1'b0	1'b0: DSP auto mute disabled; 1'b1: DSP auto mute enabled.
DAL	dsp_amute_len[2:0]	RW	3'b000	3'b000: auto mute zero detect length, 512; 3'b001: auto mute zero detect length, 1024; 3'b010: auto mute zero detect length, 2048; 3'b011: auto mute zero detect length, 4096; 3'b100: auto mute zero detect length, 4096*2; 3'b101: auto mute zero detect length, 4096*4; 3'b110: auto mute zero detect length, 4096*8; 3'b111: auto mute zero detect length, 4096*16.

Addr 0x22: PWM Control register

Bit	7	6	5	4	3	2	1	0
Name	X		SDOWN	SBY	X			

Name	Label	Type	Default	Description
SBY	enter_all_standby	RW	1'b1	1'b0:exit all-channel standby; 1'b1:enter all-channel standby (hard mute, hiz, sound off).
SDOWN	enter_all_shutdown	RW	1'b1	1'b0:exit all-channel shutdown (normal operation); 1'b1:enter all-channel shutdown (hard mute, hiz).

Addr 0x23: Fault Select Register

Bit	7	6	5	4	3	2	1	0
Name	X	FCTS			PSDE	X	SMOE	X

Name	Label	Type	Default	Description
SMOE	short_mask_oc_en	RW	1'b1	1'b0: disable; 1'b1: enable;
PSDE	poweron_short_det_en	RW	1'b0	1'b0: disable; 1'b1: enable;

FCTS	fault_clr_times_sel[2:0]	RW	3'b001	3'b000: fault detected 2 times, fault_lock active 3'b001: fault detected 5 times, fault_lock active 3'b010: fault detected 10 times, fault_lock active 3'b011: fault detected 15 times, fault_lock active 3'b100: fault detected 20 times, fault_lock active 3'b101: fault detected 25 times, fault_lock active 3'b110: fault detected 30 times, fault_lock active 3'b111: fault detected infinte times, fault_lock active

Addr 0x25: Channel1 EQ Filter Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	EQ15	EQ14	EQ5	EQ4	EQ3	EQ2	EQ1	EQ0

Name	Label	Type	Default	Description
EQ0	ch1_eq0_en	RW	1'b0	Ch1 EQ0, 1'b0: bypass, 1'b1: enable
EQ1	ch1_eq1_en	RW	1'b0	Ch1 EQ1, 1'b0: bypass, 1'b1: enable
EQ2	ch1_eq2_en	RW	1'b0	Ch1 EQ2, 1'b0: bypass, 1'b1: enable
EQ3	ch1_eq3_en	RW	1'b0	Ch1 EQ3, 1'b0: bypass, 1'b1: enable
EQ4	ch1_eq4_en	RW	1'b0	Ch1 EQ4, 1'b0: bypass, 1'b1: enable
EQ5	ch1_eq5_en	RW	1'b0	Ch1 EQ5, 1'b0: bypass, 1'b1: enable
EQ14	ch1_eq14_en	RW	1'b0	Ch1 EQ14, 1'b0: bypass, 1'b1: enable
EQ15	ch1_eq15_en	RW	1'b0	Ch1 EQ15, 1'b0: bypass, 1'b1: enable

Addr 0x26: Channel1 EQ Filter Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	EQ13	EQ12	EQ11	EQ10	EQ9	EQ8	EQ7	EQ6

Name	Label	Type	Default	Description
EQ6	ch1_eq6_en	RW	1'b0	Ch1 EQ6, 1'b0: bypass, 1'b1: enable
EQ7	ch1_eq7_en	RW	1'b0	Ch1 EQ7, 1'b0: bypass, 1'b1: enable
EQ8	ch1_eq8_en	RW	1'b0	Ch1 EQ8, 1'b0: bypass, 1'b1: enable
EQ9	ch1_eq9_en	RW	1'b0	Ch1 EQ9, 1'b0: bypass, 1'b1: enable
EQ10	ch1_eq10_en	RW	1'b0	Ch1 EQ10, 1'b0: bypass, 1'b1: enable
EQ11	ch1_eq11_en	RW	1'b0	Ch1 EQ11, 1'b0: bypass, 1'b1: enable
EQ12	ch1_eq12_en	RW	1'b0	Ch1 EQ12, 1'b0: bypass, 1'b1: enable
EQ13	ch1_eq13_en	RW	1'b0	Ch1 EQ13, 1'b0: bypass, 1'b1: enable

Addr 0x27: Channel2 EQ Filter Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	EQ15	EQ14	EQ5	EQ4	EQ3	EQ2	EQ1	EQ0

Name	Label	Type	Default	Description
EQ0	ch2_eq0_en	RW	1'b0	Ch2 EQ0, 1'b0: bypass, 1'b1: enable
EQ1	ch2_eq1_en	RW	1'b0	Ch2 EQ1, 1'b0: bypass, 1'b1: enable
EQ2	ch2_eq2_en	RW	1'b0	Ch2 EQ2, 1'b0: bypass, 1'b1: enable
EQ3	ch2_eq3_en	RW	1'b0	Ch2 EQ3, 1'b0: bypass, 1'b1: enable

EQ4	ch2_eq4_en	RW	1'b0	Ch2 EQ4, 1'b0: bypass, 1'b1: enable
EQ5	ch2_eq5_en	RW	1'b0	Ch2 EQ5, 1'b0: bypass, 1'b1: enable
EQ14	ch2_eq14_en	RW	1'b0	Ch2 EQ14, 1'b0: bypass, 1'b1: enable
EQ15	ch2_eq15_en	RW	1'b0	Ch2 EQ15, 1'b0: bypass, 1'b1: enable

Addr 0x28: Channel2 EQ Filter Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	EQ13	EQ12	EQ11	EQ10	EQ9	EQ8	EQ7	EQ6

Name	Label	Type	Default	Description
EQ6	ch2_eq6_en	RW	1'b0	Ch2 EQ6, 1'b0: bypass, 1'b1: enable.
EQ7	ch2_eq7_en	RW	1'b0	Ch2 EQ7, 1'b0: bypass, 1'b1: enable.
EQ8	ch2_eq8_en	RW	1'b0	Ch2 EQ8, 1'b0: bypass, 1'b1: enable.
EQ9	ch2_eq9_en	RW	1'b0	Ch2 EQ9, 1'b0: bypass, 1'b1: enable.
EQ10	ch2_eq10_en	RW	1'b0	Ch2 EQ10, 1'b0: bypass, 1'b1: enable.
EQ11	ch2_eq11_en	RW	1'b0	Ch2 EQ11, 1'b0: bypass, 1'b1: enable.
EQ12	ch2_eq12_en	RW	1'b0	Ch2 EQ12, 1'b0: bypass, 1'b1: enable.
EQ13	ch2_eq13_en	RW	1'b0	Ch2 EQ13, 1'b0: bypass, 1'b1: enable.

Addr 0x29: SPEQ Filter Control Register1

Bit	7	6	5	4	3	2	1	0
Name	CH1_EQ17	CH1_EQ16	CH2_EQ17	CH2_EQ16	BQ17_ctrl		BQ16_ctrl	

Name	Label	Type	Default	Description
BQ16_ctrl	bq16_ctrl[1:0]	RW	2'b00	2'b00: bq16 configured as EQ16; 2'b01: bq16 configured as SPEQ4; 2'b10: bq16 configured as SPEQ4 Limit; 2'b11: reserved.
BQ17_ctrl	bq17_ctrl[1:0]	RW	2'b00	2'b00: bq17 configured as EQ17; 2'b01: bq17 configured as SPEQ5; 2'b10: bq17 configured as SPEQ5 Limit; 2'b11: reserved.
CH2_EQ16	ch2_eq16_en	RW	1'b0	Ch2 EQ16, 1'b0: bypass, 1'b1: enable.
CH2_EQ17	ch2_eq17_en	RW	1'b0	Ch2 EQ17, 1'b0: bypass, 1'b1: enable.
CH1_EQ16	ch1_eq16_en	RW	1'b0	Ch1 EQ16, 1'b0: bypass, 1'b1: enable.
CH1_EQ17	ch1_eq17_en	RW	1'b0	Ch1 EQ17, 1'b0: bypass, 1'b1: enable.

Addr 0x2A: SPEQ Filter Control Register2

Bit	7	6	5	4	3	2	1	0
Name	BQ15_ctrl		BQ14_ctrl		BQ13_ctrl		BQ12_ctrl	

Name	Label	Type	Default	Description
BQ12_ctrl	bq12_ctrl[1:0]	RW	2'b00	2'b00: bq12 configured as EQ12; 2'b01: bq12 configured as SPEQ0; 2'b10: bq12 configured as SPEQ0 Limit; 2'b11: reserved.
BQ13_ctrl	bq13_ctrl[1:0]	RW	2'b00	2'b00: bq13 configured as EQ13; 2'b01: bq13 configured as SPEQ1; 2'b10: bq13 configured as SPEQ1 Limit; 2'b11: reserved.
BQ14_ctrl	bq14_ctrl[1:0]	RW	2'b00	2'b00: bq14 configured as EQ14; 2'b01: bq14 configured as SPEQ2; 2'b10: bq14 configured as SPEQ2 Limit; 2'b11: reserved.
BQ15_ctrl	bq15_ctrl[1:0]	RW	2'b00	2'b00: bq15 configured as EQ15; 2'b01: bq15 configured as SPEQ3; 2'b10: bq15 configured as SPEQ3 Limit; 2'b11: reserved.

Addr 0x2B: SPEQ Filter Control Register3

Bit	7	6	5	4	3	2	1	0
Name	X							SDM

Name	Label	Type	Default	Description
SDM	speq_det_method	RW	1'b0	1'b0: envelope 1'b1: rms

Addr 0x2C:Prescaler

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRE															

Name	Label	Type	Default	Description
PRE	prescaler[15:0]	RW	16'h7FFF	0000~FFFF, pre scale. Linear gain, 7FFF is x1(0dB). FFFF is x2(6dB)

Addr 0x2D: Postscaler

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POST															

Name	Label	Type	Default	Description
POST	postscaler[15:0]	RW	16'h7FFF	0000~FFFF, post scale. Linear gain, 7FFF is x1(0dB). FFFF is x2(6dB)

Addr 0x2F~0x40: BQn(n=0,1,2…17)

Bit	159:128	127:96	95:64	63:32	31:0
Name	A2	A1	B2	B1	B0

Name	Label	Type	Default	Description
B0	bqn_b0[31:0]	RW	0x0400_0000	BQ coefficient,
B1	bqn_b1[31:0]	RW	0x0000_0000	BQ coefficient,
B2	bqn_b2[31:0]	RW	0x0000_0000	BQ coefficient,
A1	bqn_a1[31:0]	RW	0x0000_0000	BQ coefficient,
A2	bqn_a2[31:0]	RW	0x0000_0000	BQ coefficient,

Addr 0x41~46: SPEQn(n=0,1,2…5)

Bit	95:64	63:32	31:0
Name	COEF2	COEF1	TH

Name	Label	Type	Default	Description
TH	speqn_th[31:0]	RW	0x0020_0000	SPEQn threshold
COEF1	speqn_coef1[31:0]	RW	0x0400_0000	SPEQn coefficient 1
COEF2	speqn_coef2[31:0]	RW	0x0200_0000	SPEQn coefficient 2

Addr 0x47~56: DRC BQn(n=0,1,2…15)

Bit	159:128	127:96	95:64	63:32	31:0
Name	A2	A1	B2	B1	B0

Name	Label	Type	Default	Description
B0	drcn_bq0_b0[31:0]	RW	0x0400_0000	BQ coefficient, [31:29] is reserved
B1	drcn_bq0_b1[31:0]	RW	0x0000_0000	BQ coefficient, [31:29] is reserved
B2	drcn_bq0_b2[31:0]	RW	0x0000_0000	BQ coefficient, [31:29] is reserved
A1	drcn_bq0_a1[31:0]	RW	0x0000_0000	BQ coefficient, [31:29] is reserved
A2	drcn_bq0_a2[31:0]	RW	0x0000_0000	BQ coefficient, [31:29] is reserved

Addr 0x57: Channel 1&2 Loudness

Bit	95:64	63:32	31:0
Name	LD3_G	LD2_G	LD1_G

Name	Label	Type	Default	Description
LD1_G	ld1_gain[31:0]	RW	0x4000_0000	loudness gain of BQ1, only positive. 0x0000_0000(-inf)~0x0800_0000(x1, 0dB)~0x0FFF_FFFF(x2, +6dB)
LD2_G	ld2_gain[31:0]	RW	0x4000_0000	loudness gain of BQ2, only positive. 0x0000_0000(-inf)~0x0800_0000(x1, 0dB)~0x0FFF_FFFF(x2, +6dB)
LD3_G	ld3_gain[31:0]	RW	0x4000_0000	loudness gain of BQ3, only positive. 0x0000_0000(-inf)~0x0800_0000(x1, 0dB)~0x0FFF_FFFF(x2, +6dB)

Addr 0x5D: SPEQ_ATK_REL_TC_1

Bit	143	142:120	119	118:96	95	94:72	71	70:48	47	46:24	23	22:0
Name	X	SPEQ5	X	SPEQ4	X	SPEQ3	X	SPEQ2	X	SPEQ1	X	SPEQ0

Name	Label	Type	Default	Description
SPEQ0AT	speq0_atk_tc[22:0]	RW	23'h000_800	Attack time control
SPEQ1AT	speq1_atk_tc[22:0]	RW	23'h000_800	Attack time control
SPEQ2AT	speq2_atk_tc[22:0]	RW	23'h000_800	Attack time control
SPEQ3AT	speq3_atk_tc[22:0]	RW	23'h000_800	Attack time control
SPEQ4AT	speq3_atk_tc[22:0]	RW	23'h000_800	Attack time control
SPEQ5AT	speq3_atk_tc[22:0]	RW	23'h000_800	Attack time control

Addr 0x5E: SPEQ_ATK_REL_TC_2

Bit	143	142:120	119	118:96	95	94:72	71	70:48	47	46:24	23	22:0
Name	X	SPEQ5	X	SPEQ4	X	SPEQ3	X	SPEQ2	X	SPEQ1	X	SPEQ0

Name	Label	Type	Default	Description
SPEQ0RT	speq0_rel_tc[22:0]	RW	23'h7FF800	Release time control
SPEQ1RT	speq1_rel_tc[22:0]	RW	23'h7FF800	Release time control
SPEQ2RT	speq2_rel_tc[22:0]	RW	23'h7FF800	Release time control
SPEQ3RT	speq3_rel_tc[22:0]	RW	23'h7FF800	Release time control
SPEQ4RT	speq3_rel_tc[22:0]	RW	23'h7FF800	Release time control
SPEQ5RT	speq3_rel_tc[22:0]	RW	23'h7FF800	Release time control

Addr 0x5F: ch12_mixer_gain

Bit	31	30	29:24	23	22	21:16	15	14	13:8	7	6	5:0
Name	X	P11	G11	X	P12	G12	X	P21	G21	X	P22	G22

Name	Label	Type	Default	Description
G22	ch2_mixer_fch2_gain [5:0]	RW	6'h27	Refer to mixer gain table
P22	ch2_mixer_fch2_polarity	RW	1'b0	1'b0: plus 1'b1: minus
G21	ch2_mixer_fch1_gain [5:0]	RW	6'h00	Refer to mixer gain table
P21	ch2_mixer_fch1_polarity	RW	1'b0	1'b0: plus 1'b1: minus
G12	ch1_mixer_fch2_gain [5:0]	RW	6'h00	Refer to mixer gain table
P12	ch1_mixer_fch2_polarity	RW	1'b0	1'b0: plus 1'b1: minus
G11	ch1_mixer_fch1_gain [5:0]	RW	6'h27	Refer to mixer gain table
P11	ch1_mixer_fch1_polarity	RW	1'b0	1'b0: plus 1'b1: minus

Addr 0x60: DRC Control

Bit	31:25	24	23:12	11	10:9	8	7:4	3	2	1	0
Name	X	DDM	X	DCO	DCM	EM	X	LLE	MLE	HLE	PLE

Name	Label	Type	Default	Description
PLE	drc4_lmt_en	RW	1'b0	0:disable 1: enable
HLE	drc3_lmt_en	RW	1'b0	0:disable 1: enable
MLE	drc2_lmt_en	RW	1'b0	0:disable 1: enable
LLE	drc1_lmt_en	RW	1'b0	0:disable 1: enable
EM	envlp_mode	RW	1'b0	Envelope detection method selection. 0: classic method, 1: new method.
DCM	drc_crossover_mode[1:0]	RW	2'b00	DRC crossover filter mode selection. 2'b00: tree mode 2'b01: sum mode. 2'b10: seperated mode 2'b11: reserved
DCO	drc_crossover_order	RW	1'b0	1'b0: low order 1'b1: high order
DDM	drc_det_method	RW	1'b1	1'b0: envelope 1'b1: rms

Addr 0x61/64/67: DRCxLMT_CFG1(x=1,2,3)

Bit	23:22	21:12	11:10	9:0
Name	X	MGx	X	THx

Name	Label	Type	Default	Description
THx	drcx_lmt_thr[9:0]	RW	10'h30C	DRC limit threshold, 10'h000(-97.5dB)~10'h3FC(30dB), step is 0.125dB 10'h30C = 0dB, 10'h3FC = 30dB
MGx	drcx_makeup[9:0]	RW	10'h3CC	Gain control of DRC band. 10'h000(-121.5dB)~10'h3FC(6dB), step is 0.125dB 10'h3FC = 6dB, 10'h3CC = 0dB

Addr 0x6A: DRC4_LMT_CFG1

Bit	23:10	9:0
Name	X	PTH

Name	Label	Type	Default	Description
PTH	drc4_lmt_thr[9:0]	RW	10'h30C	DRC limit threshold, 10'h000(-97.5dB)~10'h3FC(30dB), step is 0.125dB 10'h30C = 0dB, 10'h3FC = 30dB

Addr 0x62/65/68/6B: DRCx_LMT_CFG2(x=1,2,3,4)

Bit	23	22:0
Name	X	ATx

Name	Label	Type	Default	Description
ATx	drcx_lmt_atk_tc[[22:0]	RW	23'h06_0F83	Attack time control

Addr 0x63/66/69/6C: DRCx_LMT_CFG3(x=1,2,3,4)

Bit	23	22:0
Name	X	RTx

Name	Label	Type	Default	Description
RTx	drc1_lmt_rel_tc[22:0]	RW	24'h00_0122	Release time control

Addr 0x6D: drc_envlp_tc_up

Bit	23	22:0
Name	X	DETU

Name	Label	Type	Default	Description
DETU	drc_envlp_tc_up[22:0]	RW	23'h01_0000	The attack coefficient of drc signal level envelop detection

Addr 0x6E: drc_envlp_tc_dn

Bit	23	22:0
Name	X	DETD

Name	Label	Type	Default	Description
DETD	drc_envlp_tc_dn[22:0]	RW	23'h7B_ 0000	The release coefficient of drc signal level envelop detection

Addr 0x6F: auto mute threshold

Bit	15:0
Name	AM_TH

Name	Label	Type	Default	Description
AM_TH	dsp_amute_thr[15:0]	RW	16'h00	

Addr 0x71: PLL Status

Bit	31	30	29	28	27:20	19	18:8	7	6:4	3:2	1:0
Name	SRSE	SRS	PP	PPP	PRP	X	PFP	X	PCP	PRP	PVIP

Name	Label	Type	Default	Description
PVIP	pllc_vco_i_pll[1:0]	RW	2'b01	pll vco setting
PRP	pllc_rz_pll[1:0]	RW	2'b11	pll resistor setting
PCP	pllc_cp_pll[2:0]	RW	3'b010	pll charge pump setting
PFP	pllc_fbdiv_pll[10:0]	RW	11'h300	pll feedback divider, 1~1023
PRP	pllc_refdiv_pll[7:0]	RW	8'h06	pll referrence divider, 1~255
PPP	pllc_pll_prog	RW	1'b0	1'b0:pllc_pll_prog, they would be auto controlled. 1'b1:pllc_pll_prog, all pll reference value would use register control : 1) refdiv 2) fbdiv 3) rz_pll 4) cp_pll 5) vco_i_pll 6) d2a_ref_sel_osc
PP	pllc_pllclksel	RW	1'b0	1'b0:pllc_pllclksel, pll refer_clk select OSC 1'b1:pllc_pllclksel, pll refer_clk select SCLK
SRS	sw_refclk_sel	RW	1'b0	1'b0:sw_refclk_sel : select OSC_CLK 1'b1:sw_refclk_sel : select SCLK
SRSE	sw_refclk_sel_en	RW	1'b0	1'b0:sw_refclk_sel_disable 1'b1:sw_refclk_sel_enbale

Addr 0x72: PLL Control Register

Bit	15:13	12	11	10:1	0
Name	X	PES	PME	X	POFE

Name	Label	Type	Default	Description
POFE	pll_osc_force_en	RW	1'b0	1'b0: pll reference clock is sclk, if no sclk apply pll will not start; 1'b1: when no sclk, force pll power up ,using osc clk as refercnce clock
PME	pll_manual_en	RW	1'b0	1'b0:pll manual disable 1'b1:pll manual enable
PES	pll_enable_sel	RW	1'b0	1'b0: select auto control : hardware control 1'b1:pll_enable_sel, select register control : pll manual enable

Addr 0x73: SPK Sequence Bypass

Bit	7	6	5	4	3	2	1	0
Name	X					PAMD	C2SB1	C1SB1

Name	Label	Type	Default	Description
C1SB1	ch1_seq_bypass_1ms	RW	1'b0	1'b0:channel 1 spk_state bypass disable 1'b1:channel 1 spk_state bypass, (not wait 1ms)
C2SB1	ch2_seq_bypass_1ms	RW	1'b0	1'b0:channel 2 spk_state bypass disable 1'b1:channel 2 spk_state bypass (not wait 1ms)
PAMD	pwm_automute_dis	RW	1'b0	1'b0: pwm auto mute enable 1'b1: pwm auto mute disable

Addr 0x76: protection system control

Bit	7	6	5	4	3	2	1	0
Name	X			PRE	SPE	OTPE	OCPE	AUPE

Name	Label	Type	Default	Description
AUPE	avdd_uv_protect_en	RW	1'b1	1'b0: disable; 1'b1: enable.
OCPE	oc_protect_en	RW	1'b1	1'b0: disable; 1'b1: enable.
OTPE	otuv_protect_en	RW	1'b1	1'b0: disable; 1'b1: enable.
SPE	short_protect_en	RW	1'b1	1'b0: disable; 1'b1: enable.
PRE	poweron_retry_en	RW	1'b1	1'b0: disable; 1'b1: enable.

Addr 0x78: HARD_CLIPPER_THR

Bit	23:0
Name	HCTH

Name	Label	Type	Default	Description
HCTH	hard_clipper_thr[23:0]	RW	24'h7FF_ FFF	Hard clipper threshold. Default 24'h7FF_FFF.

Addr 0x80: Dsp_3d_coef

Bit	23:0
Name	3DCOEF

Name	Label	Type	Default	Description
3DCOEF	dsp_3d_coef[23:0]	RW	0x400000	3D coefficient, linear gain. 2's complement, 0(-inf) ~ 0x7FFFFF(2), 0x800000(-2) ~0xFFFFFF(near -0), 0x400000 =1, 0x7FFFFF = 2, 0xc00000 = -1.

Addr 0x81: Dsp_3d_mix

Bit	23:0
Name	3DMIX

Name	Label	Type	Default	Description
3DMIX	dsp_3d_mix[23:0]	RW	0x400000	3D mix gain, linear gain. 2's complement, 0(-inf) ~ 0x7FFFFF(2), 0x800000(-2) ~0xFFFFFF(near -0), 0x400000 =1, 0x7FFFFF = 2, 0xc00000 = -1.

Addr 0x82: Inter Private register

Bit	31:8	7	6	5	4	3:1	0
Name	X	RSRE	SEE	LEE	RSEE	X	SSE

Name	Label	Type	Default	Description
SSE	spk_scdet_en	RW	1'b0	1'b0: spk_scdet_en, enable All channel should be set Binary mode 1'b1: pwm_outA = pwm_outB = CH1_P_SIDE pwm_outC = pwm_outD = CH2_P_SIDE
RSEE	refclk_stop_err_en	RW	1'b1	1'b0: sclk_stop will not be judged a clock error 1'b1: sclk stop will be judged a clock error
LEE	lrclk_err_en	RW	1'b1	1'b0: lr_clk_error disable 1'b1: lr_clk_error enable
SEE	sclk_err_en	RW	1'b1	1'b0: sclk error disable 1'b1: sclk error enable
RSRE	refclk_stop_reg_en	RW	1'b1	1'b0: sclk_stop disable , would not shown in 0x02 (bit[7]) 1'b1: sclk_stop enable, would show in 0x02(bit[7])

Addr 0x85: OC Detect Window Width

Bit	31:10	9	8	7:6	5:0
Name	X	OTE	OMS	X	OWW

Name	Label	Type	Default	Description
OWW	ocdet_wind_width[5:0]	RW	6'h06	ocdet_wind_width
OMS	ocdet_mannual_sel	RW	1'b0	ocdet_mannual_sel
OTE	ocfast_trig_en	RW	1'b0	oc fast trigger

Addr 0x86: Fault Over Current Threshold

Bit	31:15	14:12	11:9	8:0
Name	X	FD	X	OEN

Name	Label	Type	Default	Description
OEN	ocdet_en_num[8:0]	RW	9'h006	Threshold of total cycles that "fault_oc" be counted in large detect window. A counted number over the threshold will trigger an oc fault
FD	filter_deglitch[2:0]	RW	3'b010	Deglitch all the fault_oc signal pulse if its width is smaller than this configured cycle number

Addr 0x89: Error Status

Bit	7	6	5	4	3	2	1	0
Name	X				PNEC1	PPEC1	PNEC2	PPEC2

Name	Label	Type	Default	Description
PPEC2	pwm_pdc_err_ch2	R		1'b1: channel 2 has an p-side DC error; 1'b0: no such error;
PNEC2	pwm_ndc_err_ch2	R		1'b1: channel 2 has an n-side DC error; 1'b0: no such error;
PPEC1	pwm_pdc_err_ch1	R		1'b1: channel 1 has an p-side DC error; 1'b0: no such error;
PNEC1	pwm_ndc_err_ch1	R		1'b1: channel 1 has an n-side DC error; 1'b0: no such error;

Addr 0x8B: DSP Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	X						3D_en	HC_en

Name	Label	Type	Default	Description
HC_en	hard_clipper_en	RW	1'b0	Hard clipper enable. 1'b0: disable 1'b1: enable
3D_en	3d_en	RW	1'b0	3d enable: 1'b0:disable 1'b1:enable

Addr 0x8E: drc1_envlp_tc_up

Bit	23	22:0
Name	X	LETU

Name	Label	Type	Default	Description
LETU	drc1_envlp_tc_up[22:0]	RW	23'h01_0000	The attack coefficient of drc signal level envelop detection

Addr 0x8F: drc1_envlp_tc_dn

Bit	23	22:0
Name	X	LETD

Name	Label	Type	Default	Description
LETD	drc1_envlp_tc_dn[22:0]	RW	23'h7B_0000	The release coefficient of drc signal level envelop detection

Addr 0x90: drc2_envlp_tc_up

Bit	23	22:0
Name	X	METU

Name	Label	Type	Default	Description
METU	drc2_envlp_tc_up[22:0]	RW	23'h01_0000	The attack coefficient of drc signal level envelop detection

Addr 0x91: drc2_envlp_tc_dn

Bit	23	22:0
Name	X	METD

Name	Label	Type	Default	Description
METD	drc2_envlp_tc_dn[22:0]	RW	23'h7B_0000	The release coefficient of drc signal level envelop detection

Addr 0x92: drc3_envlp_tc_up

Bit	23	22:0
Name	X	HETU

Name	Label	Type	Default	Description
HETU	drc3_envlp_tc_up[22:0]	RW	23'h01_0000	The attack coefficient of drc signal level envelop detection

Addr 0x93: drc3_envlp_tc_dn

Bit	23	22:0
Name	X	HETD

Name	Label	Type	Default	Description
HETD	drc3_envlp_tc_dn[22:0]	RW	23'h7B_0000	The release coefficient of drc signal level envelop detection

Addr 0x94: PWM MUX register

Bit	31:21	20	19	18	17	16	15:5	4	3:1	0
Name	X	PCT[4]	PCT[3]	PCT[2]	PCT[1]	PCT[0]	X	PE	X	PNZ

Name	Label	Type	Default	Description
PNZ	pwm_ns_zr	RW	1'b0	1'b0: normal 1'b1: add zero to fs/2 to desrease high frequency noise
PE	pwm_evenbit	RW	1'b0	1: quantize, input data even, tri-mode, (10bit, {[23,15],1'b0}). quantize, input data even, bin-mode (9 bit ,{[23:16],2'b0}) 0: quantize, input data not even, tri-mode, (10bit, {[23,14]}). quantize, input data not even, bin-mode (9 bit ,{[23:15],1'b0})
PCT[0]	pwm_connection_test[0]	RW	1'b0	1'b0: pwm_out_a = 0 1'b1: control pwm_out_a in case of pwm_conection enable, used to test analog connection. pwm_out_a = 1
PCT[1]	pwm_connection_test[1]	RW	1'b0	1'b0: pwm_out_b = 0 1'b1: pwm_out_b = 1
PCT[2]	pwm_connection_test[2]	RW	1'b0	1'b0: pwm_out_c= 0 1'b1: pwm_out_c= 1
PCT[3]	pwm_connection_test[3]	RW	1'b0	1'b0: pwm_out_d= 0 1'b1: pwm_out_d= 1
PCT[4]	pwm_connection_test[4]	RW	1'b0	1'b0: pwm connection test disable 1'b1: pwm_connection test enable

Addr 0x95: PWM Outflip register

Bit	31	30:24	23:22	21	20	19:17	16	15	14;12	11	10:8	7	6:4	3	2:0
Name	X	PDRP	X	PCM	PAME	X	POR[12]	X	POR[11:9]	X	POR[8:6]	X	POR[5:3]	X	POR[2:0]

Name	Label	Type	Default	Description
POR[2:0]	pwm_outflip_reg[2:0]	RW	3'b000	3'b000: pwm_outflip[2:0]: pwm_outa = side1_p 3'b001: pwm_outflip[2:0]: pwm_outa = side1_n 3'b010: pwm_outflip[2:0]: pwm_outa = side2_p 3'b011: pwm_outflip[2:0]: pwm_outa = side2_n others: reserved
POR[5:3]	pwm_outflip_reg[5:3]	RW	3'b001	3'b000: pwm_outflip[5:3]: pwm_outb = side1_p 3'b001: pwm_outflip[5:3]: pwm_outb = side1_n 3'b010: pwm_outflip[5:3]: pwm_outb = side2_p 3'b011: pwm_outflip[5:3]: pwm_outb = side2_n others: reserved
POR[8:6]	pwm_outflip_reg[8:6]	RW	3'b010	3'b000: pwm_outflip[7:6]: pwm_outc = side1_p 3'b001: pwm_outflip[7:6]: pwm_outc = side1_n 3'b010: pwm_outflip[7:6]: pwm_outc = side2_p 3'b011: pwm_outflip[7:6]: pwm_outc = side2_n others: reserved
POR[11:9]	pwm_outflip_reg[11:9]	RW	3'b011	3'b000: pwm_outflip[11:9]: pwm_outd = side1_p 3'b001: pwm_outflip[11:9]: pwm_outd = side1_n 3'b010: pwm_outflip[11:9]: pwm_outd = side2_p 3'b011: pwm_outflip[11:9]: pwm_outd = side2_n others: reserved
POR[12]	pwm_outflip_reg[12]	RW	1'b0	1'b0: pwm_outflip[12] disable 1'b1: pwm outflip[12] enable
PAME	pwm_ad_mode_en	RW	1'b0	1'b0: tri-mode 1'b1: binary mode
PCM	pwm_clip_mode	RW	1'b0	1'b0: trunck to 0 1'b1: clip to pwm_mod_limt[2:0]
PDRP	pwm_dval_ramp_point [6:0]	RW	7'h40	Start point to decrease the pwm compensation pulse

Addr 0x96: PWM Outflip register

Bit	31:29	28:27	26	25	24	23	22	21	20:16	15:8	7:0
Name	X	PNO	PNBC	PR	P7	PDC	PDE	PDR	PDP	PCDS	PCDV

Name	Label	Type	Default	Description
PCDV	pwm_cnvt_dvalue[7:0]	RW	8'h2F	pwm_cnvt_dvalue [7:0], differential value
PCDS	pwm_cnvt_dstep[7:0]	RW	8'h00	pwm_cnvt_dstep[7:0], differential step value,
PDP	pwm_dither_pos[4:0]	RW	5'h00	5'd0: shift the dither[23:0] to right 0 bit, and complementary "0" 5'd1: shift to right 0 bit 5'd2: shift to right 0 bit 5'd3: shift to right 1 bit 5'd4: shift to right 2 bit 5'd5: shift to right 3 bit 5'dx: pwm_dither_pos[4:0], shift the dither to where the lsb of the quantizer will be. (shift to right (x-2) bits) 5'd18: shift to right 16 bit 5'd19: shift to right 17 bit others: shift 0 bit
PDR	pwm_dither_range	RW	1'b0	1'b0: pwm_dither_range, -3 to 3 1'b1: pwm_dither_range, -1 to 1
PDE	pwm_dither_en	RW	1'b0	1'b0: pwm_dither_en, disable dither 1'b1: pwm_dither_en, enable dither
PDC	pwm_dither_clr	RW	1'b0	1'b0: pwm_dither_clr 1'b1: pwm_dither_clr, clear dither module generate a triangular
P7	pwm_768x	RW	1'b0	pwm modulation frequency select. 1'b0: 384khz 1'b1: 768khz
PR	pwm_roundup	RW	1'b0	1'b0: pwm_roundup, quantize to 9 or 10 bits, truncate 1'b1: pwm_roundup, quantize to 9 or 10 bits, roundup
PNBC	pwm_ns_bf_clr	RW	1'b0	1'b0: pwm_ns_bf_clr 1'b1: pwm_ns_bf_clr, clear noise shaper sate counter
PNO	pwm_ns_order	RW	2'b10	PWM noise shipping order select. 2'b00: 1rst order. 2'b01: 2nd order. 2'b10: 3rd order. 2'b11: 4th order.

Addr 0x97: PM_COEF

Bit	47	46:24	23	22:0
Name	X	PCU	X	PCD

Name	Label	Type	Default	Description
PCD	pm_coef_dn[22:0]	RW	23'h7FF800	Power meter envelop detection release coefficient
PCU	pm_coef_up[22:0]	RW	23'h0008	Power meter envelop detection attack

			00	coefficient

Addr 0x98: Power Meter Control rb1

Bit	23:20	19	18:17	16	15:8	7:2	1:0
Name	X	PDM	PS	PL	PLD[9:2]	X	PLD[1:0]

Name	Label	Type	Default	Description
PLD[1:0]	pm_lvl_db[1:0]	R	2'd0	10'h000 ~ 10'h3fc: -127.875db~0db, step is 0.125db
PLD[9:2]	pm_lvl_db[9:2]	R	8'd0	8'h00 ~ 8'hff: -127.5db~0db, step is 0.5db
PL	pm_loc	RW	1'b0	1'b0: after volume 1'b1: before volume
PS	pm_source[1:0]	RW	2'b00	00: (l+r)/2, 01: left channel, 10: right channel, 11:reserved
PDM	pm_det_method	RW	1'b0	1'b0: envelope 1'b1: rms

Addr 0x99: Power Meter Control rb2

Bit	23	22:0
Name	X	PLL

Name	Label	Type	Default	Description
PLL	pm_lvl_linear[22:0]	R	23'd0	23'h000000 ~ 23'h7fffff: 2^(-23)~1

Addr 0x9A: PBQ checksum

Bit	31:0
Name	PCK

Name	Label	Type	Default	Description
PCK	pbq_checksum_key[31:0]	RW	32'h0000_0000	The reference value of pbq memory checksum result

Addr 0x9B: MDRC checksum

Bit	31:0
Name	MCK

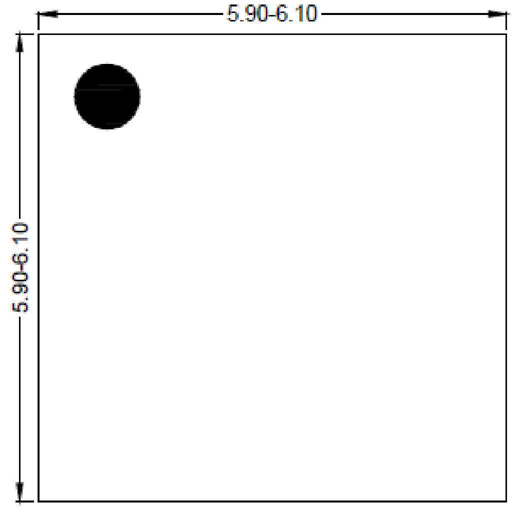
Name	Label	Type	Default	Description
MCK	mdrc_checksum_key[31:0]	RW	32'h4000_0000	The reference value of drc memory checksum result

Addr 0x9C: amute threshold

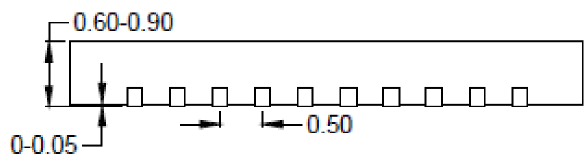
Bit	31:0
Name	PC2CK

Name	Label	Type	Default	Description
PC2CK	mdrc_checksum_key[31:0]	RW	32'h0000_0000	The reference value of drc memory checksum result

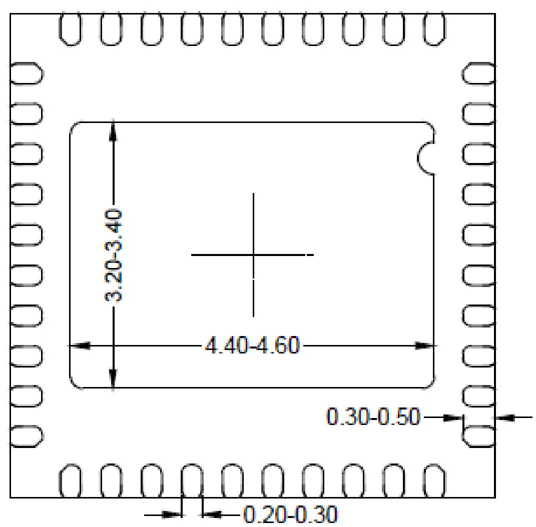
QFN6×6-40 Package Outline



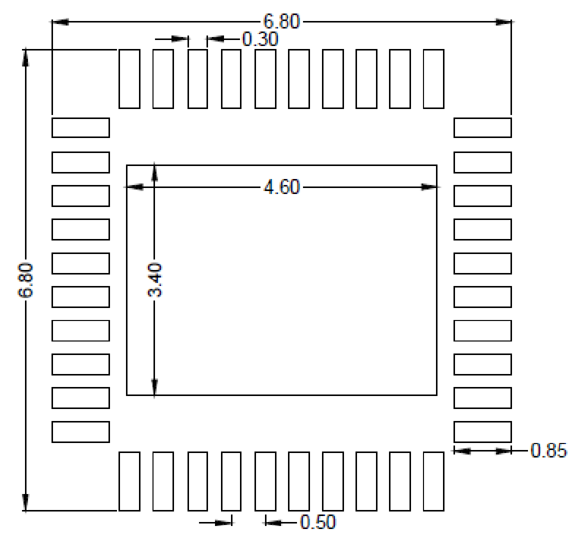
Top view



Side view



Bottom View



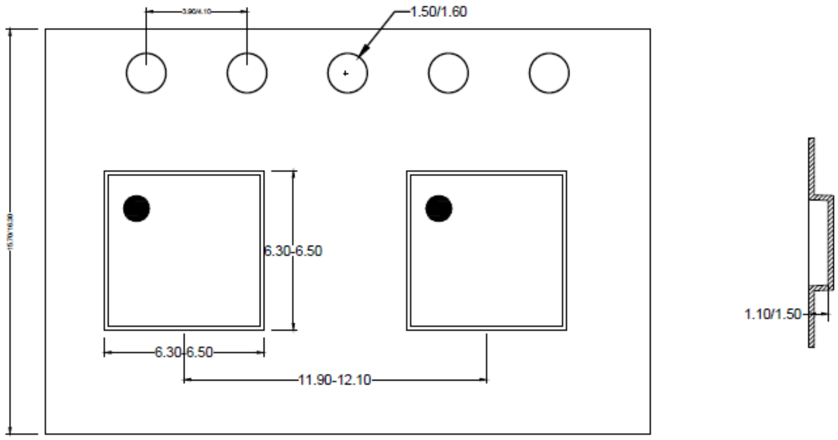
Recommended PCB Layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

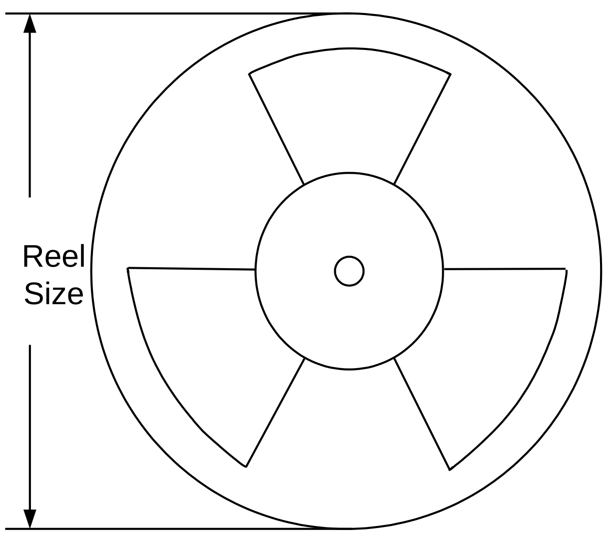
1. Taping orientation

QFN6×6



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN6×6	16	12	13"	400	400	2500

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 9, 2024	Revision 1.0	Production Release
Jun 9, 2023	Revision 0.9C	Change the maximum spec of Trs/Tfs of I2C timing from 8ns to 1/8 SCLK period. (Page 13)
July 27, 2021	Revision 0.9B	1. Modify the max value of Enable I^2C duration time from 12.0 to 0.1 in page 12 2. Update Addr 0x96: PWM Outflip register 3. 0x6F delete the bit 23:16 4. 0x82 bit 4 refclk_stop_err_en resigter type is changed from "R" to "RW"
Mar.11, 2021	Revision 0.9A	1. Delete single filter in Feature 2. Delete the description of BD or Ternary mode support 3. Delete the Block in the description of DRC
Oct. 15, 2019	Revision 0.9	Initial Release

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