

Features

- Transient protection for high-speed data lines
IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (Air)
 $\pm 30\text{kV}$ (Contact)
IEC 61000-4-5 (Surge) 7.5A (8/20 μs)
- Small package (2.9mm \times 2.4mm \times 1.0mm)
- Protects two data lines
- Low capacitance: 1.2pF Typical (I/O-GND)
- Low leakage current: 0.01 μA @ V_{RWM} (Typical)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for $\pm 8\text{kV}$ contact discharge

Description

SYT04L05AWC is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 1.2pF only, SYT04L05AWC is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD) ($\pm 30\text{kV}$ air, $\pm 30\text{kV}$ contact discharge), IEC 61000-4-5 (Surge) (7.5A, 8/20 μs), etc.

SYT04L05AWC uses small SOT-143 package. Each SYT04L05AWC device can protect two high-speed data lines. The combined features of low capacitance, small size and high ESD robustness make SYT04L05AWC ideal for high-speed data ports and high-frequency lines (e.g., VGA) applications. The low clamping voltage of the SYT04L05AWC guarantees a minimum stress on the protected IC.

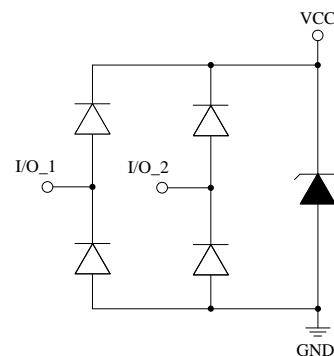
Applications

- Desktops, Servers and Notebooks
- USB2.0 Power and Data Line Protection
- IEEE 1394 Firewire Ports
- Video Graphics Cards
- SIM Ports

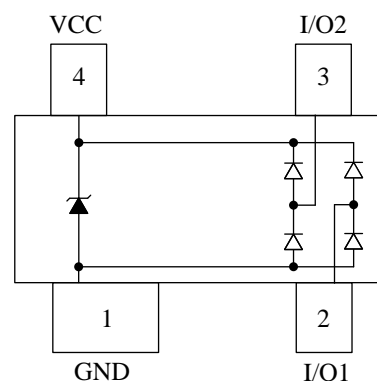
Mechanical Characteristics

- SOT-143 package
- Marking: Device code, Date code
- Packaging: Tape and Reel

Circuit Diagram



Pin Configuration



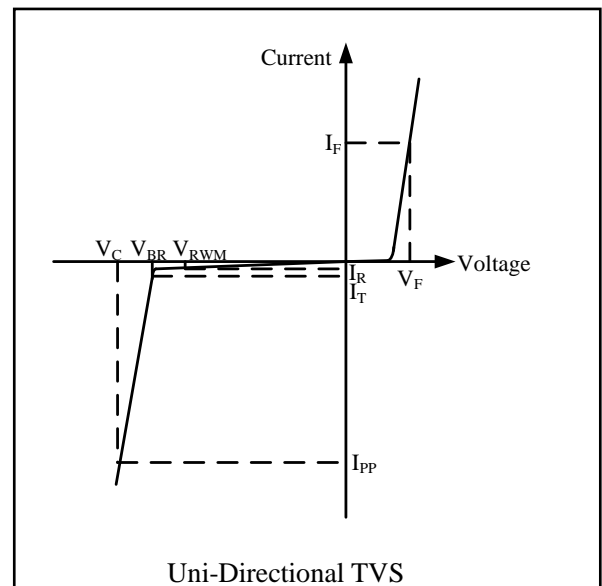
SOT-143
(Top View)

Absolute Maximum Rating

Symbol	Parameter	Value	Units
I_{PP}	Maximum Peak Pulse Current (8/20 μ s)	7.5	A
P_{PK}	Maximum Peak Pulse Power (8/20 μ s)	100	Watts
V_{ESD}	ESD per IEC 61000-4-2 (Air)	± 30	kV
	ESD per IEC 61000-4-2 (Contact)	± 30	
T_{OPT}	Operating Temperature	-40/+125	$^{\circ}$ C
T_{STG}	Storage Temperature	-55/+150	$^{\circ}$ C

Electrical Characteristics ($T_A = 25^{\circ}$ C)

Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Reverse Breakdown Voltage @ I_T
I_T	Test Current for Reverse Breakdown
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Maximum Peak Pulse Current
C_{ESD}	Parasitic Capacitance
V_R	Reverse Voltage
f	Small Signal Frequency
I_F	Forward Current
V_F	Forward Voltage @ I_F



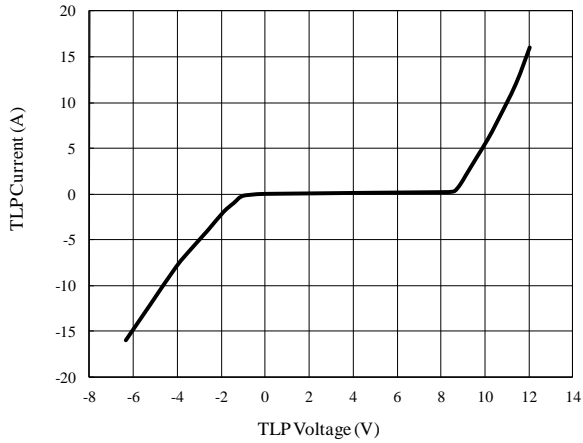
Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				5.0	V
I_R	$V_{RWM} = 5V, T_A = 25^{\circ}C$ From I/O to GND		0.01	0.1	μ A
V_{BR}	$I_T = 1mA$ From I/O to GND	6.0	8.0	10.0	V
V_F	$I_F = 1mA$ From GND to I/O	0.4	0.7	1.2	V
V_C^1	$I_{PP} = 7.5A, t_p = 8/20\mu s$ From I/O to GND		12.5	13.5	V
V_C^1	$I_{PP} = 16A, t_p = 10/100ns$ From I/O to GND		12		V
$R_{DYN}^{1,2}$	$t_p = 10/100ns$ From I/O to GND		0.25		Ω
C_{ESD}^1	$V_R = 2.5V, f = 1MHz$ From I/O to GND		1.20	1.50	pF
C_{ESD}^1	$V_R = 2.5V, f = 1MHz$ Between I/O and I/O		0.60	0.75	pF

NOTES

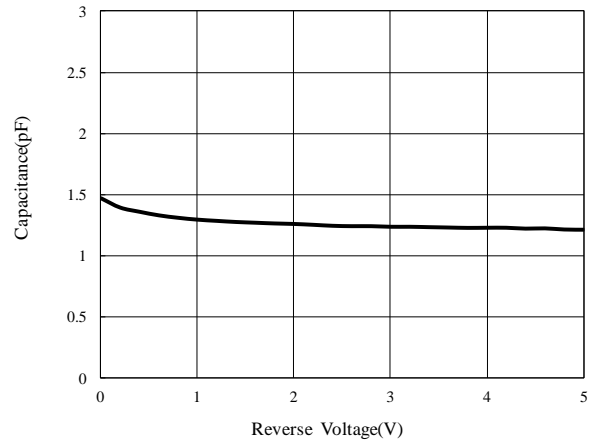
¹Guaranteed by design and not subject to production test.

² R_{DYN} calculated based on $I_{PP}=8A$ to $I_{PP}=16A, t_p = 10/100ns$.

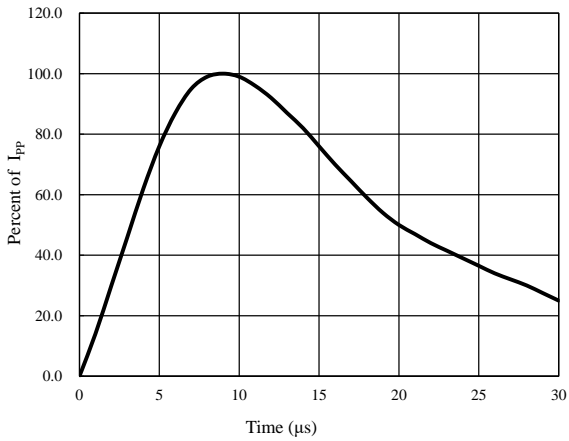
TLP Sweeping of I/O to GND



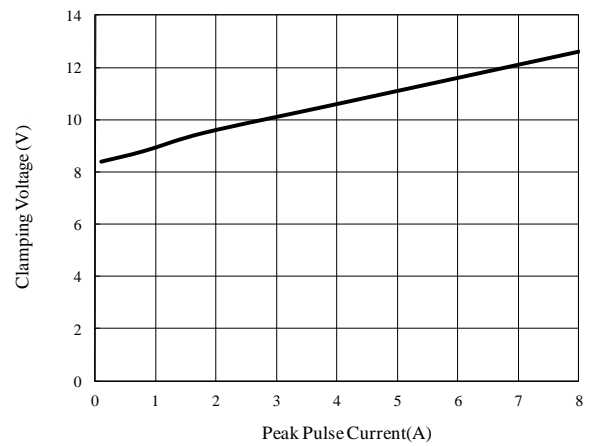
Capacitance vs. Voltage



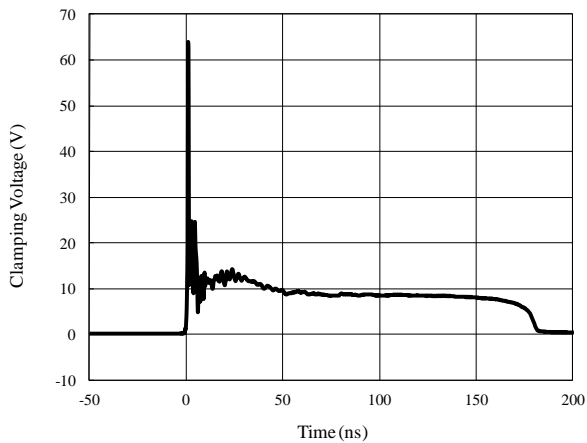
Pulse Waveform



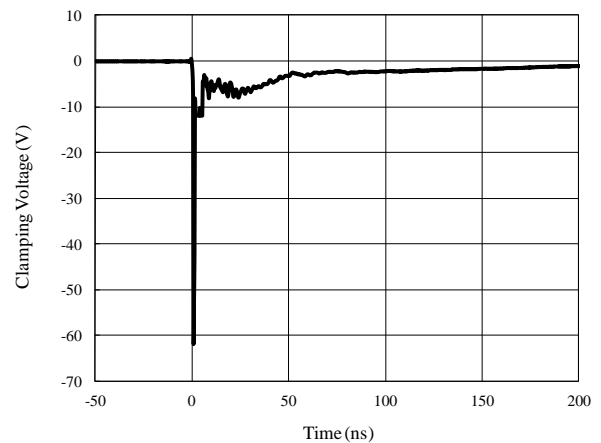
Clamping Voltage vs. Peak Pulse Current



**ESD Clamping of I/O to GND
(+8kV Contact per IEC 61000-4-2)**



**ESD Clamping of I/O to GND
(-8kV Contact per IEC 61000-4-2)**



Application Information

Pin Connection in PCB

SYT04L05AWC is capable to provide ESD protection for two data lines simultaneously. The pin connection is shown in Figure 1.

Two parallel data lines, from inner IC to I/O port connector, could connect to SYT04L05AWC two I/O pins directly. Pin 1 of SYT04L05AWC is the negative reference pin, which should connect to the GND of PCB. The connection wires should be as short as possible in order to minimize the parasitic inductance.

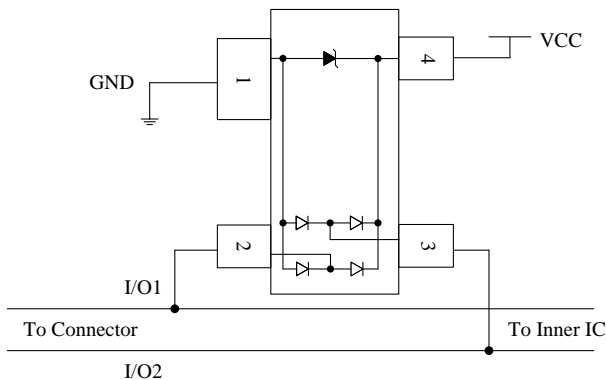


Figure 1 SYT04L05AWC pin connection in PCB

PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- SYT04L05AWC GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting SYT04L05AWC VCC & GND pins to the PCB VCC & GND should be wide.
- Place SYT04L05AWC as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

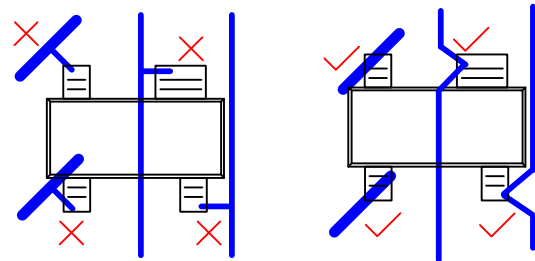
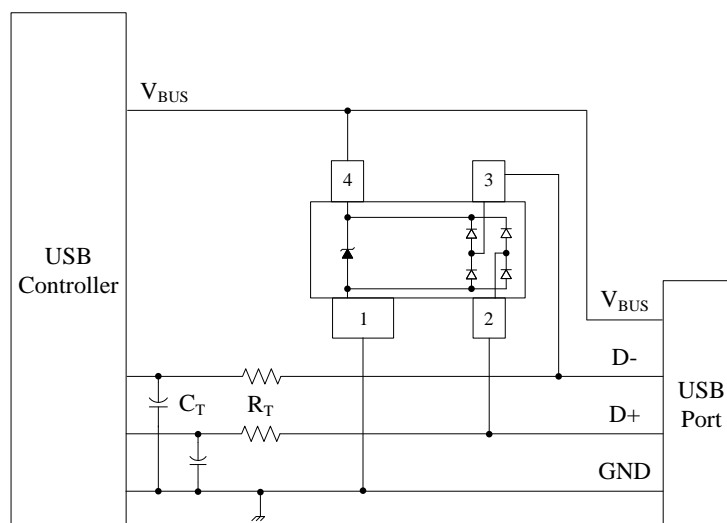


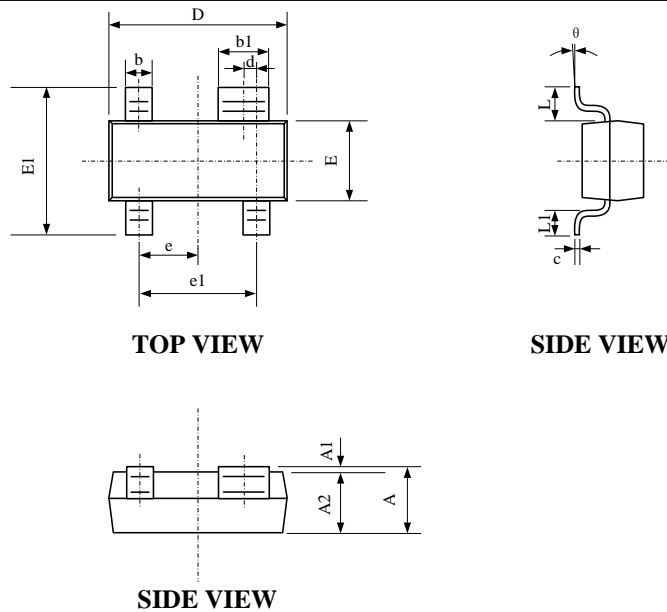
Figure 2 SYT04L05AWC Layout Guideline

Universal Serial Bus ESD Protection



Package Outline

- SOT-143 package

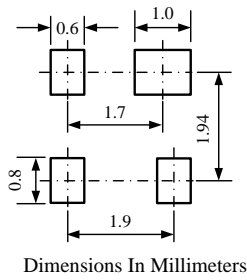


Package Dimensions

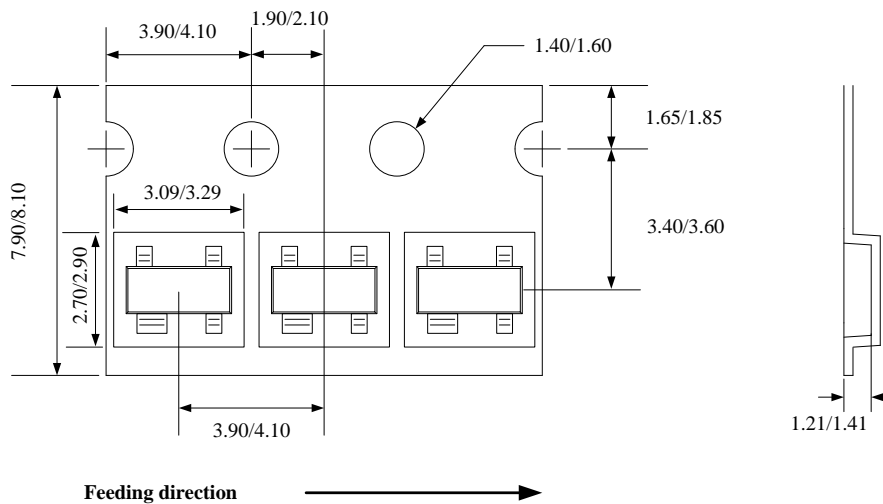
Symbol	Dimensions In Millimeters	
	Minimum	Maximum
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
b	0.300	0.500
b1	0.750	0.900
c	0.080	0.150
d	0.200 TYP.	
e	0.950 TYP.	
e1	1.800	2.000
L	0.550 REF.	
L1	0.300	0.500
θ	0°	8°

Notes: All dimension in millimeter and exclude mold flash & metal burr.

PCB Layout Pattern

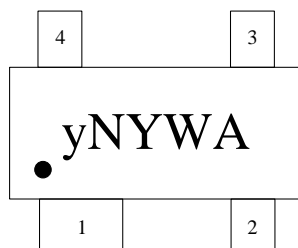


Tape and Reel Specification



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Qty per reel (pcs)
SOT-143	8	4	7"	3000

Marking Codes



Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
SYT04L05AWC	5V	3,000	7 Inch

Note:

- (1) "yN" is device code, fixed.
- (2) "YWA" is date code.



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	08/14/2020	Initial Release	
1.0	08/14/2021	Production Release	



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