SQ24903

2.5V to 18V High Efficiency Power Limiting Hot-swap Controller

General Description

The SQ24903 is an easy-to-use, 2.5V to 18V, hot-swap controller that safely drives an external N-channel MOSFET. The programmable current limit and fault time protect the supply and load from excessive current at startup. After startup, currents above the user-selected limit will be allowed to flow until programmed timeout – except in extreme overload events, the load is immediately disconnected from source. The low, 25mV current sense threshold is highly accurate and allows use of smaller, more efficient sense resistors yielding lower power loss and smaller footprint.

Programmable power limiting ensures the external MOSFET operates inside its safe operating area (SOA) at all times. This allows the use of smaller MOSFETS while improving system reliability. Power good and fault outputs are provided for status monitoring and downstream load control.

Features

- 2.5V to 18V Operation
- Accurate Current Limiting for Startup
- Programmable FET SOA Protection
- Accurate 25mV Current-Sense Threshold
- Power Good Output
- Fast Breaker for Short-Circuit Protection
- Programmable Fault Timer
- Programmable UV Threshold
- RoHS Compliant and Halogen Free
- MSOP-10 Package

Applications

- SSD
- Networking
- DWDM

Ordering Information

SQ24903 □(□ □ □)

- □□□: Package Code
- □: Optional Spec Code

Ordering Number	Package type	Note
SQ24903FBP	MSOP10	----

Typical Application

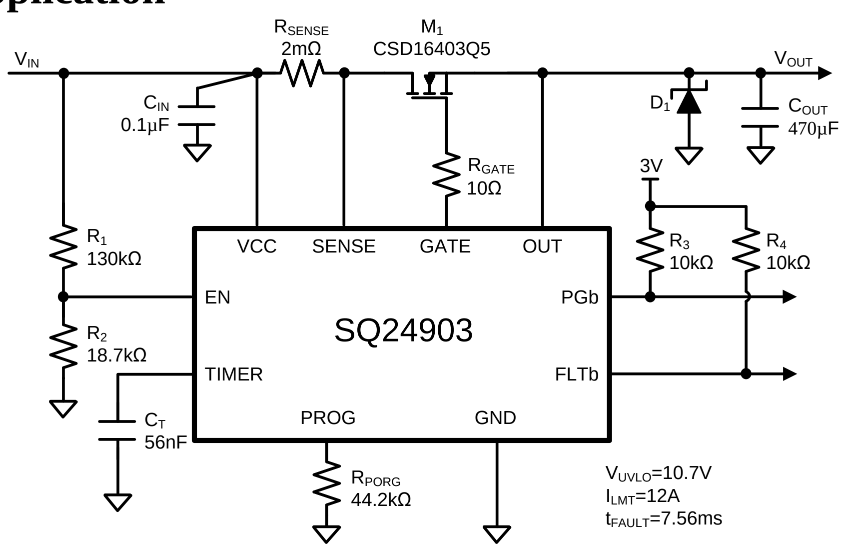
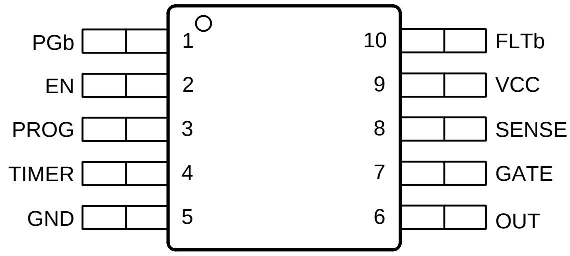


Figure1. Schematic Diagram

Pinout (top view)

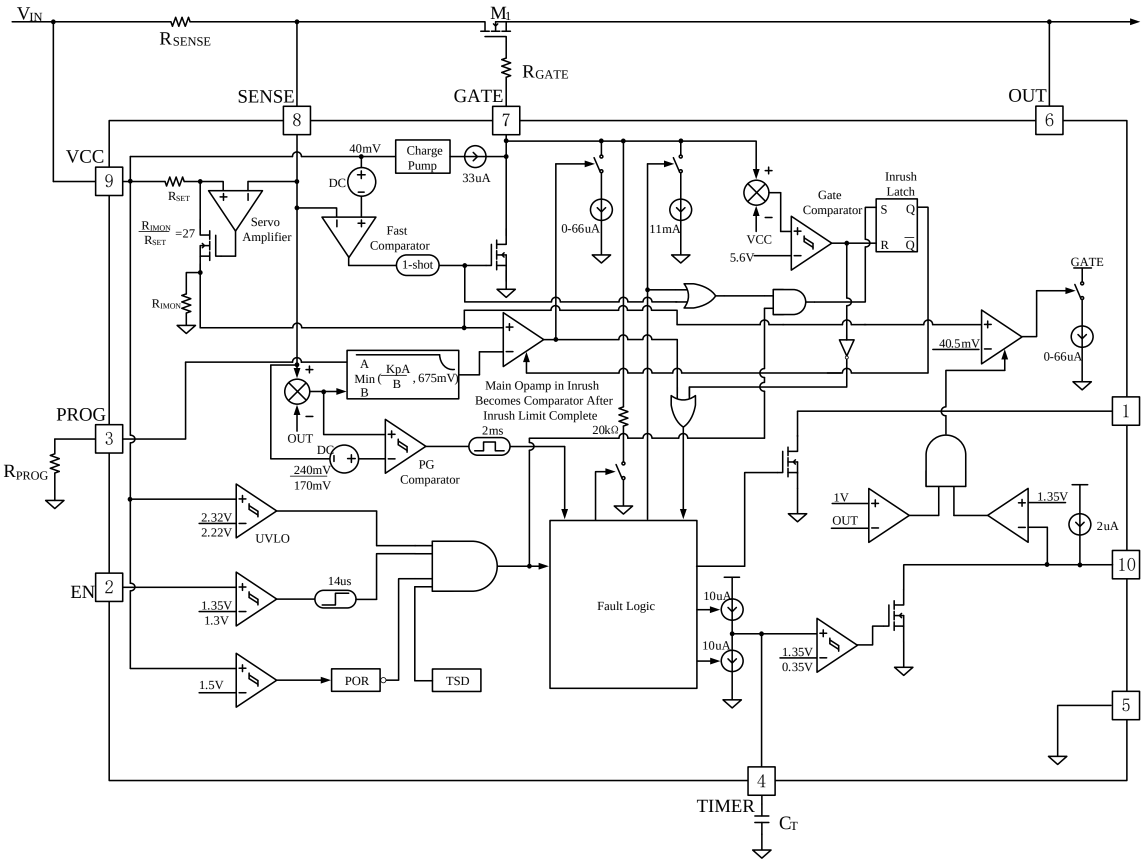


(MSOP10)

Top Mark: **DQH*xyz*** for SQ24903FBP **(**Device code: DQH; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	NO.	TYPE	Pin Description
EN	2	I	Active-high enable input. Logic input. Connects to resistor divider. Do not leave it floating.
FLTb	10	I/O	Active-low, open-drain output indicates overload fault timer has turned MOSFET off. Connect a pull-high resistor to this pin. If FLTb connects to ground through a <100kΩ resistor, IC start up with current limit mode when OUT lower than 1V. If FLTb pin connects a pull-high resistor to OUT pin, the pull-high resistor must be greater than 1.5MΩ. Leave it floating when not used.
GATE	7	O	Gate driver output for external MOSFET. No external resistor should be directly connected from GATE to GND or from GATE to OUT.
GND	5	-	Ground.
OUT	6	I	Output voltage sensor for monitoring MOSFET power.
PGb	1	O	Active-low, open-drain power good indicator. Connect a pull-high resistor. Status is determined by the voltage across the MOSFET. Leave it floating when not used.
PROG	3	I	Power-limiting programming pin. A resistor from this pin to GND sets the maximum power dissipation for the FET. Do not apply a voltage to this pin.
SENSE	8	I	Current sensing input for resistor shunt from VCC to SENSE.
TIMER	4	I/O	A capacitor connected from this pin to GND provides a fault timing function.
VCC	9	I	Input-voltage sense and power supply.

Block Diagram



Absolute Maximum Ratings (Note 1)

EN, FLTb(Note 2), GATE, OUT, PGb(Note 2), SENSE, VCC Voltage ---------------------- –0.3V to 30V
GATE Voltage (t<1ms) -- –0.8V to 30V
OUT Voltage (t<1ms) -- –3V to 30V
PROG(Note2), TIMER Voltage --- –0.3V to 3.6V
SENSE to VCC Voltage --- –0.3V to 0.3V
FLTb, PGb Sink Currents -- 5mA
Power Dissipation, P_D @ T_A = 25°C --- 0.85W
Package Thermal Resistance (Note 3)
θ_{JA} -- 117.56°C/W
θ_{JC} -- 48.4°C/W
Storage Temperature Range -- –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---260°C
Junction Temperature Range -- -40°C to +150°C

Recommended Operating Conditions

SENSE, VCC Voltages -- 2.5V to 18V
EN, FLTb, PGb, OUT Voltages -- 0V to 18V
FLTb, PGb Sink Currents --- 0 to 2mA
PROG Resistance -- 4.99kΩ to 500kΩ
Minimum TIMER External Capacitance --- 1nF
Operating Junction Temperature Range -- –40°C to 125°C
Ambient Temperature Range -- -40°C to 125°C

Electrical Characteristics

(–40°C≤ T_J ≤125°C, V_{CC} = 12V, V_{EN} = 3V, and R_{PROG} = 50kΩ to GND, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.) (Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC						
UVLO Threshold, Rising	$V_{UVLO,R}$		2.15	2.32	2.45	V
UVLO Threshold, Falling	$V_{UVLO,F}$		2.05	2.22	2.35	V
UVLO Hysteresis	$V_{UVLO,HYS}$			0.1		V
Supply Current	I_S	Enabled: $I_{OUT}+I_{VCC}+I_{SENSE}$		1	1.4	mA
		Disabled: EN = 0V, $I_{OUT}+I_{VCC}+I_{SENSE}$		0.45		mA
EN						
Threshold Voltage, Falling	$V_{EN,F}$		1.2	1.3	1.4	V
Hysteresis	$V_{EN,HYS}$			50		mV
Input Leakage Current	$I_{EN,LEAK}$	0V≤V_{EN}≤30V	-1	0	1	uA
FLTb						
Output Low Voltage	$V_{FLTb,LOW}$	Sinking 2mA		0.11	0.25	V
Current Limit Mode Threshold	$V_{FLTb,CLT}$	V_{OUT}=0V, V_{FLTb} rising	1.2	1.35	1.5	V
Sourcing Current	$I_{FLTb,SRC}$		1	2	4	μA
Input Leakage Current	$I_{FLTb,LEAK}$	V_{FLTb}=0V, 30V	-1	0	1	μA
PGb						
Threshold	$V_{PGb,T}$	$V_{(SENSE-OUT)}$ rising, PGb going high	140	240	340	mV
Hysteresis	$V_{PGb,HYS}$	Measured $V_{(SENSE-OUT)}$ falling, PGb going low		70		mV
Output Low Voltage	$V_{PGb,LOW}$	Sinking 2mA		0.11	0.25	V
Input Leakage Current	$I_{PGb,LEAK}$	V_{PGb} = 0V, 30V	-1	0	1	μA
PROG						
Bias Voltage	$V_{PROG,BIAS}$	Sourcing 10μA	0.65	0.678	0.7	V
Input Leakage Current	$I_{PROG,LEAK}$	V_{PROG} = 1.5V	-0.2	0	0.2	μA
TIMER						
Sourcing Current	$I_{TIMER,SRC}$	V_{TIMER} = 0V	8	10	12	μA
Sinking Current	$I_{TIMER,SNC1}$	V_{TIMER} = 1.5V	8	10	12	μA
	$I_{TIMER,SNC2}$	V_{EN} = 0V, V_{TIMER} = 1.5V	2	4.5	8	mA
Upper Threshold Voltage	$V_{TIMER,U}$		1.3	1.35	1.4	V
Lower Threshold Voltage	$V_{TIMER,L}$		0.33	0.35	0.37	V
Timer Activation Voltage	$V_{(GATE-VCC),TIMER}$	Raise GATE until I_{TIMER} sinking, measure $V_{(GATE-VCC)}$, VCC = 12V	4.7	5.6	6.7	V
Bleed-down Resistance	$R_{TIMER,ENSD}$	V_{ENSD} = 0V, V_{TIMER} = 1.5V	70	104	130	kΩ
OUT						
Input Bias Current	I_{OUT}	V_{OUT} = 12V		4	10	μA
Start Current Limit Mode Threshold	$V_{OUT,CLT}$	V_{FLTb}=0V, V_{OUT} rising	0.9	1	1.1	V

GATE						
Output Voltage	V_{GATE}	V_{OUT} = 12V	23.5	25.8	28	V
Clamp Voltage	$V_{(GATE-VCC),CLAMP}$	Inject 10 µA into GATE, measure $V_{(GATE-VCC)}$	12	13.9	15.5	V
Sourcing Current	$I_{GATE,SRC}$	V_{GATE} = 12V	20	33	45	µA
Sinking Current	$I_{GTAE,SNC,FSTOFF}$	Fast turnoff, V_{GATE} = 14V	0.5	1	1.6	A
	$I_{GTAE,ST}$	Sustained, V_{GATE} = 4V to 23V	5	11	20	mA
	$I_{GTAE,SNC,CL}$	In inrush current limit, V_{GATE} = 4V to 17V	15	33	50	µA
Pull-down Resistance (Note 5)	$R_{GATE,TSD}$	Thermal shutdown	10	20	30	kΩ
SENSE						
Input Bias Current	$I_{SENSE,BIAS}$	V_{SENSE} = 12V, sinking current		45	65	µA
Current Limit Threshold	$V_{(VCC-SENSE),CLT1}$	Normal, V_{OUT} = 12V	22.5	25	27.5	mV
	$V_{(VCC-SENSE),CLT2}$	Start, V_{OUT}=0V, V_{FLTb}=0V	0.6	1.5	2.4	mV
Power Limit Threshold	$V_{(VCC-SENSE),PLT}$	V_{OUT} = 7V, R_{PROG} = 50kΩ	10.1	11.6	13.1	mV
		V_{OUT} = 2V, R_{PROG} = 25kΩ	10.1	11.6	13.1	
Fast-trip Threshold	$V_{(VCC-SENSE),FST}$		34.7	40	45.3	mV
OTSD						
Threshold, Rising (Note 5)	T_{SD}		130	150		°C
Hysteresis (Note 5)	$T_{SD,HYS}$			20		°C

Timing Requirements

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN						
Turn Off Time	$t_{EN,OFF}$	EN↓ to V_{GATE} < 1V, C_{GATE} = 33nF	20	60	150	µs
Deglitch Time(Note 5)	$t_{EN,DEGL}$	EN↑	8	14	25	µs
Disable Delay	$t_{EN,DLY}$	EN↓ to GATE↓, C_{GATE} = 0, $t_{pff50-90}$, See Figure 2	0.1	0.4	1.5	µs
PGb						
Delay (Deglitch) Time	$t_{PGb,DLY}$	Rising or falling edge	2	3.4	6	ms
GATE						
Fast-Turn Off Duration	$t_{GATE,FSTOFF}$		8	13.5	18	µs
Turn On Delay	$t_{GATE,ONDLY}$	V_{CC} rising to GATE sourcing, $t_{prr50-50}$, See Figure3		100	250	µs
SENSE						
Fast-Turn Off Duration	$t_{SENSE,FSTOFF}$		8	13.5	18	µs
Fast-Turn Off Delay (Note 5)	$t_{SENSE,FSTDLY}$	$V_{(VCC-SENSE)}$ = 80 mV, C_{GATE} = 0pF, $t_{prf50-50}$, See Figure4		200		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: Do not apply voltages directly to these pins.

Note 3: θ_{JA} is simulated at T_A=25°C on Silergy's demo board.

Note 4: All voltages referenced to GND, unless otherwise noted.

Note 5: This specification is guaranteed by design.

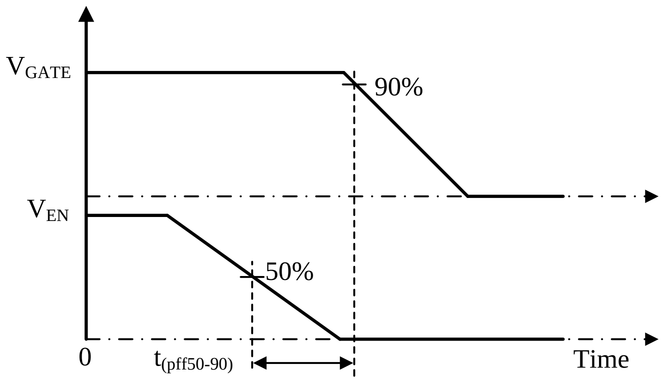


Figure2. $t_{pff50-90}$ Timing Definition

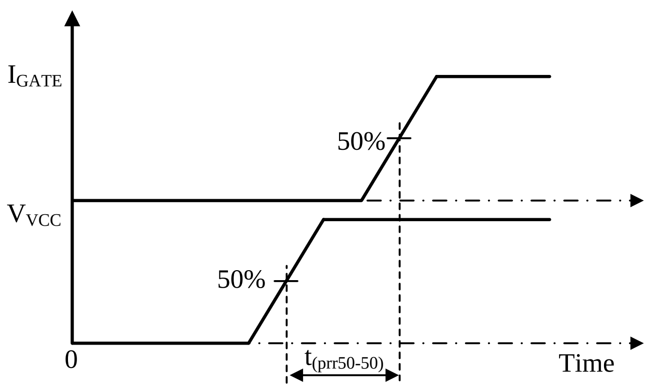


Figure3. $t_{prr50-50}$ Timing Definition

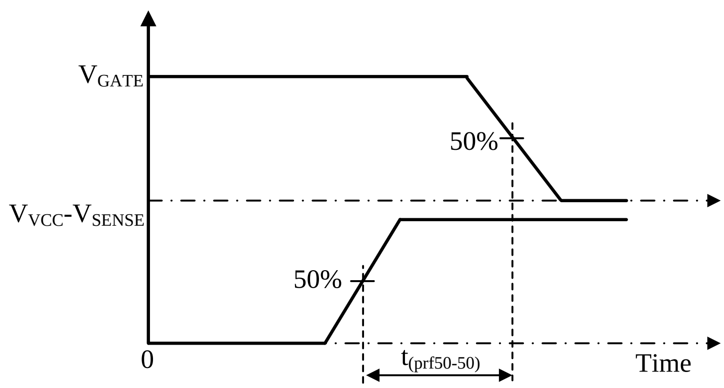
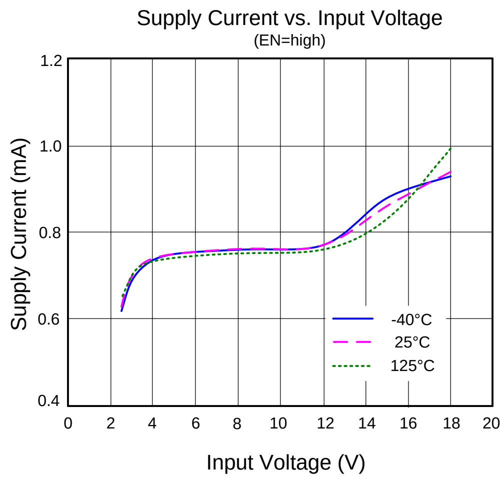
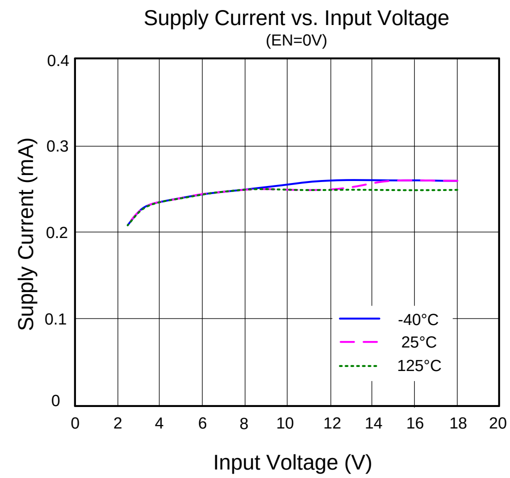
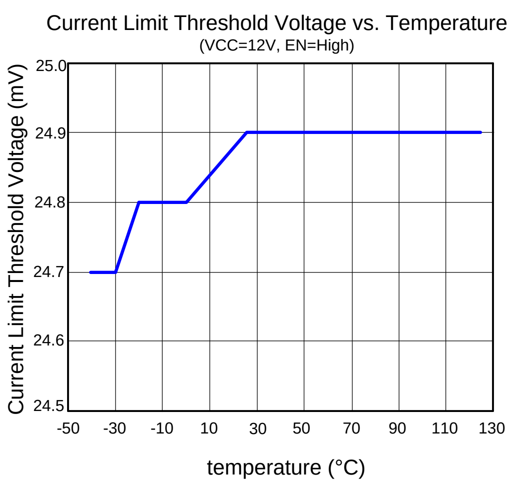


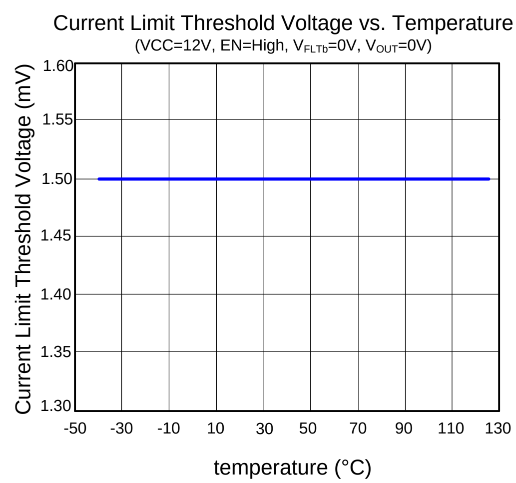
Figure4. $t_{prf50-50}$ Timing Definition

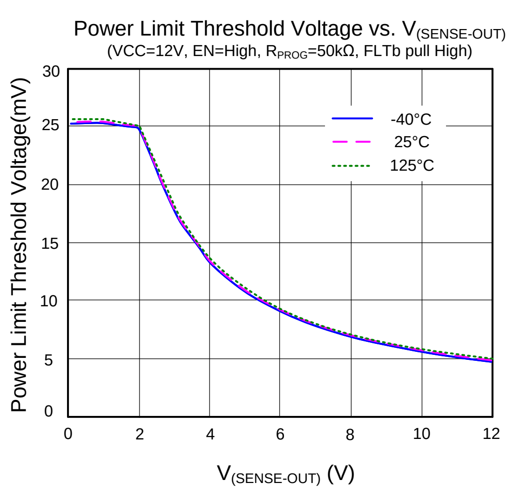
Typical Performance Characteristics

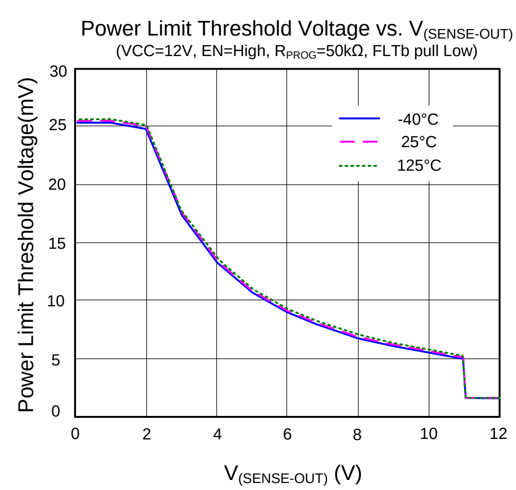




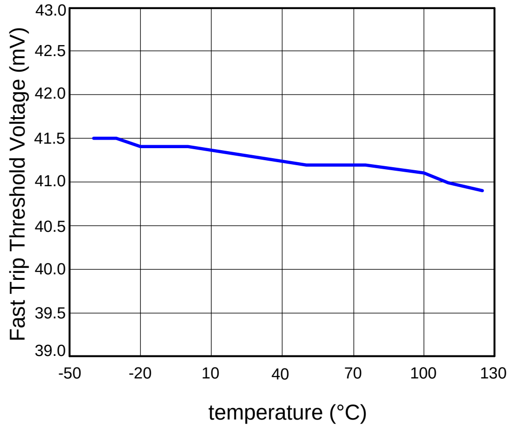




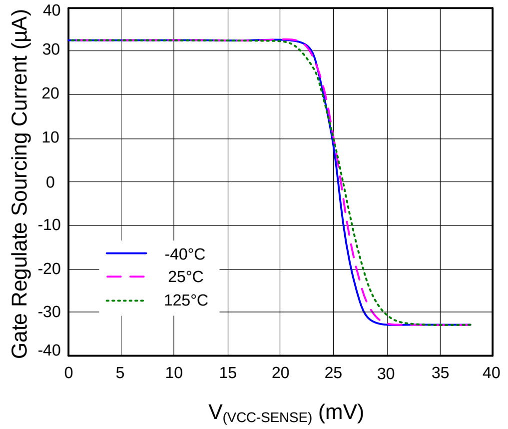




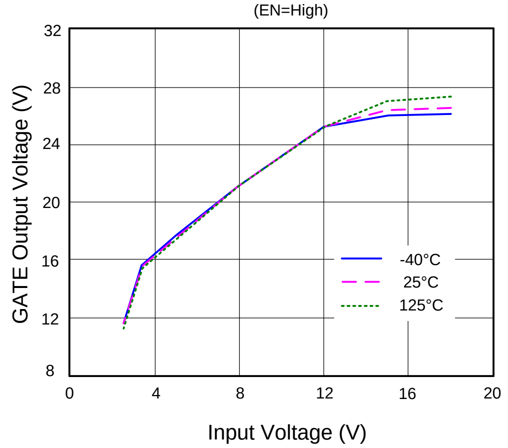
Fast Trip Threshold Voltage vs. Temperature
(VCC=12V, EN=High)



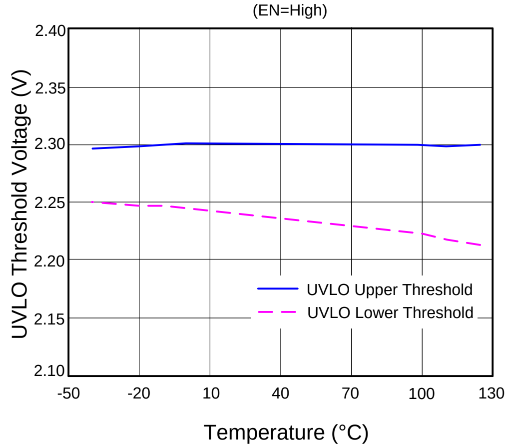
Gate Regulate Sourcing Current vs. $V_{(VCC-SENSE)}$
(VCC=12V, EN=High)



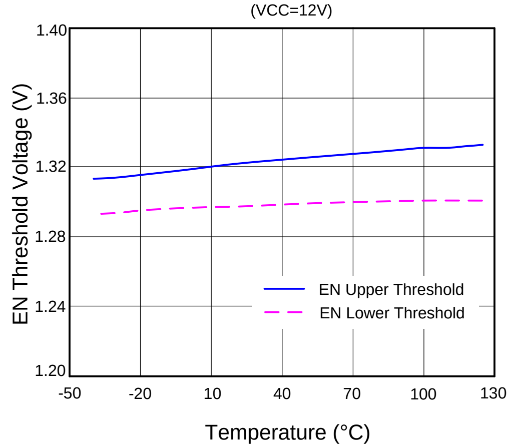
GATE Output Voltage vs. Input Voltage
(EN=High)



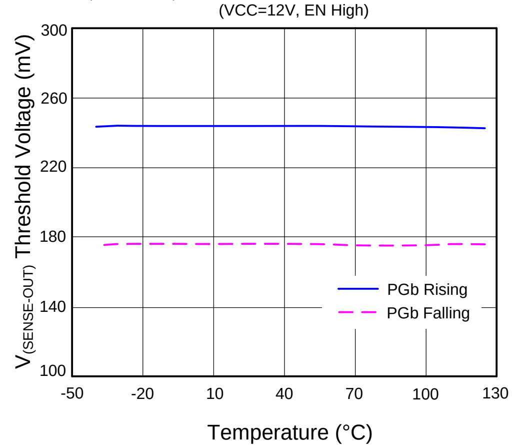
UVLO Threshold Voltage vs. Temperature
(EN=High)

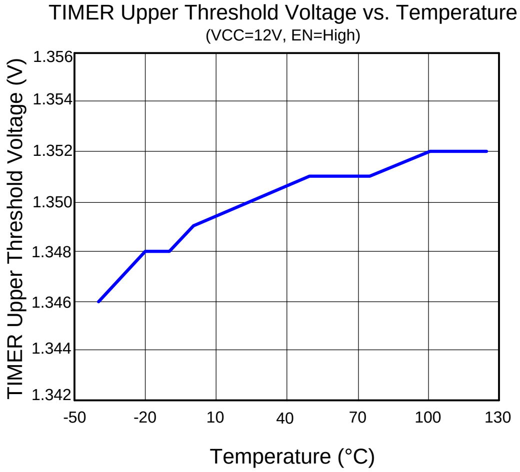


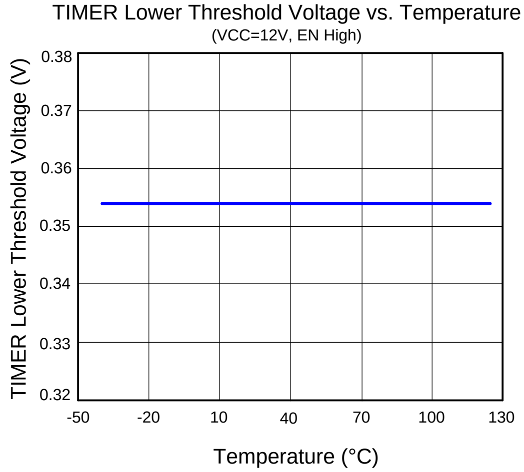
EN Threshold Voltage vs. Temperature
(VCC=12V)

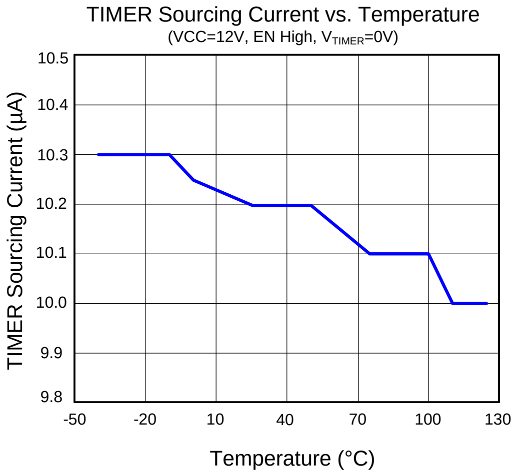


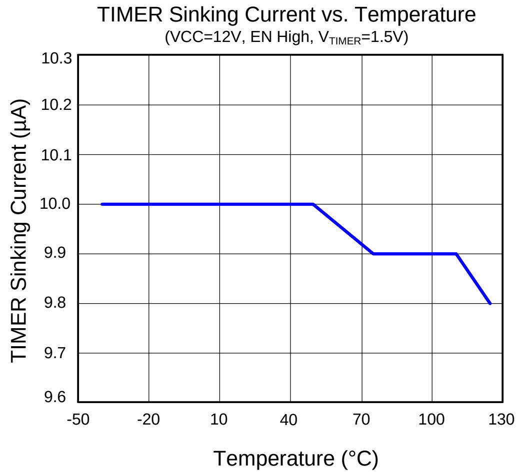
$V_{(SENSE-OUT)}$ Threshold Voltage vs. Temperature
(VCC=12V, EN High)




TIMER Upper Threshold Voltage vs. Temperature
(VCC=12V, EN=High)
TIMER Upper Threshold Voltage (V)
1.356
1.354
1.352
1.350
1.348
1.346
1.344
1.342
-50
-20
10
40
70
100
130
Temperature (°C)


TIMER Lower Threshold Voltage vs. Temperature
(VCC=12V, EN High)
TIMER Lower Threshold Voltage (V)
0.38
0.37
0.36
0.35
0.34
0.33
0.32
-50
-20
10
40
70
100
130
Temperature (°C)


TIMER Sourcing Current vs. Temperature
(VCC=12V, EN High, VTIMER=0V)
TIMER Sourcing Current (µA)
10.5
10.4
10.3
10.2
10.1
10.0
9.9
9.8
-50
-20
10
40
70
100
130
Temperature (°C)


TIMER Sinking Current vs. Temperature
(VCC=12V, EN High, VTIMER=1.5V)
TIMER Sinking Current (µA)
10.3
10.2
10.1
10.0
9.9
9.8
9.7
9.6
-50
-20
10
40
70
100
130
Temperature (°C)

Feature Description

EN
Applying a voltage of 1.35V or more to this pin enables the gate driver. The addition of an external resistor divider allows the EN pin to serve as an under-voltage monitor. This pin should not be left floating.

FLTb
The protection at start-up can be configured through FLTb pin, the control mode is shown in Table1.

Table1. Control Mode

Conditions	Control Mode
FLTb pin floating	Power Limiting
FLTb pin is pulled up to a power supply above 2V by a resistor (the FLTb pin sink current cannot exceed 2mA)	Power Limiting
FLTb pin is connected to ground through a <100kΩ resistor	V_{OUT}>1V, Power Limiting
	V_{OUT}<1V, Current Limiting (Fixed $V_{(VCC\text{-}SENSE)}$ to 1.5mV)

If FLTb pin connects a pull-high resistor to OUT pin, the pull-high resistor must be greater than 1.5MΩ. This pin can be left floating when not used.

If FLTb pin is used for indicator, this active-low open-drain output pulls low when SQ24903 has remained in current limit long enough for the fault timer to expire. In retry mode, a fault timeout first disables the external MOSFET, next waits sixteen cycles of TIMER charging and discharging, and finally attempts a restart. This process repeats as long as the fault persists. And the FLTb pin is pulled low whenever the external MOSFET is disabled by the fault timer. In a sustained fault, the FLTb waveform becomes a train of pulses. The FLTb pin does not assert if the external MOSFET is disabled by EN, over temperature shutdown, or UVLO.

GATE
This pin provides gate drive to the external MOSFET. A charge pump sources 33µA to enhance the external MOSFET. A 13.9V clamp between GATE and VCC limits the gate-to-source voltage, because V_{VCC} is very close to V_{OUT} in normal operation. During start-up, a transconductance amplifier regulates the gate voltage of M_1 to provide inrush current limiting. The TIMER pin charges timer capacitor C_T during the inrush. Inrush current limiting continues until the $V_{(GATE-VCC)}$ exceeds the Timer Activation Voltage (5.6V for V_{VCC} = 12V). Then the SQ24903 enters into circuit-breaker mode. The Timer Activation Voltage is defined as a threshold voltage. When $V_{(GATE\text{-}VCC)}$ exceeds this threshold voltage, the inrush operation is finished and the TIMER stops sourcing current and begins sinking current. In the circuit-breaker mode, the current flowing in R_{SENSE} is compared with the current-limit threshold derived from the MOSFET power-limit scheme (see PROG). If the current flowing in R_{SENSE} exceeds the current limit threshold, then MOSFET M_1 is turned off. The GATE pin is disabled by the following three conditions:

- GATE is pulled down by an 11mA current source when
  - The fault timer expires during an overload current fault (V_{SENSE} > 25mV)
  - V_{EN} is below its falling threshold
  - V_{VCC} drops below the UVLO threshold
- GATE is pulled down by a 1A current source for 13.5µs when a hard output short circuit occurs and $V_{(VCC-SENSE)}$ is greater than 40mV, i.e., the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11mA sustaining current ensures that the external MOSFET remains off.
- GATE is discharged by a 20kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold.

GATE attempts a restart periodically in retry mode. No external resistor should be directly connected from GATE to GND or from GATE to OUT.

GND
This pin is connected to system ground.

OUT
This pin allows the controller to measure the drain-to-source voltage across the external MOSFET M_1. The power-good indicator (PGb) relies on this information, as does the power limiting engine. The OUT pin should be protected from negative voltage transients by a clamping diode or sufficient capacitors. A Schottky diode of 3A/40V is recommended as a clamping diode for high-power applications. The OUT pin should be bypassed to GND with a low-impedance ceramic capacitor in the range of 10nF to 1µF.

PGb
This active-low, open-drain output is intended to interface to downstream dc/dc converters or monitoring circuits. PGb pulls low after the drain-to-source voltage of the FET has fallen below 170mV

and a 3.4ms deglitch delay has elapsed. It goes open-drain when V_{DS} exceeds 240mV. PGb assumes high-impedance status after a 3.4ms deglitch delay once V_{DS} of M_1 rises up, resulting from GATE being pulled to GND at any of the following conditions:

- An overload current fault occurs (V_{SENSE} > 25mV).
- A hard output short circuit occurs, leading to $V_{(VCC-SENSE)}$ greater than 40mV, i.e., the fast-trip shutdown threshold has been exceeded.

This pin can be left floating when not used.

RROG

A resistor from this pin to GND sets the maximum power permitted in the external MOSFET M_1 during inrush. Do not apply a voltage to this pin. If the constant power limit is not desired, use a PROG resistor of 4.99kΩ. To set the maximum power, use Equation (1).

$$R_{PROG} = \frac{3125}{R_{SENSE} \times P_{LIM} + 0.9mV \times V_{VCC}} \quad (1)$$

To compute the Power limit based on an existing RPROG use Equation (2).

$$P_{LIM} = \frac{3125}{R_{SENSE} \times R_{PROG}} - \frac{0.9mV \times V_{(VCC\text{-}OUT)}}{R_{SENSE}} \quad (2)$$

where P_{LIM} is the allowed power limit of MOSFET M_1. R_{SENSE} is the load-current-monitoring resistor connected between the VCC pin and the SENSE pin. R_{PROG} is the resistor connected from the PROG pin to GND. Both R_{PROG} and R_{SENSE} are in ohms and P_{LIM} is in watts. P_{LIM} is determined by the maximum allowed thermal stress of MOSFET M_1, given by Equation (3),

$$P_{LIM} \le \frac{T_{J(MAX)} - T_{C(MAX)}}{R_{\theta JC(MAX)}} \quad (3)$$

where $T_{J(MAX)}$ is the maximum desired transient junction temperature and $T_{C(MAX)}$ is the maximum case temperature prior to a start or restart. $R_{\Theta JC(MAX)}$ is the junction-to-case thermal impedance of the pass MOSFET M_1 in units of °C/W. Both $T_{J(MAX)}$ and $T_{C(MAX)}$ are in °C.

SENSE

This pin connects to the negative terminal of R_{SENSE}. It provides a means of sensing the voltage across this resistor, as well as a way to monitor the drain-to-source voltage across the external FET. The current limit I_{LIM} is set by Equation (4).

$$I_{LIM} = \frac{25mV}{R_{SENSE}} \quad (4)$$

A fast trip shutdown occurs when $V_{(VCC-VSENSE)}$ exceeds 40mV.

TIMER

A capacitor C_T connected from the TIMER pin to GND determines the overload fault timing. TIMER sources 10μA when an overload is present, and discharges C_T at 10μA otherwise. M_1 is turned off when V_{TIMER} reaches 1.35V. In an application implementing auto-retry after a fault, this capacitor also determines the period before the external MOSFET is re-enabled. A minimum timing capacitance of 1nF is recommended to ensure proper operation of the fault timer. The value of C_T can be calculated from the desired fault time t_{FLT}, using Equation (5).

$$C_T = \frac{10\mu A}{1.35V} \times t_{FLT} \quad (5)$$

The retry mode occurs if the load current exceeds the current limit threshold or the fast-trip shutdown threshold. While in retry mode, the external MOSFET is disabled for sixteen cycles of TIMER charging and discharging. The TIMER pin is pulled to GND by a 2mA current source at the end of the 16th cycle of charging and discharging. The external MOSFET is then re-enabled. The TIMER pin capacitor, C_T, can also be discharged to GND during retry mode by a 4.5mA current source whenever any of the following occurs:

- V_{EN} is below its falling threshold.
- V_{VCC} drops below the UVLO threshold.

VCC

This pin performs three functions. First, it provides biasing power to the integrated circuit. Second, it serves as an input to the power-on reset (POR) and under-voltage lockout (UVLO) functions. The VCC trace from the integrated circuit should connect directly to the positive terminal of R_{SENSE} to minimize the voltage sensing error. Bypass capacitor C_{IN}, shown in the typical application diagram on the front page, should be connected to the positive terminal of R_{SENSE}. A capacitance of at least 10nF is recommended.

Device Functional Modes

The SQ24903 provides all the features needed for a positive hot-swap controller. These features include:

- Under-voltage Lockout
- Adjustable (System-Level) Enable
- Turn-on Inrush Limiting
- High-side Gate Drive for an External N-Channel MOSFET

- MOSFET Protection by Power Limiting
- Adjustable Overload Timeout
  — Also Called an Electronic Circuit Breaker
- Charge-complete Indicator for Downstream Converter Coordination

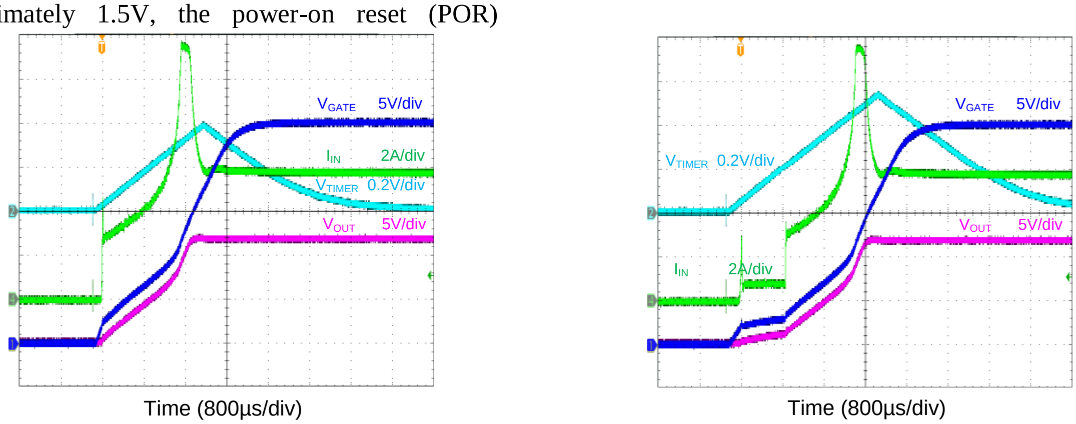
The Typical Application (12V at 10A), and oscilloscope plots shown in Figure 5 through Figure 7 and Figure 9 through Figure 11, demonstrate many of the functions described previously.

Board Plug In

Figure 5 and Figure 6 illustrate the inrush current that flows when a hot swap board under the control of the SQ24903 is plugged into a system bus. Only the bypass capacitor charge current is evident when a board is first plugged in. The SQ24903 is held inactive, for a short period while internal voltages stabilize. During this period GATE, PROG, TIMER are held low and PGb and FLTb are held open drain. When the voltage on the internal VCC rail exceeds approximately 1.5V, the power-on reset (POR) circuit initializes the SQ24903 and a start-up cycle is ready to take place.

GATE, PROG, TIMER, PGb, and FLTb are released after the internal voltages have stabilized and the external EN (enable) thresholds have been exceeded. The part begins sourcing current from the GATE pin to turn on MOSFET M_1. The SQ24903 monitors both the drain-to-source voltage across MOSFET M_1 and the drain current passing through it. Based on these measurements, the SQ24903 limits the drain current by controlling the gate voltage so that the power dissipation within the MOSFET does not exceed the power limit programmed by the user. The current increases as the voltage across the MOSFET decreases until finally the current reaches the current limit I_{LIM}.

If FLTb connects to ground through a <100kΩ resistor, the SQ24903 limits the drain current by fixed $V_{(VCC\text{-}SENSE)}$ to 1.5mV when VOUT lower than 1V, as shown in Figure 5(b).



(a) FLTb is pulled high (b) FLTb is pulled low

Fig 5 Inrush Mode at Hot-Swap Circuit Insertion

Inrush Operation

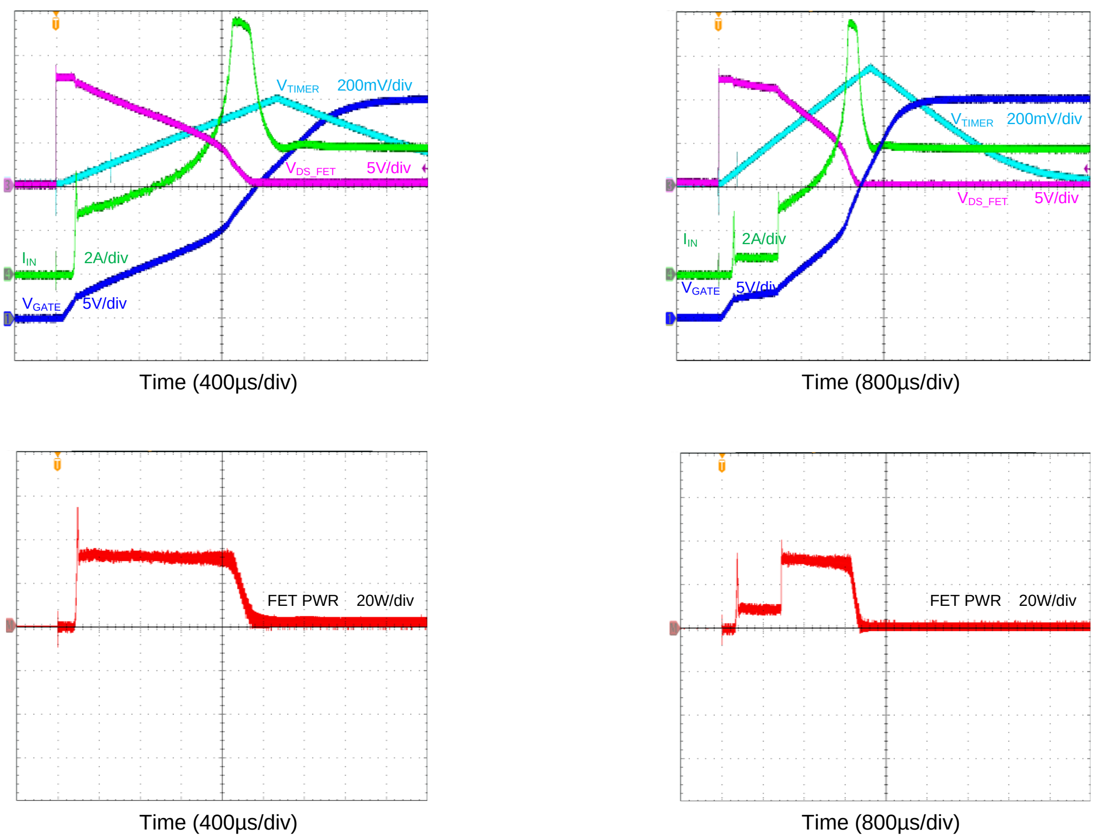
After SQ24903 initialization is complete (as described in the Board Plug-In section) and EN is active, GATE is enabled (V_{GATE} starts increasing). When V_{GATE} reaches the MOSFET M_1 gate threshold, a current flows into the downstream bulk storage capacitors. When this current exceeds the limit set by the power limit engine, the gate of the MOSFET is regulated by a feedback loop to make the MOSFET current rise in a controlled manner. This not only limits the inrush current charging capacitance but it also limits the power dissipation of the MOSFET to safe levels. A more complete explanation of the power limiting scheme is given in the section entitled *Action of the Constant Power Engine*. When Gate is enabled, the TIMER pin begins to charge the timing capacitor C_T with a current of approximately 10µA.

The TIMER pin continues to charge C_T until $V_{(GATE-VCC)}$ reaches the timer activation voltage (5.6V for V_{VCC} = 12V). The TIMER then begins to discharge C_T with a current of approximately 10µA. This indicates that the inrush mode is finished. If the TIMER exceeds its upper threshold of 1.35V before $V_{(GATE-VCC)}$ reaches the timer activation voltage, the GATE pin is pulled to GND and the hot-swap circuit enter auto-retry mode.

The power limit feature is disabled once the inrush operation is finished and the hot swap circuit becomes a circuit breaker. The SQ24903 will turn off the MOSFET, M_1, after a fault timer period once the load exceeds the current limit threshold.

Action of the Constant-Power Engine

Figure 6 illustrates the operation of the constant-power engine during start-up. The circuit used to generate the waveforms of Figure 6 was programmed to a power limit of 29.3W by means of the resistor connected between PROG and GND. At the moment current begins to flow through the MOSFET, a voltage of 12V appears across it (input voltage V_{VCC} = 12V), and the constant-power engine therefore allows a current of 2.44A (equal to 29.3W divided by 12V) to flow. This current increases in inverse ratio as the drain-to-source voltage diminishes, so as to maintain a constant dissipation of 29.3W. The constant-power engine adjusts the current by altering the reference signal fed to the current limit amplifier. The lower part of Figure 6 shows the measured power dissipated within the MOSFET, labeled *FET PWR*, remaining substantially constant during this period of operation, which ends when the current through the MOSFET reaches the current limit I_{LIM}. This behavior can be considered a form of fold back limiting, but unlike the standard linear form of fold back limiting, it allows the power device to operate near its maximum capability, thus reducing the start-up time and minimizing the size of the required MOSFET.



(a) FLTb is pulled high (b) FLTb is pulled low

Fig 6 Computation of M1 Power Stress During Start-up

Circuit Breaker and Fast Trip

The SQ24903 monitors load current by sensing the voltage across R_{SENSE}. The SQ24903 incorporates two distinct thresholds: a current-limit threshold and a fast-trip threshold.

The functions of circuit breaker and fast-trip turn off are shown in Figure 7 through Figure 10.

Figure7 shows the behavior of the SQ24903 when a fault in the output load causes the current passing through R_{SENSE} to increase to a value above the current limit but less than the fast-trip threshold. When the current exceeds the current-limit threshold, a current of approximately 10µA begins to charge timing capacitor C_T. If the voltage on C_T reaches 1.35V, then the external MOSFET is turned off. The SQ24903 commences a restart cycle, and fault pin FLTb pulls low to signal a fault condition. Overload between the current limit and the fast trip threshold is permitted for this period. This shutdown scheme is sometimes called an electronic circuit breaker.

The fast-trip threshold protects the system against a severe overload or a dead short circuit. When the voltage across the sense resistor R_{SENSE} exceeds the 40mV fast-trip threshold, the GATE pin immediately pulls the external MOSFET gate to ground with approximately 1A of current. This extremely rapid shutdown may generate disruptive transients in the system, in which case a low-value resistor inserted between the GATE pin and the MOSFET gate can be used to moderate the turn off current. The fast-trip circuit holds the MOSFET off for only a few microseconds, after which the SQ24903 turns back on slowly, allowing the current-limit feedback loop to take over the gate control of M_1. Then the hot-swap circuit goes into auto-retry mode. Figure 9 and Figure 10 illustrate the behavior of the system implementing SQ24903 when the current exceeds the fast-trip threshold.

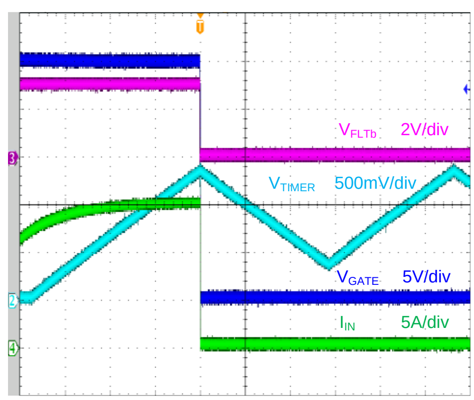


Fig 7 Circuit Breaker Mode During Over Load Condition

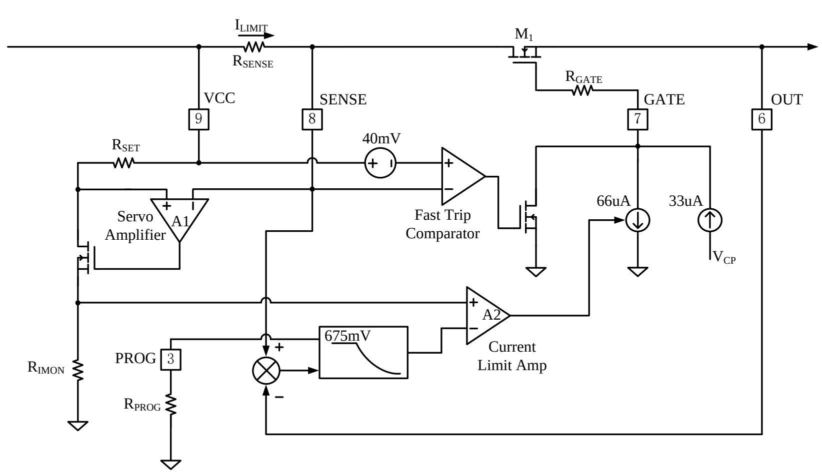
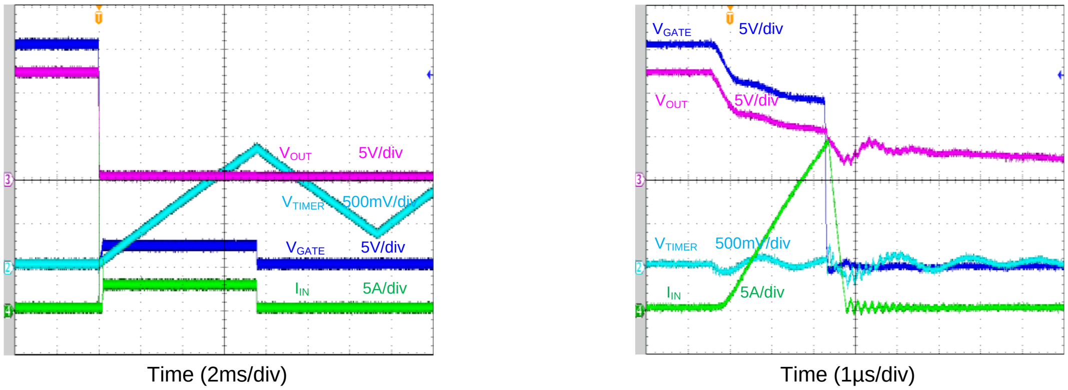
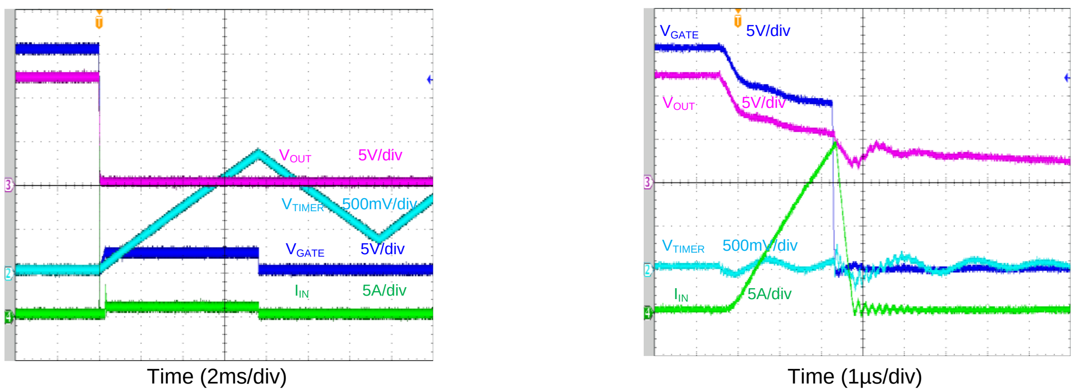


Fig 8 Partial Diagram of SQ24903 with Selected External Components



(a) Overview (b) Onset

Fig 9 Current Limit During Output Load Short Circuit Condition when FLTb is Pulled High



(a) Overview (b) Onset

Fig 10 Current Limit During Output Load Short Circuit Condition when FLTb is Pulled Low

Automatic Restart

The SQ24903 automatically initiates a restart after a fault has caused it to turn off the external MOSFET M_1. Internal control circuits use C_T to count 16 cycles before re-enabling M_1 as shown in Figure 11. This sequence repeats if the fault persists. The timer has a 1: 1 charge-to-discharge current ratio. For the very first cycle, the TIMER pin starts from 0V and rises to the upper threshold of 1.35V and subsequently falls to 0.35V before restarting. For the following 16 cycles, 0.35V is used as the lower threshold. This small duty cycle often reduces the average short-circuit power dissipation to levels associated with normal operation and eliminates special thermal considerations for surviving a prolonged output short.

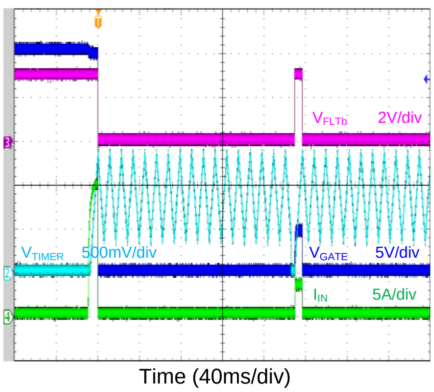


Fig 11 Auto-Restart Cycle Timing

PGb, FLTb, and Timer Operations

The open-drain PGb output provides a deglitched end-of-inrush indication based on the voltage across M_1. PGb is useful for preventing a downstream dc/dc converter from starting while its input capacitor C_{OUT} is still charging. PGb goes active low about 3.4 ms after C_{OUT} is charged. This delay allows M_1 to fully turn on and any transients in the power circuits to end before the converter starts up. This type of sequencing prevents the downstream converter from demanding full current before the power-limiting engine allows the MOSFET to conduct the full current set by the current limit I_{LIM}. Failure to observe this precaution may prevent the system from starting. The pull up resistor shown on the PGb pin in the typical application diagram on the front page is illustrative only; the actual connection to the converter depends on the application. The PGb pin may indicate that inrush has ended before the MOSFET is fully enhanced, but the downstream capacitor will have been charged to substantially its full operating voltage. Care should be taken to ensure that the MOSFET on-resistance is sufficiently small to ensure that the voltage drop across this transistor is less than the minimum power-good threshold of 140mV. After the hot-swap circuit successfully starts up, the PGb pin can return to a high-impedance status whenever the drain-to-source voltage of MOSFET M_1 exceeds its upper threshold of 240 mV, which presents the downstream converters a warning flag. This flag may occur as a result of overload fault, output short fault, input overvoltage, higher die temperature, or the GATE shutdown by UVLO and EN.

FLTb is an indicator that the allowed fault-timer period during which the load current can exceed the programmed current limit (but not the fast-trip threshold) has expired. The fault timer starts when a current of approximately 10μA begins to flow into the external capacitor, C_T, and ends when the voltage of C_T reaches TIMER upper threshold, i.e., 1.35V. FLTb pulls low at the end of the fault timer. Otherwise, FLTb assumes a high-impedance state.

If the FLTb pin connects to ground through a <100kΩ resistor, the SQ24903 limits the drain current by fixed $V_{(VCC-SENSE)}$ to 1.5mV when V_{OUT} lower than 1V.

If the FLTb pin connects a pull-high resistor to OUT pin, the pull-high resistor must be greater than 1.5MΩ. This pin can be left floating when not used.

The fault-timer state requires an external capacitor C_T connected between the TIMER pin and GND pin. The length of the fault timer is the charging time of C_T from 0V to its upper threshold of 1.35V. The fault timer begins to count under any of the following three conditions:

- In the inrush mode, TIMER begins to source current to the timer capacitor, C_T, when MOSFET M_1 is enabled. TIMER begins to sink current from the timer capacitor, C_T when $V_{(GATE-VCC)}$ exceeds the timer activation voltage (see the Inrush Operation section). If $V_{(GATE-VCC)}$ does not reach the timer activation voltage before TIMER reaches 1.35V, then the SQ24903 disables the external MOSFET M_1. After the MOSFET turns off, the timer goes into retry mode.
- In an overload fault, TIMER begins to source current to the timer capacitor, C_T, when the load current exceeds the programmed current limits. When the timer capacitor voltage reaches its upper threshold of 1.35V, TIMER begins to sink current from the timer capacitor, C_T, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into retry mode.
- In output short-circuit fault, TIMER begins to source current to the timer capacitor, C_T, when the load current exceeds the programmed current limits following a fast-trip shutdown of

M_1. When the timer capacitor voltage reaches its upper threshold of 1.35V, TIMER begins to sink current from the timer capacitor, C_T, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into retry mode.

If the fault current drops below the programmed current limit within the fault timer period, V_{TIMER} decreases and the pass MOSFET remains enabled.

If the timer capacitor reaches the upper threshold of 1.35V, in retry mode, TIMER charges and discharges C_T between the lower threshold of 0.35V and the upper threshold of 1.35V for sixteen cycles before the SQ24903 attempts to re-start. The TIMER pin is pulled to GND at the end of the 16th cycle of charging and discharging and then ramps from 0V to 1.35V for the initial half-cycle in which the GATE pin sources current. This periodic pattern is stopped once the overload fault is removed or the SQ24903 is disabled by UVLO or EN.

Over Temperature Shutdown

The SQ24903 includes a built-in over temperature shutdown circuit designed to disable the gate driver if the die temperature exceeds approximately 150℃. An over temperature condition also causes the FLTb and PGb pins to go to high-impedance states. Normal operation resumes once the die temperature has fallen approximately 20℃.

Start-up of Hot-swap Circuit by VCC or EN

The connection and disconnection between a load and the system bus are controlled by turning on and turning off the MOSFET, M_1.

The SQ24903 has two ways to turn on MOSFET M_1:

- Increasing V_{VCC} above UVLO upper threshold while EN is already higher than its upper threshold sources current to the GATE pin. After an inrush period, SQ24903 fully turns on MOSFET M_1.
- Increasing EN above its upper threshold while V_{VCC} is already higher than UVLO upper threshold sources current to the GATE pin. After an inrush period, SQ24903 fully turns on MOSFET M_1.

The EN pin can be used for starting up the SQ24903 at a selected input voltage V_{VCC}.

To isolate the load from the system bus, the GATE pin sinks current and pulls the gate of MOSFET M_1 low. The MOSFET can be disabled by any of the following conditions: UVLO, EN, load current above current limit threshold, hard short at load, or OTSD. Three separate conditions pull down the GATE pin:

- GATE is pulled down by an 11mA current source when any of the following occurs.
  - The fault timer expires during an overload current fault (V_{SENSE} > 25mV).
  - V_{EN} is below its falling threshold.
  - V_{VCC} drops below the UVLO threshold.
- GATE is pulled down by a 1A current source for 13.5µs when a hard output short circuit occurs and $V_{(VCC-SENSE)}$ is greater than 40mV, i.e., the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11mA sustaining current ensures that the external MOSFET remains off.
- GATE is discharged by a 20kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold.

Application and Implementation

(Note: Information in the following applications sections is not part of the Silergy component specification, and Silergy does not warrant its accuracy or completeness. Silergy's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.)

Application Information

The SQ24903 is a hot swap used to manage inrush current and provide load fault protection. When designing a hot swap, three key scenarios should be considered:

- Start-up.
- Output of a hot swap is shorted to ground when the hot swap is on. This is often referred to as a hot-short.
- Powering-up a board when the output and ground are shorted. This is usually called a start-into-short.

Each of these scenarios place stress on the hot swap MOSFET. Take special care when designing the hot swap circuit to keep the MOSFET within its SOA. The following design example is provided as a guide.

Typical Application

This section provides an application example utilizing power limited start-up and MOSFET SOA protection. The design parameters are listed in the *Design Requirements* section and represent a more moderate level of fault current.

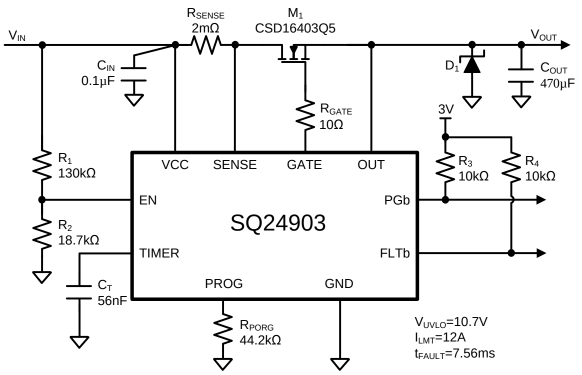


Fig 12 Typical Application (12V at 10A)

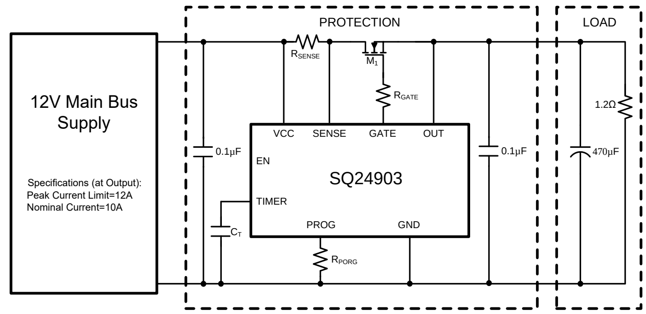


Fig 13 Simplified Block Diagram of the System Constructed in the Design Example

Design Requirements

For this design example, use the parameters shown in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
Input Voltage	12 V±2V
Maximum Operating Load Current	10A
Operating Temperature	20°C ~ 50°C
Fault Trip Current	12A
Load Capacitance	470µF

Detailed Design Procedure

A. Power-Limited Start-Up

This design example assumes a 12V system voltage with an operating tolerance of ±2V. The rated load current is 10A, corresponding to a dc load of 1.2Ω. If the current exceeds 12A, then the controller should shut down and then attempt to restart. Ambient temperatures may range from 20°C to 50°C. The load has a minimum input capacitance of 470µF. Figure 13 shows a simplified system block diagram of the proposed application.

This design procedure seeks to control the junction temperature of MOSFET M_1 under both static and transient conditions by proper selection of package, cooling, $R_{DS(on)}$, current limit, fault timeout, and power limit. The design procedure further assumes that a unit running at full load and maximum ambient temperature experiences a brief input-power interruption sufficient to discharge C_{OUT}, but short enough to keep M_1 from cooling. A full C_{OUT} recharge then takes place. Adjust this procedure to fit your application and design criteria.

STEP 1. Choose R_{SENSE}

From the SQ24903 electrical specifications, the current-limit threshold voltage, $V_{(VCC-SENSE)}$, is around 25mV. A resistance of 2mΩ is selected for the peak current limit of 12A, while dissipating only 200mW at the rated 10A current (see Equation (6)). This represents a 0.17% power loss.

$$R_{SENSE}=\frac{V_{(VCC\text{-}SENSE)}}{I_{LIM}},$$

therefore,

$$R_{SENSE}=\frac{25mV}{12A}\approx 2m\Omega \quad (6)$$

STEP 2. Choose MOSFET M_1

The next design step is to select M_1. The SQ24903 is designed to use an N-channel MOSFET with a gate to source voltage rating of 20V.

Devices with lower gate-to-source voltage ratings can be used if a Zener diode is connected so as to limit the maximum gate to source voltage across the transistor.

The next factor to consider is the drain to source voltage rating, $V_{DS(MAX)}$, of the MOSFET. Although the MOSFET only sees 12V DC, it may experience much higher transient voltages during extreme conditions, such as the abrupt shutoff that occurs during a fast trip. A TVS may be required to limit inductive transients under such conditions. A transistor with a $V_{DS(MAX)}$ rating of at least twice the nominal input power supply voltage is recommended regardless of whether a TVS is used or not.

Next select the on resistance of the transistor, $R_{DS(on)}$. The maximum on resistance must not generate a voltage greater than the minimum power good threshold voltage of 140mV. Assuming a current limit of 12A, a maximum $R_{DS(on)}$ of 11.67mΩ is required. Also consider the effect of $R_{DS(on)}$ upon the maximum operating temperature $T_{J(MAX)}$ of the

MOSFET. Equation (7) computes the value of $R_{DS(on)(MAX)}$ at a junction temperature of $T_{J(MAX)}$. Most manufacturers list $R_{DS(on)(MAX)}$ at 25°C and provide a derating curve from which values at other temperatures can be derived. Compute the maximum allowable on-resistance, $R_{DS(on)(MAX)}$, using Equation (7).

$$R_{DS(on)(MAX)} \le \frac{T_{J(MAX)}-T_{A(MAX)}}{I_{MAX}^2 \times R_{\theta JA}},$$

therefore,

$$R_{DS(on)(MAX)} \le \frac{150°C-50°C}{(12A)^2 \times 51°C/W} = 13.6m\Omega \quad (7)$$

Taking these factors into consideration, the CSD16403Q5 was selected for this example. This transistor has a $V_{GS(MAX)}$ rating of 16V, a $V_{DS(MAX)}$ rating of 25V, and a maximum $R_{DS(on)}$ of 2.8mΩ at room temperature. During normal circuit operation, the MOSFET can have up to 10A flowing through it. The power dissipation of the MOSFET equates to 0.28W and a 14.28°C rise in junction temperature. This is well within the data sheet limits for the MOSFET. The power dissipated during a fault (e.g., output short) is far larger than the steady state power.

The power handling capability of the MOSFET must be checked during fault conditions.

STEP 3. Choose Power-Limit Value, P_{LIM}, and R_{PROG}

MOSFET M_1 dissipates large amounts of power during inrush. The power limit P_{LIM} of the SQ24903 should be set to prevent the die temperature from exceeding a short-term maximum temperature, $T_{J(MAX)2}$. The short-term $T_{J(MAX)2}$ could be set as high as 130°C while still leaving ample margin to the usual manufacturer's rating of 150°C. Equation (8) is an expression for calculating P_{LIM},

$$P_{LIM} \le 0.8 \times \frac{T_{J(MAX)2}-\left[\left(I_{MAX}^2 \times R_{DS(on)} \times R_{\theta CA}\right)+T_{A(MAX)}\right]}{R_{\theta JC}}$$

therefore,

$$P_{LIM} \le 0.8 \times \frac{130°C-\left[\left((12A)^2 \times 0.002\Omega \times (51°C/W-1.8°C/W)\right)+50°C\right]}{1.8°C/W} = 29.3W \quad (8)$$

where $R_{\theta JC}$ is the junction to case thermal resistance of the MOSFET, $R_{DS(on)}$ is the resistance at the maximum operating temperature, and the factor of 0.8 represents the tolerance of the constant power engine. For an ambient temperature of 50°C, the calculated maximum P_{LIM} is 29.3W. The R_{PROG} is calculated in Equation (9a) as 43.89kΩ.

$$R_{PROG} = \frac{3125}{R_{SENSE} \times P_{LIM} + 0.9mV \times V_{VCC(MAX)}}$$

therefore,

$$R_{PROG} = \frac{3125}{0.002\Omega \times 29.3W + 0.9mV \times 14V} = 43.89k\Omega \quad (9a)$$

Selecting the next highest standard value, 44.2kΩ, 1% for R_{PROG}, yields the power limit is 29.1W<29.3W(see Equation (9b)).

$$P_{LIM} = \frac{3125}{R_{SENSE} \times R_{PROG}} - \frac{0.9mV \times V_{VCC(MAX)}}{R_{SENSE}}$$

therefore,

$$P_{LIM} = \frac{3125}{44.2k\Omega \times 0.002\Omega} - \frac{0.9mV \times 14V}{0.002\Omega} = 29.1W \quad (9b)$$

STEP 4. Choose Output Voltage Rising Time, t_{ON}, C_T

The maximum output voltage rise time, t_{ON}, set by the timer capacitor C_T must suffice to fully charge the load capacitance C_{OUT} without triggering the fault circuitry. Equation (10) defines t_{ON} for two possible inrush cases.

Assuming that only the load capacitance draws current during start-up,

$$t_{ON} = \begin{cases} \frac{C_{OUT} \times P_{LIM}}{2 \times I_{LIM}^2} + \frac{C_{OUT} \times V_{VCC(MAX)}^2}{2 \times P_{LIM}} - \frac{C_{OUT} \times V_{VCC(MAX)}}{I_{LIM}} & \text{if} \quad P_{LIM} < I_{LIM} \times V_{VCC(MAX)} \\ \frac{C_{OUT} \times V_{VCC(MAX)}}{I_{LIM}} & \text{if} \quad P_{LIM} > I_{LIM} \times V_{VCC(MAX)} \end{cases}$$

therefore,

$$t_{ON} = \frac{470\mu F \times 29.3W}{2 \times (12A)^2} + \frac{470\mu F \times (14V)^2}{2 \times 29.3W} - \frac{470\mu F \times 14V}{12A} = 1.071ms \quad (10)$$

The next step is to determine the minimum fault timer period. In Equation (10), the output rise time is t_{ON}. This is the amount of time it takes to charge the output capacitor up to the final output voltage. However, the fault timer uses the difference between the input voltage and the gate voltage to determine if the SQ24903 is still in inrush limit. The fault timer continues to run until V_{GS} rises 5.6V (for V_{VCC} = 12V) above the input voltage. Some additional time must be added to the charge time to account for this additional gate voltage rise. The minimum fault time can be calculated using Equation (11),

$$t_{FLT} = t_{ON} + \frac{5.6V \times C_{ISS}}{I_{GATE}}$$

therefore,

$$t_{FLT} = 1.071ms + \frac{5.6V \times 2040pF}{20\mu A} = 1.642ms \quad (11)$$

where C_{ISS} is the MOSFET input capacitance and I_{GATE} is the minimum gate sourcing current of SQ24903, or 20μA. Using the example parameters in Equation (11) and the CSD16403Q5 datasheet leads to a minimum fault time of 1.642ms. This time is derived considering the tolerances of C_{OUT}, C_{ISS}, I_{LIM}, P_{LIM}, I_{GATE}, and $V_{VCC(MAX)}$. The fault timer must be set to a value higher than 1.642ms to avoid turning off during start up, but lower than any maximum fault time limit determined by the SOA curve (see Figure 15) derated for operating junction temperature.

For this example, select 7ms to allow for variation of system parameters such as temperature, load, component tolerance, and input voltage. The timing capacitor is calculated in Equation (5) as 52nF. Selecting the next highest standard value, 56nF, yields a 7.56ms fault time (see Equation (12)).

$$C_T = \frac{10\mu A}{1.35V} \times t_{FLT}$$

therefore,

$$C_T = \frac{10\mu A}{1.35V} \times 7ms = 52nF$$

$$t_{FLT} = \frac{1.35V \times 56nF}{10\mu A} = 7.56ms \quad (12)$$

STEP 5. Calculate the Retry-Mode Duty Ratio

In retry mode, the SQ24903 is on for one charging cycle and off for 16 charge/discharge cycles, as can be seen in Figure 11. The first C_T charging cycle is from 0V to 1.35V, which gives 7.56ms. The first C_T discharging cycle is from 1.35V to 0.35V, which gives 5.6ms. Therefore, the total time is 7.56ms+33×5.6ms=192.36ms. As a result, the retry mode duty ratio is 7.56ms/192.36ms = 3.93%.

STEP 6. Select R_1 and R_2 for UV

Next, select the values of the UV resistors, R_1 and R_2, as shown in the typical application diagram on the front page. From the SQ24903 electrical specifications, $V_{ENTHRESH}$=1.35V. The V_{UV} is the under voltage trip voltage, which for this example equals 10.7V.

$$V_{ENTHRESH} = \frac{R_2}{R_1 + R_2} \times V_{VCC} \quad (13)$$

Assume R_1 is 130kΩ and use Equation (13) to solve for the R_2 value of 18.7kΩ.

STEP 7. Choose R_{GATE}, R_3, R_4 and C_{IN}

In the typical application diagram on the front page, the gate resistor, R_{GATE}, is intended to suppress high frequency oscillations. A resistor of 10Ω will serve for most applications, but if M_1 has a C_{ISS} below 200pF, then 33Ω is recommended. Applications with larger MOSFETs and very short wiring may not require R_{GATE}. R_3 and R_4 are required only if PGb and FLTb are used for indicator; these resistors serve as pullups for the open-drain output drivers. The current sunk by each of these pins should not exceed 2mA (see the RECOMMENDED OPERATING CONDITIONS table). C_{IN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise while in the disabled state. Where acceptable, a value in the range of 0.001μF to 0.1μF is recommended.

B. Additional Design Considerations

Use of PGb

Use the PGb pin to control and coordinate a downstream dc/dc converter. If this is not done, then a long time delay is needed to allow C_{OUT} to fully charge before the converter starts. An undesirable latch-up condition can be created between the SQ24903 output characteristic and the dc/dc converter input characteristic if the converter starts while C_{OUT} is still charging; the PGb pin is one way to avoid this.

Output Clamp Diode

Inductive loads on the output may drive the OUT pin below GND when the circuit is unplugged or during a current limit event. The OUT pin ratings can be satisfied by connecting a diode from OUT to GND. The diode should be selected to control the negative voltage at the full short circuit current. Schottky diodes are generally recommended for this application.

Gate Clamp Diode

The SQ24903 has a relatively well-regulated gate voltage of 12V to 15.5V with a supply voltage V_{VCC} higher than 5V. A small clamp Zener from GATE to source of M_1 is recommended if V_{GS} of M_1 is rated below 12V. A series resistance of several hundred ohms or a series silicon diode is recommended to prevent the output capacitance from discharging through the gate driver to ground.

High-Gate-Capacitance Applications

Gate voltage overstress and abnormally large fault current spikes can be caused by large gate capacitance. An external gate clamp Zener diode is recommended to assist the internal Zener if the total gate capacitance of M_1 exceeds about 4000pF.

Bypass Capacitors

It is a good practice to provide low-impedance ceramic capacitor bypassing of the VCC and OUT pins. Values in the range of 10nF to 1μF are recommended. Some system topologies are insensitive to the values of these capacitors; however, some are not and require minimization of the value of the bypass capacitor. Input capacitance on a plug in board may cause a large inrush current as the capacitor charges through the low impedance power bus when inserted. This stresses the connector contacts and causes a short voltage sag on the input bus. Small amounts of capacitance (e.g., 10nF to 0.1μF) are often tolerable in these systems.

Output Short Circuit Measurements

Repeatable short circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in this datasheet; every setup differs.

Using Soft-start with SQ24903

In some applications, it may be desired to have a constant dv/dt ramp on the output of the SQ24903 to ensure a constant inrush current. This is often accomplished by adding a capacitor from GATE to GND as shown in Figure 14. This limits the gate ramp speed, which in turn limits the ramp of the output.

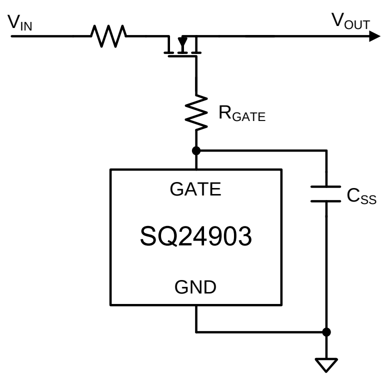


Fig 14 Simplified Diagram for Using Soft-start

Due to the nature of the timer and the gate driver, there are several considerations that must be taken into account when using this type of a design.

Application Curve

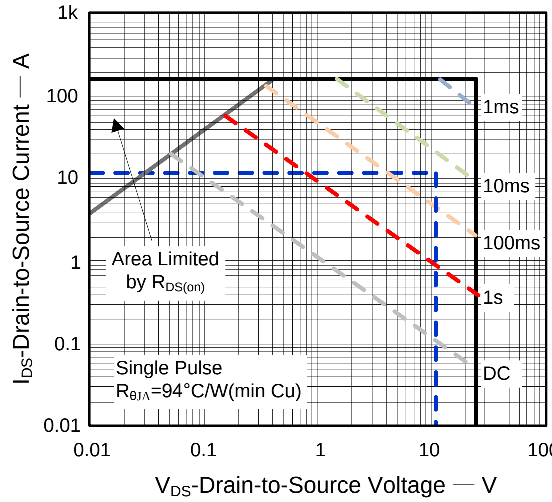


Fig 15 CSD16403Q5 SOA Curve

Power Supply Recommendations

Use a 10nF to 1μF ceramic capacitor to bypass the VCC pin to GND. When the input bus power feed is inductive, then a transient voltage suppressor (TVS) may also be required.

PCB Layout Guide

The SQ24903 applications require careful attention to layout to ensure proper performance and to minimize susceptibility to transients and noise. In general, all traces should be as short as possible, but the following list deserves first consideration:

- ✧ Decoupling capacitors on VCC pin should have minimal trace lengths to the pin and to GND.
- ✧ Traces to VCC and SENSE must be short and run side-by-side to maximize common-mode rejection. Kelvin connections should be used at the points of contact with R_{SENSE}. (see Figure 16).
- ✧ Power path connections should be as short as possible and sized to carry at least twice the full load current, more if possible.
- ✧ Protection devices such as snubbers, TVS, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, the protection Schottky diode shown in the typical application diagram on the front page of this data sheet should be physically close to the OUT pin.

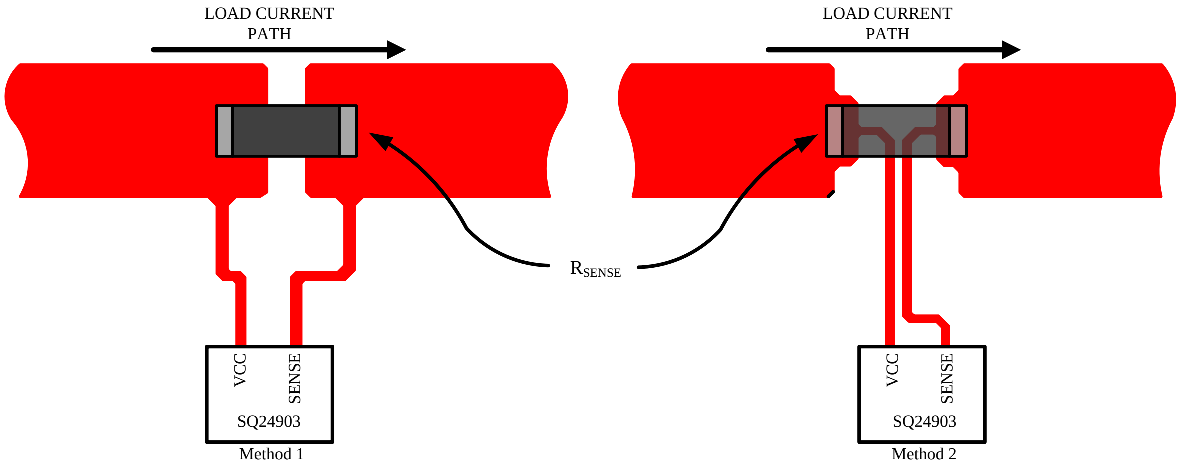
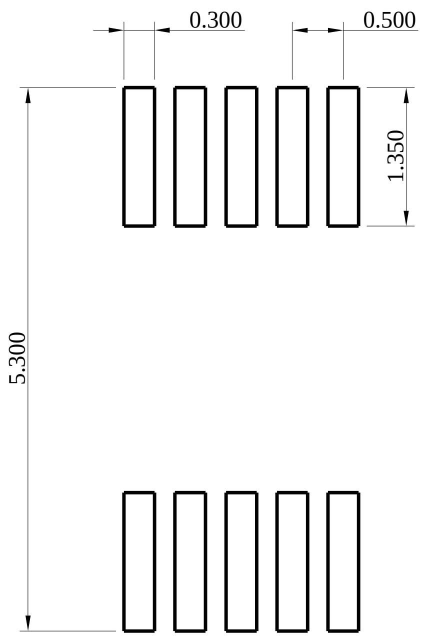
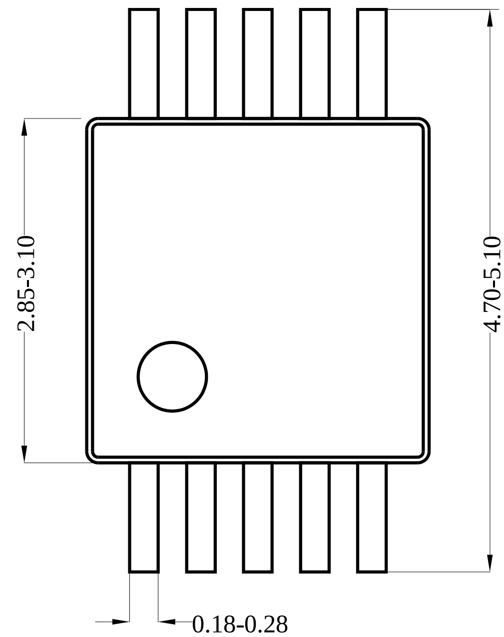


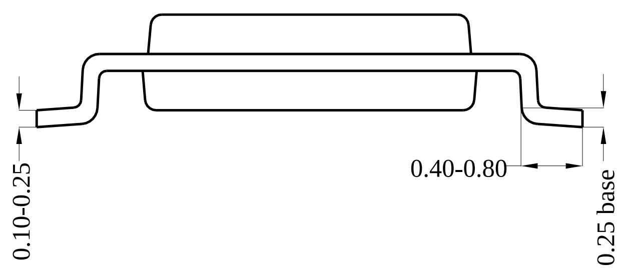
Fig 16 Recommended R_{SENSE} Layout

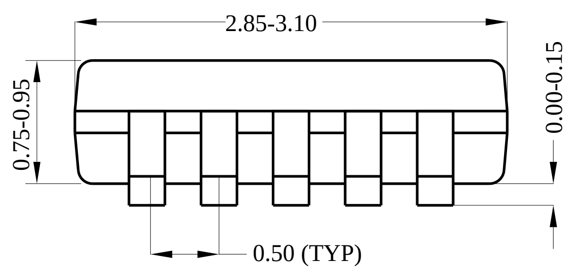
MSOP10 Package Outline & PCB Layout





Recommended Pad Layout



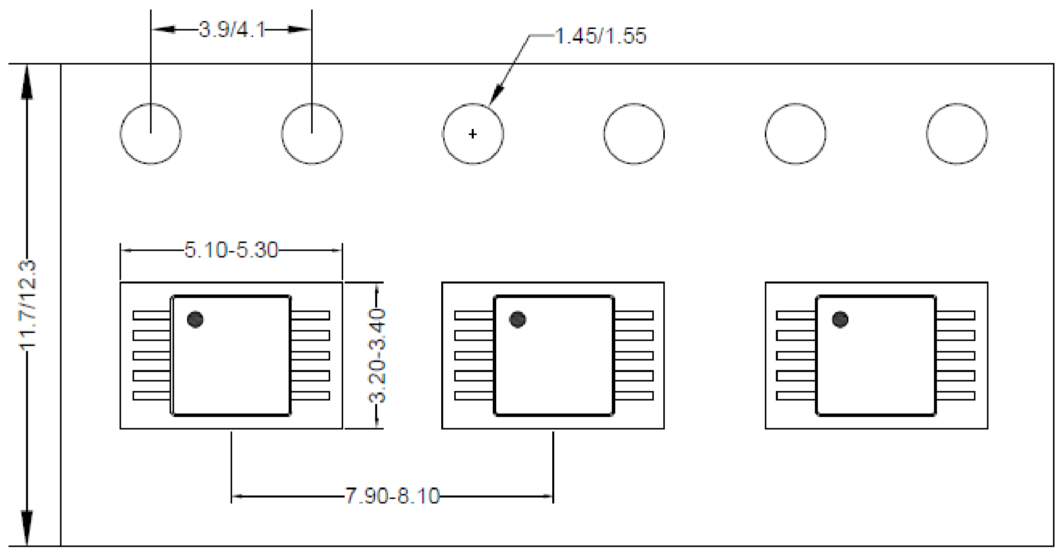


Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

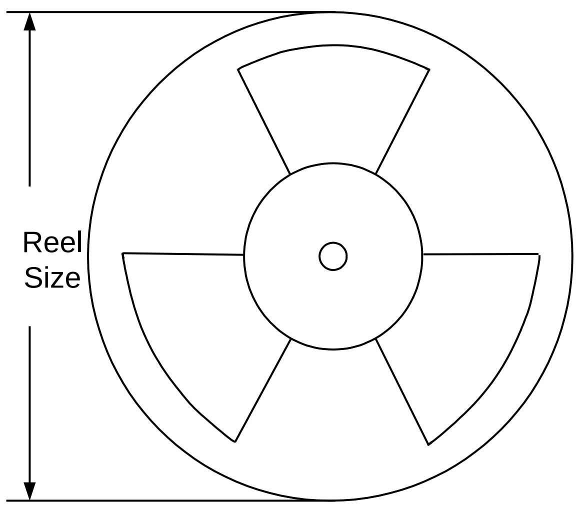
1. Taping Orientation

MSOP10



Feeding direction →

2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
MSOP10	12	8	13"	400	400	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.21, 2021	Revision 0.9	Initial Release

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