SY6986

High Efficiency, 1.6A, Two-Cell Boost Li-Ion Battery Charger with Power Path Management and Cell Balance

General Description

The SY6986 is a 1.6A two-cell synchronous Boost Li-ion battery charger for 3.6-5.5V input voltage, which integrates 500kHz switching frequency and full protection functions. The charge current up to 1.6A can be programmed by external resistor for different portable applications. It also has programmable charge timeout, input current and input voltage DPM functions for safety battery charge operation.

The SY6986 can support supplement mode. When input power cannot support system load, IC will allow the reverse current from battery to support system load together with input power.

The SY6986 supports battery cell balance function to remove voltage difference between two cells and has each cell voltage limit protection during balance.

It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

The SY6986 is available with small QFN3×3 package to provide a small PCB area application.

Ordering Information

SY6986 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6986RAC	QFN3×3-20	

Features

- Integrated Synchronous Boost with 18V Rating Low R_{DSON} FETs for High Charge Efficiency
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Programmable Threshold for Input Voltage DPM Function
- Programmable Threshold for Input Current DPM Function
- Maximum 1.6A Constant Charge Current
- Programmable Constant Charge Current
- Selectable Constant Voltage
- Programmable Charge Timeout
- System Power Path Management Function
- External Separated Control Function for Boost and BATFET
- Up to 200mA Cell Balance Current
- Cell Voltage Limit Protection during Balance
- Battery Pack Temperature Monitor Complying with JEITA Standard
- Input and Charge Status Indication
- Input Voltage UVLO and OVP
- BAT OVP and Short Protection
- Over Temperature Protection
- Low Profile QFN3×3 Package

Applications

- Bluetooth Speaker
- Digital Cameras
- POS
- PSP Game Players, NDS Game Players

Typical Application

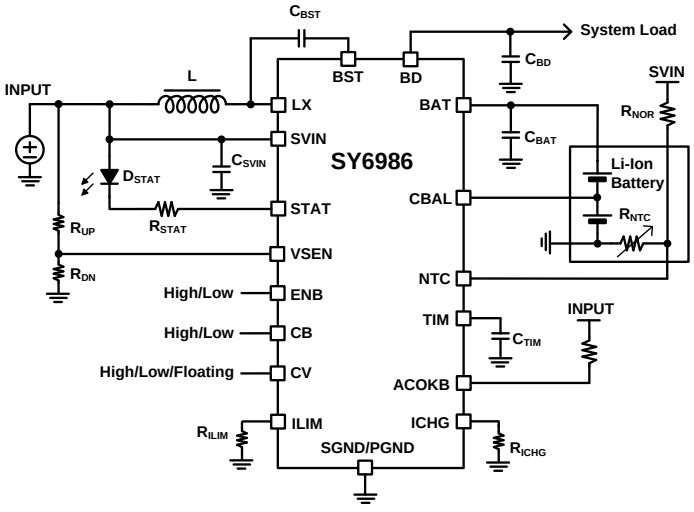
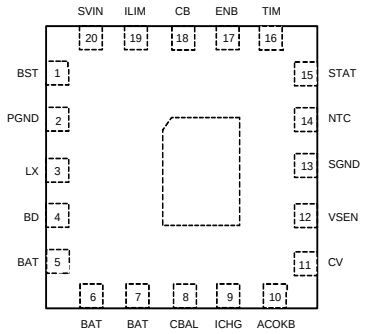


Figure1. Schematic Diagram

Pinout (top view)



(QFN3×3-20)

Top Mark: CTDxyz(device code: CTD, x=year code, y=week code, z=lot number code)

Pin Name	Pin No	Description
BST	1	Boot-strap pin. Supply rectified FET's gate driver. Connect this pin to LX with 0.1μF ceramic capacitor.
PGND	2	Power ground pin.
LX	3	Switch node pin. Connect to external inductor.
BD	4	Boost output pin. Bypass at least 20μF ceramic capacitor to PGND. System load can be drawn from this pin.
BAT	5-7	Battery positive pin.
CBAL	8	Cell balance pin. If cell balance is needed, connect this pin to the middle point of the two-cell batteries. Otherwise, leave this pin floating.
ICHG	9	Charge current program pin. Pull down to ground with a resistor $R_{ICHG.}$ $I_{CC}=(1V/ R_{ICHG})\times10000$, and $I_{TC}=(1V/ R_{ICHG}) \times1000+0.05A$.
ACOKB	10	Input power good indication pin. Open drain output. Pull low when a good input source is present.
CV	11	Battery voltage selection pin. Pull low for 8.4V, float for 8.2V and pull high for 8.7V.
VSEN	12	Input voltage sense pin. If the voltage drops to internal 1.2V reference voltage, the input voltage will be clamped to the setting value. Different resistor configuration on this pin can enable or disable cell balance function.
SGND	13	Signal ground pin.
NTC	14	Thermal sense pin for the battery pack thermal protection.
STAT	15	Charge status and fault indication pin. It is an open-drain output pin and pulled high to SVIN through a LED to indicate the charge in process. When the charge is done, the LED will be off. If any fault happens, the LED will flash with 1.3Hz frequency.
TIM	16	Charge timeout program pin. Connect this pin with a capacitor to ground to program both TC and fast charge (CV&CC) modes' charge time limit. TC charge time limit is about 1/9 of fast charge time limit.
ENB	17	Boost enabled pin. Low logic can enable Boost stage. When ENB pin is pulled high, Boost stage will stop and BATFET will turn on. Do not leave this pin floating.
CB	18	BATFET control pin. Low logic can turn on BATFET. Do not leave this pin floating.
ILIM	19	Input current limit program pin. Connect a resistor R_{ILIM} from this pin to ground to program input current limit. $I_{INLIM} = (1V/R_{ILIM}) \times9000$.
SVIN	20	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage range.
Thermal PAD		Exposed pad under the IC. Always solder Thermal PAD to the board GND area, and have paths on the Thermal PAD plane to dissipate the heat.

Block Diagram

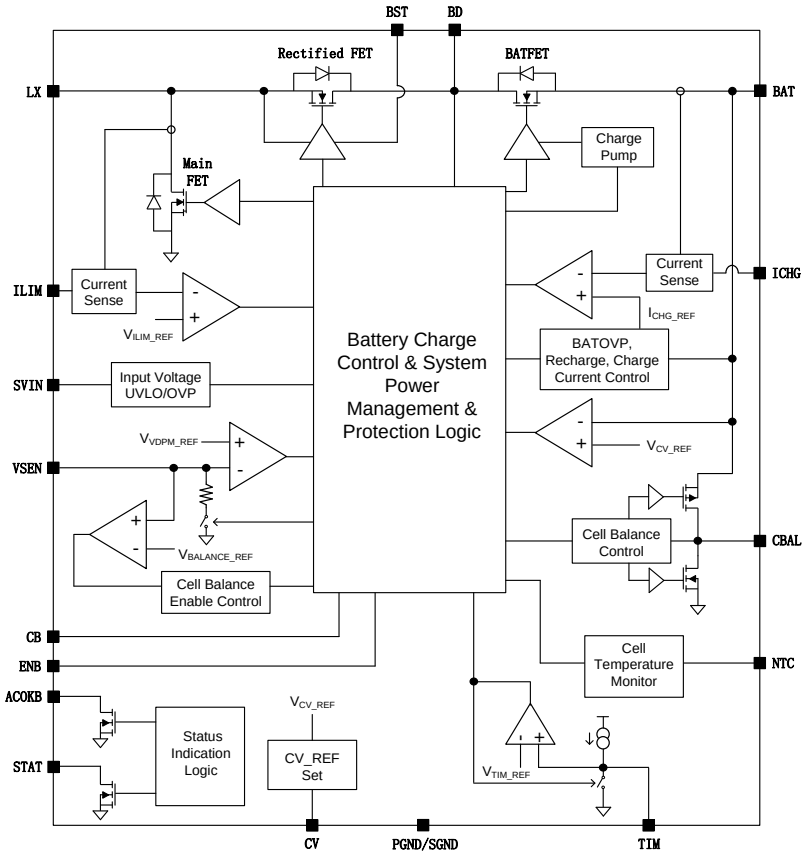


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

SVIN, BAT, LX, BD, NTC, CV, STAT, ENB, CB, ACOKB, VSEN ---------- -0.3V to 18V
CBAL ---------- -0.3V to V_{BAT}
TIM, ICHG , ILIM, BST-LX---------- -0.3V to 4V
Power Dissipation, P_D @ T_A = 25°C, QFN3×3(Note 2)---------- 2.17W
Package Thermal Resistance(Note 3)
θ_{JA} ---------- 62°C/W
θ_{JC} (top) ---------- 19°C/W
Junction Temperature Range ---------- -40°C to 160°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 160°C

Recommended Operating Conditions (Note 4)

SVIN ---------- 3.6V to 5.5V
BAT, LX, BD, NTC, CV, STAT, ENB, CB, ACOKB, VSEN ---------- -0.3V to 16V
CBAL ---------- 0 to V_{BAT}
TIM, ICHG, ILIM, BST-LX---------- -0.3V to 3.6V
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

T_A=25°C, V_{SVIN}=5V, C_{SVIN}=10uF, L=2.2μH, R_{ICHG}=10kΩ, C_{TIM}=330nF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{SVIN})						
Input Voltage Range	V_{SVIN}		3.6		16	V
V_{SVIN} Under Voltage Lockout Threshold	V_{UVLO}	V_{SVIN} rising and measured from V_{SVIN} to GND	3.1	3.3	3.5	V
V_{SVIN} Under Voltage Lockout Hysteresis	ΔV_{UVLO}	Measured from V_{SVIN} to GND		100		mV
Input Overvoltage Protection Threshold	V_{OVP}	V_{SVIN} rising and measured from V_{SVIN} to GND	5.7	5.85	6.0	V
Input Overvoltage Protection Hysteresis	ΔV_{OVP}	Measured from V_{SVIN} to GND		0.5		V
Quiescent Current						
Battery Discharge Current	I_{BAT}	The input source is absent, V_{BAT}=7V, BATFET is on			70	μA
Input Quiescent Current	I_{IN}	V_{SVIN}=V_{NTC}=5V,V_{ENB}>V_H			1.5	mA
Oscillator and PWM						
Switching Frequency	f_{SW}	V_{SVIN}=5V, V_{BAT}=7V, I_{CHG}=1A	400	500	600	kHz
Main FET Minimum On Time	t_{ON_MIN}			100		ns
Main FET Minimum Off Time	t_{OFF_MIN}			100		ns
Power MOSFET						
$R_{DS(ON)}$ of Main FET	R_{FET_M}			50		mΩ
$R_{DS(ON)}$ of Rectified FET	R_{FET_R}			30		mΩ
$R_{DS(ON)}$ of BATFET	R_{FET_B}			45		mΩ
Main FET Peak Current Limit	I_{PEAK_M}		4	4.9	5.8	A
BAT Voltage Regulation						
2-Cell CV Charge Mode Voltage	V_{BAT_REG}	CV pin is floating	8.159	8.2	8.241	V
		V_{CV}<V_{CV_L}	8.358	8.4	8.442	
		V_{CV}>V_{CV_H}	8.656	8.7	8.743	
Recharge Voltage refer to V_{BAT_REG}	ΔV_{RCH}		140	200	260	mV
2-Cell Trickle Charge Mode Voltage Threshold	V_{TC}	Rising edge threshold	5.7	5.8	5.9	V
Battery Short Protection Threshold	V_{SC}	Rising edge threshold	2.35	2.45	2.55	V
Charge Current						
Constant Current	I_{CC}	R_{ICHG}=10kΩ	0.9	1	1.1	A
Trickle Current	I_{TC}		100	150	200	mA
Battery Short Current	I_{SC}		90	150	210	mA
Charge Termination Current	I_{TERM}		75	100	125	mA
BAT Voltage OVP						
Battery Voltage OVP Threshold	V_{BAT_OVP}		105%	110%	115%	V_{BAT_REG}
BD Voltage Regulation						
BD Regulation Voltage with Low Voltage Battery or Battery Removal	V_{BD_REG}	V_{BAT}<V_{TC}	6.5	6.6	6.7	V
BD Regulation Voltage with Normal Voltage Battery, V_{BD}=V_{BAT}+ΔV_{BD_REG}	ΔV_{BD_REG}	V_{BAT}>6.4V, BATFET is off.	200	265	330	mV
BD Over Voltage Protection Threshold	V_{BD_OVP}	Rising edge threshold	9.6	10	10.5	V
BD Over Voltage Protection Threshold Hysteresis	ΔV_{BD_OVP}			250		mV

Input Voltage DPM						
Reference Voltage of VSEN for VDPM	V_{VSEN_VDPM}		1.18	1.2	1.225	V
Input Current Limit						
Input Current Limit Value	I_{INLIM}	R_{ILIM}=9kΩ	0.9	1	1.1	A
Cell Balancing Control						
The Cell Voltage Differential Threshold to Enable Cell Balance	ΔV_{CELL}	V_{BAT}=7.6V		50	80	mV
The Cell Voltage Differential Threshold to Disable Cell Balance	ΔV_{CELL_HYS}	V_{BAT}=7.6V		0		mV
Cell Balance Current	I_{CBAL}	V_{BAT}=7.6V		200		mA
Cell Voltage Limit during Cell Balance	V_{CELL_LIMIT}	CV pin is floating	3.8	3.9	4.0	V
		V_{CV}<V_{CV_L}	3.9	4	4.1	V
		V_{CV}>V_{CV_H}	4.05	4.15	4.25	V
Cell Voltage Limit Hysteresis	ΔV_{CELL_LIMIT}			75		mV
Timer						
Trickle Charge Timeout	t_{TC}	C_{TIM}=330nF	0.45	0.54	0.63	hour
Fast Charge Timeout	$t_{CC\&CV}$		4.1	4.9	5.7	hour
Termination Delay Time	t_{TERM}			30		ms
Recharge Delay Time	t_{RCHG}			20		s
Logic Input Voltage (ENB, CB,CV)						
Logic High Voltage Threshold for ENB, CB	V_H		1.5			V
Logic Low Voltage Threshold for ENB, CB	V_L				0.4	V
Logic High Voltage Threshold for CV	V_{CV_H}		2.6			V
Logic Low Voltage Threshold for CV	V_{CV_L}				0.4	V
NTC Thermal Protection JEITA Spec						
T1(0℃) Threshold	V_{NTC_T1}	V_{NTC} rising	72.55%	73.25%	73.95%	V_{SVIN}
T1(0℃) Threshold Hysteresis	$V_{NTC\_T1\_HYS}$			1.5%		
T2(10℃) Threshold	V_{NTC_T2}	V_{NTC} rising	67.65%	68.25%	68.85%	
T2(10℃) Threshold Hysteresis	$V_{NTC\_T2\_HYS}$			1.5%		
T3(45℃) Threshold	V_{NTC_T3}	V_{NTC} falling	44.25%	44.75%	45.25%	
T3(45℃) Threshold Hysteresis	$V_{NTC\_T3\_HYS}$			1%		
T5(60℃) Threshold	V_{NTC_T5}	V_{NTC} falling	33.875%	34.375%	34.875%	
T5(60℃) Threshold Hysteresis	$V_{NTC\_T5\_HYS}$			1%		
Battery Removal Detection						
Battery Removal Detection Threshold on NTC Pin	V_{NTC_NOBAT}	V_{NTC} rising edge	90%	94%	98%	V_{SVIN}
Battery Removal Detection Hysteresis	ΔV_{NTC_NOBAT}			2%		V_{SVIN}
Battery Removal Detection Delay Time	t_{NOBAT}			20		ms

Thermal Foldback and Thermal Shutdown						
Thermal Foldback Temperature	T_{FDBK}	Temperature rising		120		ºC
Thermal Foldback Temperature Hysteresis	T_{FDBK_HYS}			20		ºC
Thermal Foldback Ratio				0.25		I_{CC}
Thermal Shutdown Temperature	T_{SD}	Temperature rising		160		ºC
Thermal Shutdown Temperature Hysteresis	T_{SD_HYS}			30		ºC

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing IC to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Note 3: θ_{JA} is measured in the natural convection at T_A=25ºC， high effective four layer PCB with thermal via, in accordance with JESD 51-2,-5,-7 thermal measurement standard.

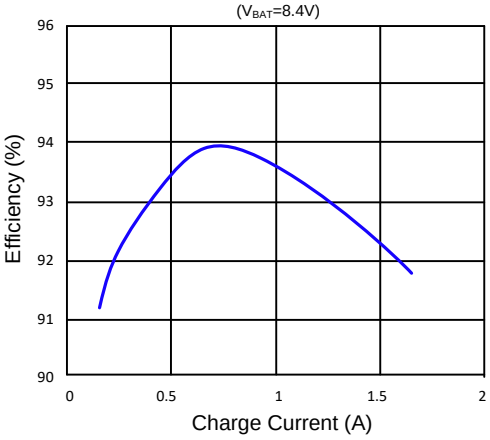
Note 4: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

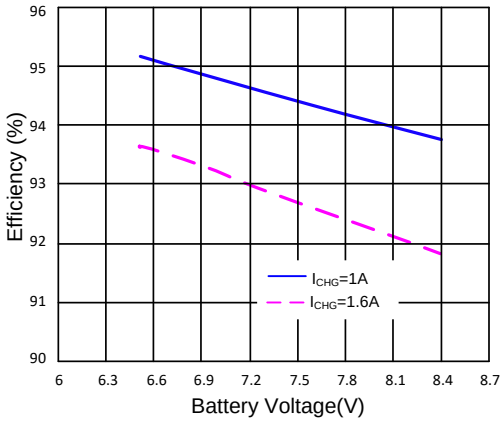
(T_A=25°C, V_{SVIN}=5V, C_{SVIN}=10μF, L=2.2μH, R_{ICHG}=10kΩ, unless otherwise specified.)

Efficiency vs. Charge Current(CV Mode)

(V_{BAT}=8.4V)

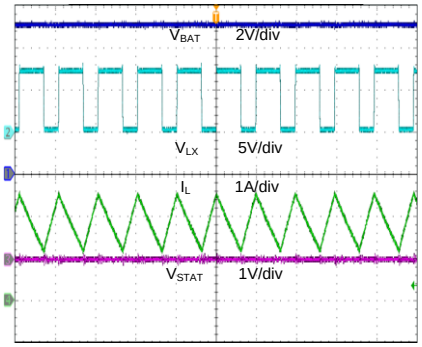


Efficiency vs. Battery Voltage(CC Mode)



Steady Waveform(CC Mode)

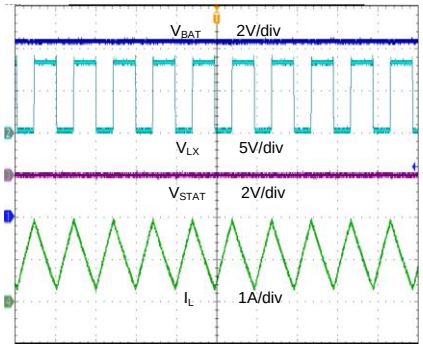
V_{SVIN}=5V, V_{BAT}=7V, I_{CC}=1A



Time(2μs/div)

Steady Waveform(CV Mode)

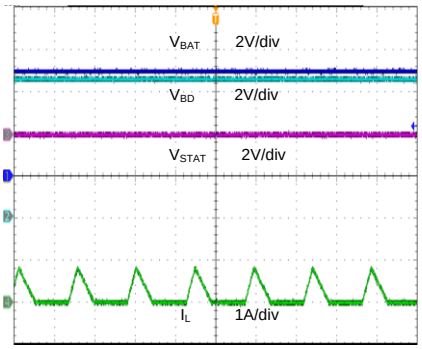
V_{SVIN}=5V, V_{BAT}=8.4V, I_{CHG}=0.6A



Time(2μs/div)

Steady Waveform(TC Mode)

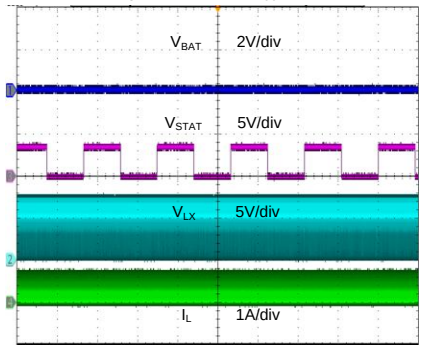
V_{SVIN}=5V, V_{BAT}=5V, I_{CC}=1A



Time(2μs/div)

Steady Waveform(SC Mode)

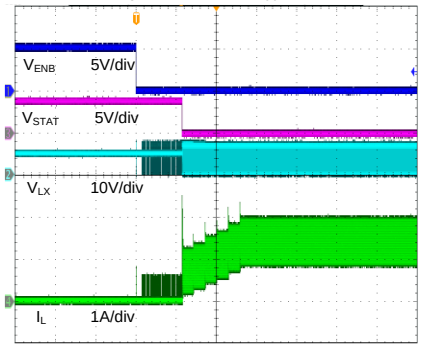
V_{SVIN}=5V, V_{BAT}=0V, I_{CC}=1A



Time(400ms/div)

Start up from ENB

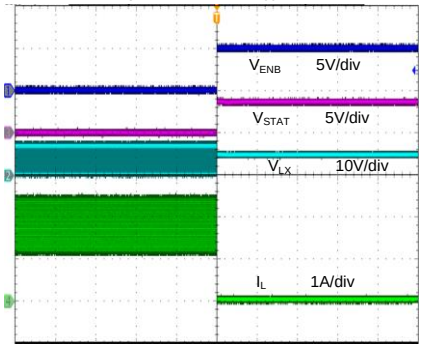
V_{SVIN}=5V, V_{BAT}=7V, I_{CC}=1A



Time(20ms/div)

Shut down from ENB

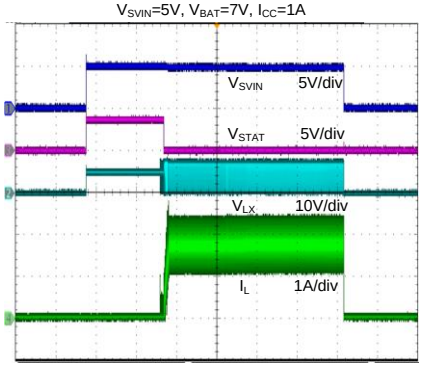
V_{SVIN}=5V, V_{BAT}=7V, I_{CC}=1A



Time(20ms/div)

Adapter Insert/Remove

V_{SVIN}=5V, V_{BAT}=7V, I_{CC}=1A

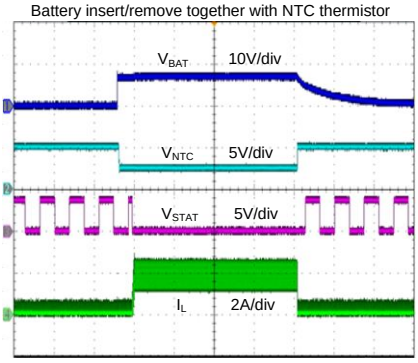


Time(400ms/div)

Battery(NTC) Insert/Remove

V_{SVIN}=5V, V_{BAT}=7V, I_{CC}=1A

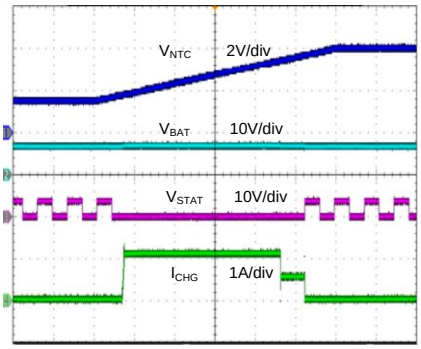
Battery insert/remove together with NTC thermistor



Time(1s/div)

JEITA Function(CC Mode)

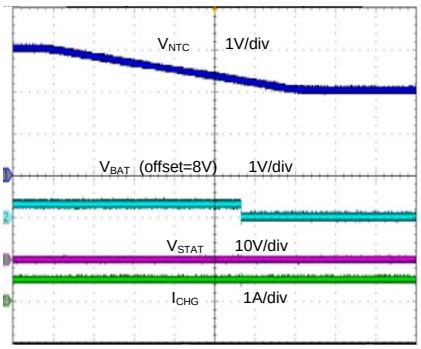
V_{SVIN}=5V, V_{BAT}=7V, I_{CC}=1A



Time(1s/div)

JEITA Function(CV Mode)

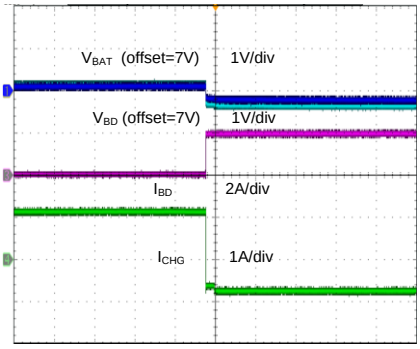
V_{SVIN}=5V, V_{BAT_REG}=8.4V, I_{CHG}=0.5A



Time(400ms/div)

Supplement Function(Charge Ongoing)

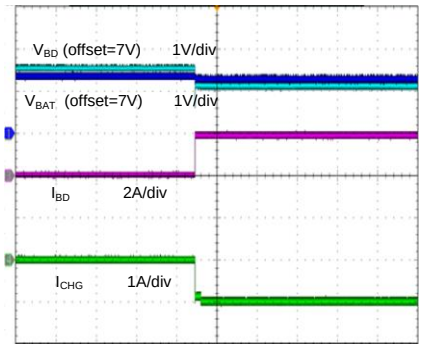
V_{SVIN}=5V, V_{BAT}=7V, I_{CC}=1A



Time(400ms/div)

Supplement Function(Charge Termination)

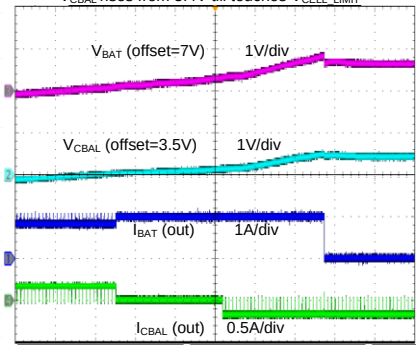
V_{SVIN}=5V, V_{BAT_REG}=8.4V, V_{BAT}=8.3V, I_{CHG}=0A



Time(400ms/div)

Cell Balance and Cell Limit Function

V_{SVIN}=5V, V_{BAT}-V_{CBAL}=3.5V, I_{CC}=1A,
V_{CBAL} rises from 3.4V till touches V_{CELL_LIMIT}



Time(2s/div)

General Function Description

The SY6986 is a 1.6A two-cell synchronous Boost Li-ion battery charger for 3.6-5.5V input voltage, which integrates 500kHz switching frequency and full protection functions. The charge current up to 1.6A can be programmed by external resistor for different portable applications. It also has programmable charge timeout, input current and input voltage DPM functions for safety battery charge operation.

The SY6986 can support supplement mode. When input power cannot support system load, the IC will allow the reverse current from battery to support system load together with input power.

The SY6986 supports battery cell balance function to remove voltage difference between two cells and has each cell voltage limit protection during balance.

ACOKB Indication Description

ACOKB pin will be pulled low when a good adapter is detected.

STAT Indication Description

STAT pin can indicate charge status and faults. Connect a LED from SVIN to STAT pin, LED on means Charge-in-Process, LED off means Charge Done, LED flashing with 1.3Hz frequency means Fault Mode.

1. Charge-In-Process – Pull and keep STAT pin to low;

2. Charge Done – Pull and keep STAT pin to high;

3. Fault Mode – Outputs high and low voltage alternatively with 1.3Hz frequency.

System Fault: Input OVP, BD OVP and Thermal shutdown

Charge Fault: BATOVP, BAT Short Circuit, NTC JEITA UTP/OTP (below T_1 or above T_5), Charge Timeout, Battery Removal

Boost(ENB) and BATFET(CB) Control Logic

1. ENB is high;

Boost is disabled. No matter CB status, BATFET will turn on to support system load if only a normal voltage battery is present.

2. ENB is low.

Boost is enabled. When CB is low, battery charge logic will be active and ready for charge, if CB is high, BATFET will be forced to turn off.

Charge Operation Principle

The whole charge process will go through BAT short, trickle charge, fast charge (CC&CV) and charge termination.

When V_{BAT} is lower than V_{TC}, it is BAT short and trickle charge mode. The linear charge current will be 1/10 of I_{CC}. Before fast charge, BATFET works as linear mode and BD voltage is always regulated at V_{BD_REG}.

When V_{BAT} reaches V_{TC}, it will enter fast charge mode after some time. BATFET turns on completely and the charge current will rise to I_{CC}. During fast charge mode, constant charge current loop is active firstly. When V_{BAT} rises to constant voltage threshold V_{BAT_REG}, constant voltage loop will take over and charge current starts to decrease. When charge current is lower than I_{TERM}, charge termination happens and BATFET will turn off. Boost still works to supply system load and regulate BD voltage at $V_{BAT}+\Delta V_{BD\_REG}$. Then BATFET waits for recharge.

To avoid unexpected result, SY6986 will disable charge termination when VDPM or IDPM is active.

The charge process is showed as below figure:

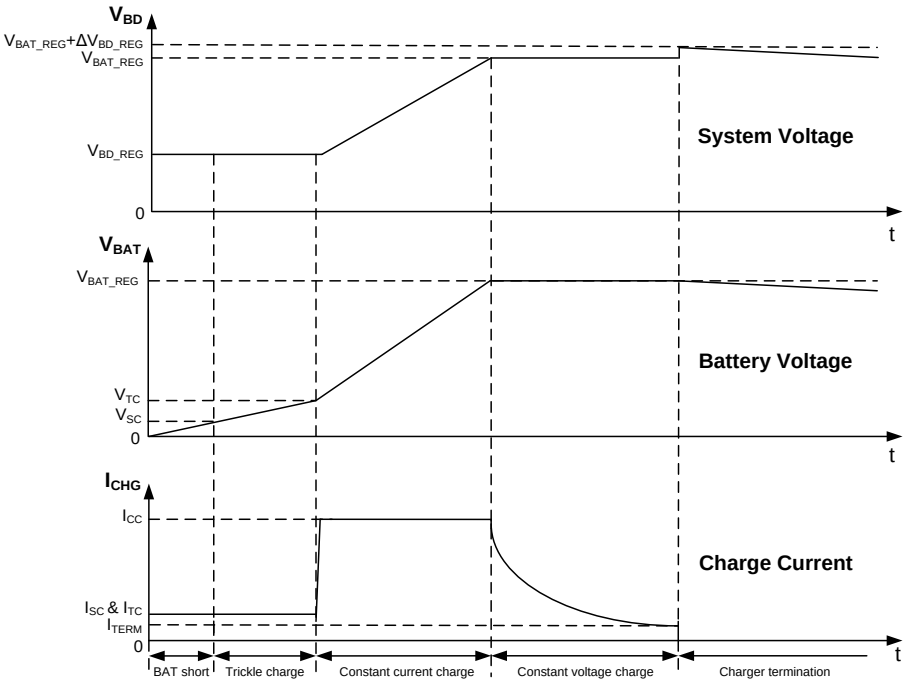


Figure3. Charge Process Diagram

System Power Path Management

SY6986 provides automatic power path selection to supply system load from adapter, battery or both.

(a) When adapter is absent but battery is present, SY6986 will turn on BATFET to provide system load from battery.

(b)When adapter is present but battery is absent (V_{NTC}>V_{NTC_NOBAT}), BATFET will turn off. Boost will regulate BD voltage at V_{BD_REG}. SY6986 will provide system load from adapter.

(c) When adapter and battery are both present, the result is as follow.

If charge is ongoing, SY6986 will provide system load and charge current from adapter.

If charge terminates, SY6986 will turn off BATFET and Boost still works to provide system load from adapter. BD voltage will be regulated at V_{BAT}+ΔV_{BD_REG}.

If charge is disabled by some fault, SY6986 will turn off BATFET and Boost works to provide system load from adapter. BD voltage will be regulated at V_{BD_REG} when V_{BAT}<V_{TC} or V_{BAT}+ΔV_{BD_REG} when battery voltage is high enough.

Under some application where adapter cannot provide enough system power because of input power limit, SY6986 will enter supplement mode. BATFET turns on completely and battery will discharge to provide system load together with adapter.

Protection

The SY6986 has full protections.

When Input OVP, BDOVP or thermal shutdown protection happens, Boost will turn off immediately.

BATFET will turn off when Input OVP or thermal shutdown happens.

When BATOVP, battery removal, NTC thermal protection or charge timeout protection happens, BATFET will turn off. Boost will regulate V_{BD}.

Input Voltage/Current DPM

For prevent input source overloading, SY6986 has IDPM and VDPM loop to limit the input power. It will automatically decrease charge current when input current exceeds setting value or VSEN voltage drops to internal 1.2V reference.

JEITA Guideline Compliance

SY6986 continuously monitors battery temperature by measuring the V_{NTC}, typically determined by a negative temperature coefficient thermistor and an external voltage divider.

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

SY6986 can meet the JEITA requirement. The charge voltage setting at warm temperature (T_3–T_5) can be 300mV (150mV for each cell) lower than V_{BAT_REG}.

The charge current setting at cool temperature (T_1–T_2) can be reduced to 50% of fast charge current I_{CC}.

Detailed function description, refer to the diagram below:

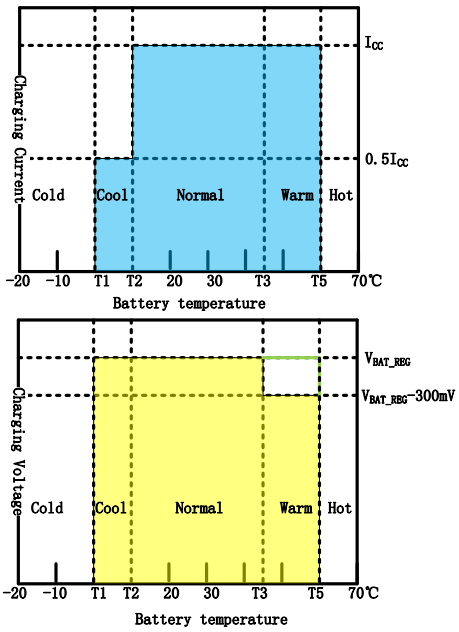


Figure4. JEITA Compliance Diagram

Cell Balance Function

SY6986 implements an internal cell balance control circuit and two power FETs to remove voltage difference between two cells. If the differential voltage between two cells is bigger than ΔV_{CELL}, the cell balance control circuit will turn on one of the power FET to discharge the higher voltage cell.

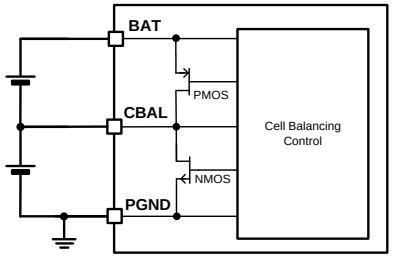


Figure5. Cell Balance Circuit Diagram

SY6986 senses the voltage of each cell. The cell balance circuits start working when below conditions are meet:

1. Cell balance is enabled.
2. V_{BAT}>3.6V
3. The cell voltage difference is bigger than ΔV_{CELL}.

When any cell voltage touches V_{CELL_LIMIT}, SY6986 will turn off BATFET to disable charge until one of below conditions occurs.

1. V_{BAT}<3.6V
2. Cell balance finishes.
3. Two cell voltages are both below the limit voltage.

Cell balance function can also be disabled by setting R_{UP} and R_{DN} on VSEN pin.

Applications Information

Because of the highly integration of SY6986, the application circuit based on this regulator IC is rather simple. Input capacitor, output capacitor, inductor, NTC resistors, and input voltage threshold resistors need to be selected for the targeted applications specifications.

NTC Resistor

SY6986 monitors battery temperature by measuring the SVIN voltage and NTC voltage. It will trigger JEITA protection when the ratio K (K= V_{NTC}/V_{SVIN}) reaches the related threshold.

The temperature sensing network is showed as below.

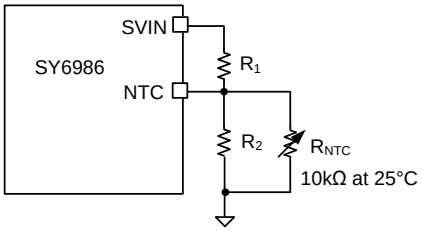


Figure6. NTC Resistors

For JEITA standard, T_1=0ºC, T_2=10ºC, T_3=45ºC, T_5=60ºC.

NTC resistors should be chosen at R_1=5.24kΩ, R_2=30.28kΩ.

Input Capacitor C_{IN}

The ripple current through input capacitor is greater than

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L \times F_{SW} \times V_{OUT}}$$

X5R or X7R ceramic capacitors with greater than 10µF capacitance are recommended to handle this ripple current.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. This ripple voltage is related to the capacitance and its equivalent series resistance (ESR). For the best performance, it is recommended to use X5R or better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required capacitance can be calculated as:

$$C_{OUT} = \frac{I_{CC} \times (V_{OUT} - V_{IN})}{F_{SW} \times V_{OUT} \times V_{RIPPLE}}$$

$V_{RIPPLE}$is the peak to peak output ripple, I_{CC} is the setting charge current.

For SY6986, output capacitor is paralleled by C_{BD} and C_{BAT}, for smaller output ripple noise, each capacitor with greater than 10µF capacitance is recommended.

Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{I_{CC} \times F_{SW} \times 40\%}$$

Where F_{SW} is the switching frequency and I_{CC} is the setting charge current.

The SY6986 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{CC} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Input Voltage DPM

The SY6986 will monitor input voltage by measuring the V_{VSEN}, when V_{VSEN} drops below the internal 1.2V reference, SY6986 will decrease the duty cycle to control the charge current.

The input voltage sense network is showed as below, choose R_{UP}, R_{DN} to set the input voltage threshold V_{IN_VDPM}:

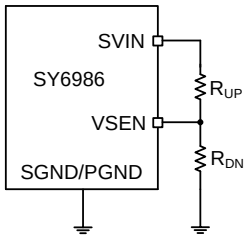


Figure7. Input Voltage Sense Network

$$V_{IN\_VDPM} = \frac{V_{VSEN\_VDPM} \times (R_{DN} + R_{UP})}{R_{DN}}, V_{VSEN\_VDPM} = 1.2V$$

Notice that R_{DN} should be selected at 3.3kΩ or 100kΩ for cell balance application.

Cell Balance Enable

The SY6986 can enable or disable cell balance function by setting proper R_{UP} and R_{DN} value on VSEN pin.

If cell balance is needed, set R_{DN} as 3.3kΩ.

If cell balance is not needed, set R_{DN} as 100kΩ and leave CBAL floating.

Layout Design

Efficient PCB layout is critical to achieve good regulation, ripple rejection, transient response, and thermal performance. It is recommended highly to duplicate the EVB layout for optimum performance. If changes are necessary, refer to the Figure8 and guidelines as below:

The layout design of SY6986 is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{SVIN}, L, and C_{BD}.

1) The loop of main FET, rectified FET, and C_{BD} must be as small as possible.
2) To achieve the best thermal and noise performance, it is desirable to maximize the PCB copper area connecting to SGND/PGND pin and the thermal pad, add more vias to the thermal pad to help heat dissipation.
3) C_{SVIN} must be close to pin SVIN and GND.
4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
5) The small signal components R_{ILIM}, R_{ICHG}, R_{UP} and R_{DN} must be placed close to IC and must not be adjacent to the LX net on the PCB layout to avoid the noise problem.
6) CBAL pin should be connected to middle point of the 2-cell battery pack as close as possible to minimize voltage drop on the CBAL trace line when cell balance is ongoing.

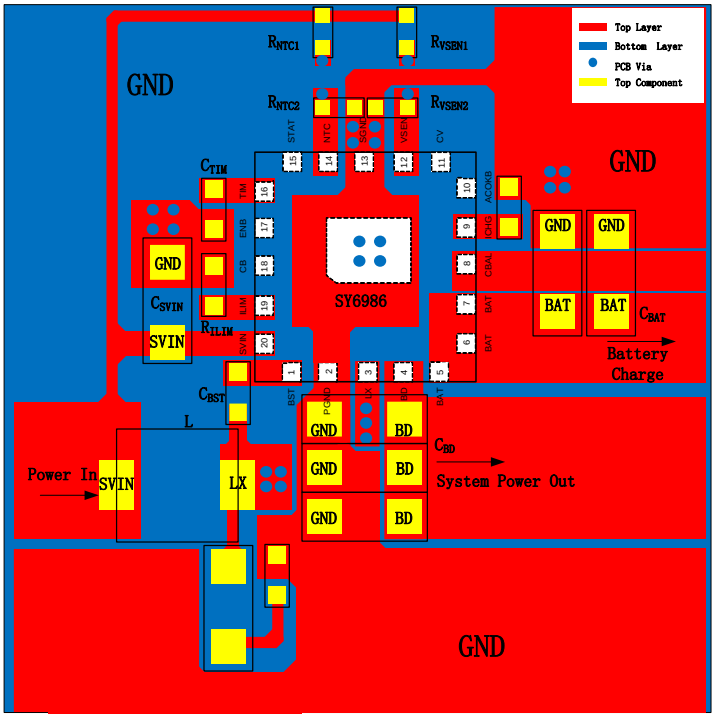
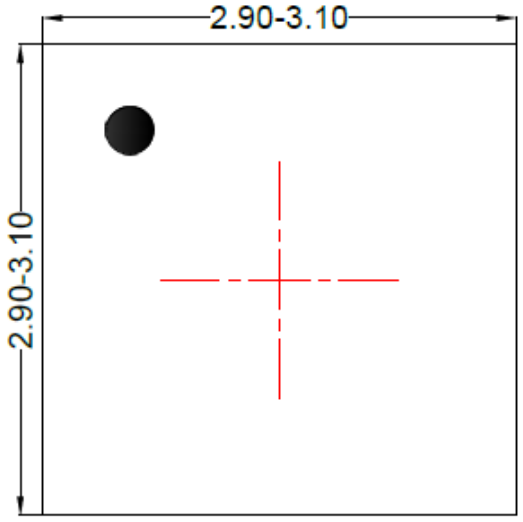
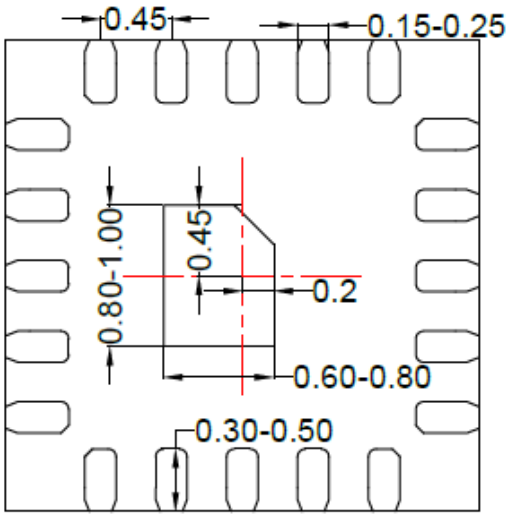


Figure8. Proposed PCB Layout

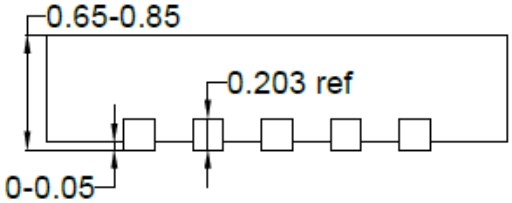
QFN3×3-20 Package Outline



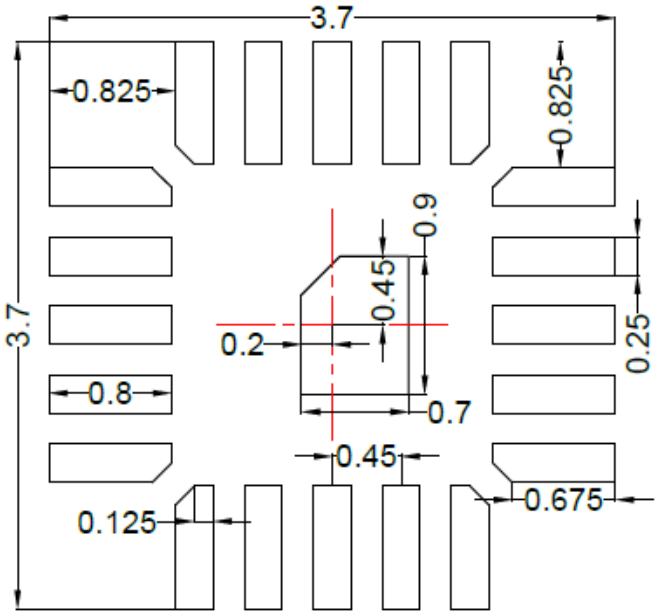
Top view



Bottom view



Side view



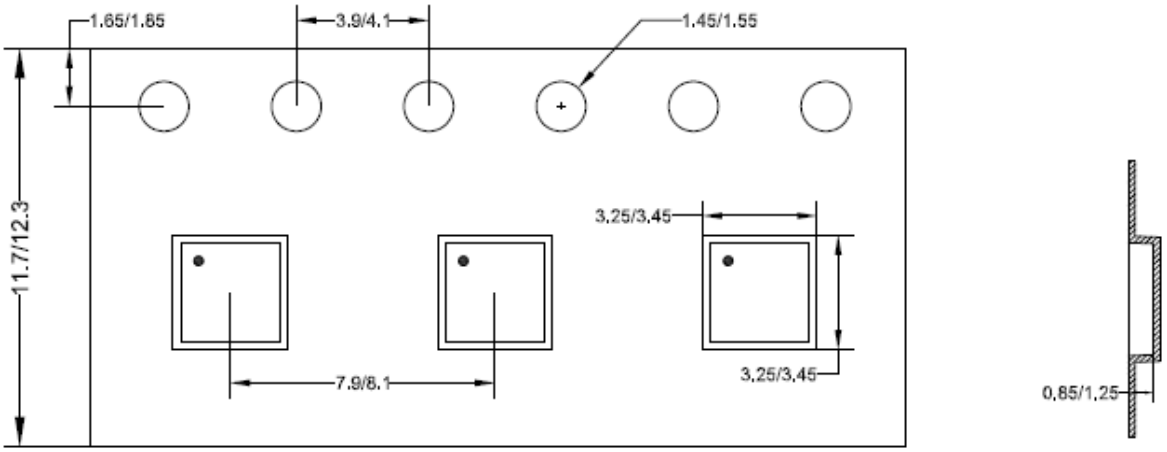
Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;
2, Center line refers the chip body center

Taping & Reel Specification

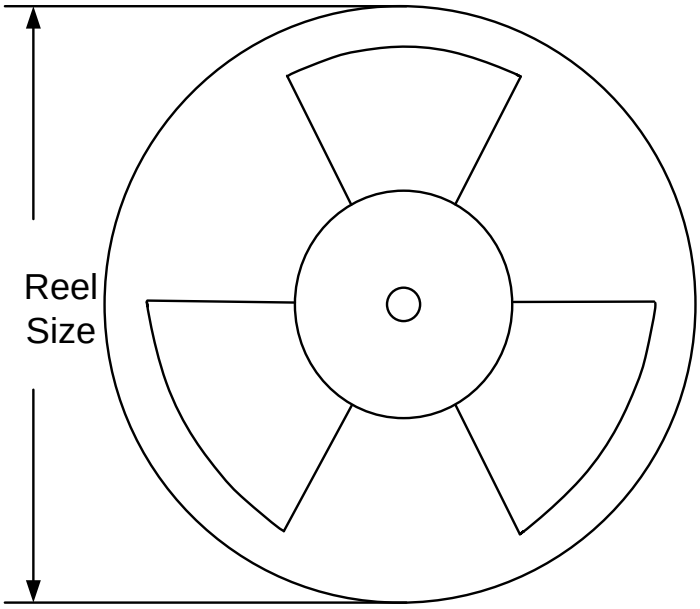
1. Taping Orientation

QFN3×3-20



Feeding Direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN3×3-20	12	8	13"	400	400	5000

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