SY8631B

6-channel PMIC with 2 Step Down Buck Regulators, 3 Low Dropout LDO and 1 Channel RESET Output

General Description

SY8631B is integrated Power Management IC for applications powered by one Li-ion or Li-Polymer cell which require multiple power rails. It integrates 2 step-down Buck regulators, 3 low dropout LDOs and 1 channel RESET output. The highly efficient, 2.2MHz step-down Buck regulators will target at providing the core voltage and I/O voltage in a processor based system. Each LDO operates with an input voltage range between 1.8V and 5.5V allowing them to be supplied from one of the step-down converters or directly from the Li-ion battery.

SY8631B operates over a wide input voltage range from 2.5V to 5.5V to optimize the device for 5V, 3.3V or Li-ion battery applications.

Ordering Information

SY8631 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8631BQCC	QFN4x4-24	----

Features

- Input voltage range: 2.5V to 5.5V
- Input voltage range for LDOs : 1.8V to 5.5V
- 2 channels DCDC regulators and 3 channels LDO regulators
- 1A output current capability for each DC/DC regulator
- DC/DC regulators output voltage externally adjustable
- 2.2MHz switching frequency
- Power save mode at light load condition for higher efficiency
- Forced-PWM mode selection by Mode pin
- Total 38uA quiescent current for DC/DC regulators
- 400mA output current capability for LDO1
- 200mA output current capability for LDO2 and LDO3
- LDO1, LDO2 output voltage externally adjustable
- Fixed 1.5V output voltage for LDO3
- Hard short protection, thermal shut down protection
- RoHS Compliant and Halogen Free
- Compact package: QFN4x4-24

Applications

- Cell Phones, Smart-Phones
- WLAN
- PDAs, Pocket PCs, GPS
- Portable Media Players
- Digital Cameras

Typical Applications

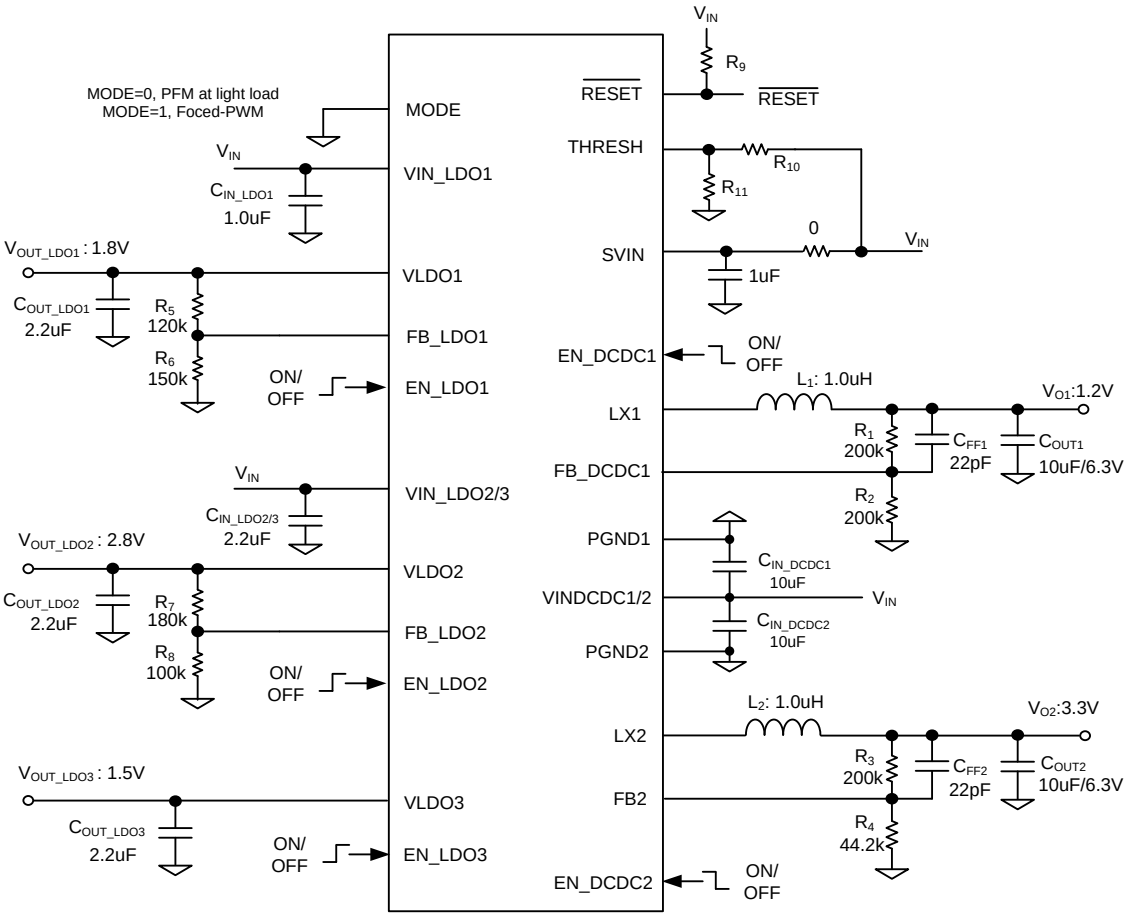
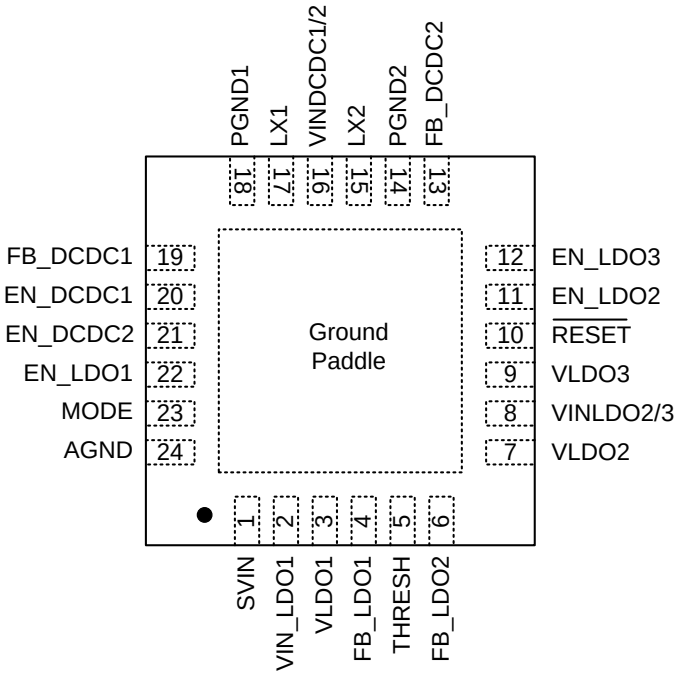


Figure 1. Schematic diagram

Pinout (Top View)



Top Mark: BDD***xyz*** **(**Device code: BDD, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
SVIN	1	Power supply for digital and analog circuitry of DCDC1, DCDC2 and LDOs. Decouple this pin to GND with at least 1uF ceramic cap. This pin must be connected to the same voltage supply with VINDCDC1/2.
VIN_LDO1	2	Input voltage for LDO1. Decouple this pin to GND with 1uF ceramic.
VLDO1	3	Output pin for LDO1. Decouple this pin to GND with at least 2.2uF ceramic cap.
FB_LDO1	4	Feedback pin for LDO1. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{LDO1}=(1+R_5/R_6)x1.0V$.
THRESH	5	Reset input detect pin. 0.99V internal reference for $\overline{\text{RESET}}$ function.
FB_LDO2	6	Feedback pin for LDO2. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{LDO2}=(1+R_7/R_8)x1.0V$.
VLDO2	7	Output pin for LDO2. Decouple this pin to GND with at least 2.2uF ceramic cap.
VINLDO2/3	8	Input pin for LDO2 and LDO3. Decouple this pin to GND with at least 2.2uF ceramic cap.
VLDO3	9	Output pin for LDO3. Fixed 1.5V output. Decouple this pin to GND with at least 2.2uF ceramic cap.
$\overline{\text{RESET}}$	10	Open drain active low $\overline{\text{RESET}}$ output, fixed 100ms $\overline{\text{RESET}}$ delay time
EN_LDO2	11	Enable pin for LDO2. Pull high to turn on LDO2 or low to turn off. Do not leave it floating.
EN_LDO3	12	Enable pin for LDO3. Pull high to turn on LDO3 or low to turn off. Do not leave it floating.
FB_DCDC2	13	Feedback pin for DCDC2. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage:

		$V_{O2}=(1+R_3/R_4)x0.6V$.
PGND2	14	Ground pin for DCDC2.
LX2	15	Switching node for DCDC2. Connect it to inductor.
VINDCDC1/2	16	Input pin for DCDC1 and DCDC2. Decouple this pin to GND with at least 2pcs 10uF ceramic caps for each channel.
LX1	17	Switching node for DCDC1. Connect it to inductor.
PGND1	18	Ground pin for DCDC1.
FB_DCDC1	19	Feedback pin for DCDC1. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{O1}=(1+R_1/R_2)x0.6V$.
EN_DCDC1	20	Enable pin for DCDC1. Pull high to turn on DCDC1 or low to turn off. Do not leave it floating.
EN_DCDC2	21	Enable pin for DCDC2. Pull high to turn on DCDC2 or low to turn off. Do not leave it floating.
EN_LDO1	22	Enable pin for LDO1. Pull high to turn on LDO1 or low to turn off. Do not leave it floating.
MODE	23	Mode selection pin for DCDC1 and DCDC2. MODE=low, PFM mode operation at light load condition. MODE=high, forced PWM mode operation.
AGND	24	Analog ground pin.

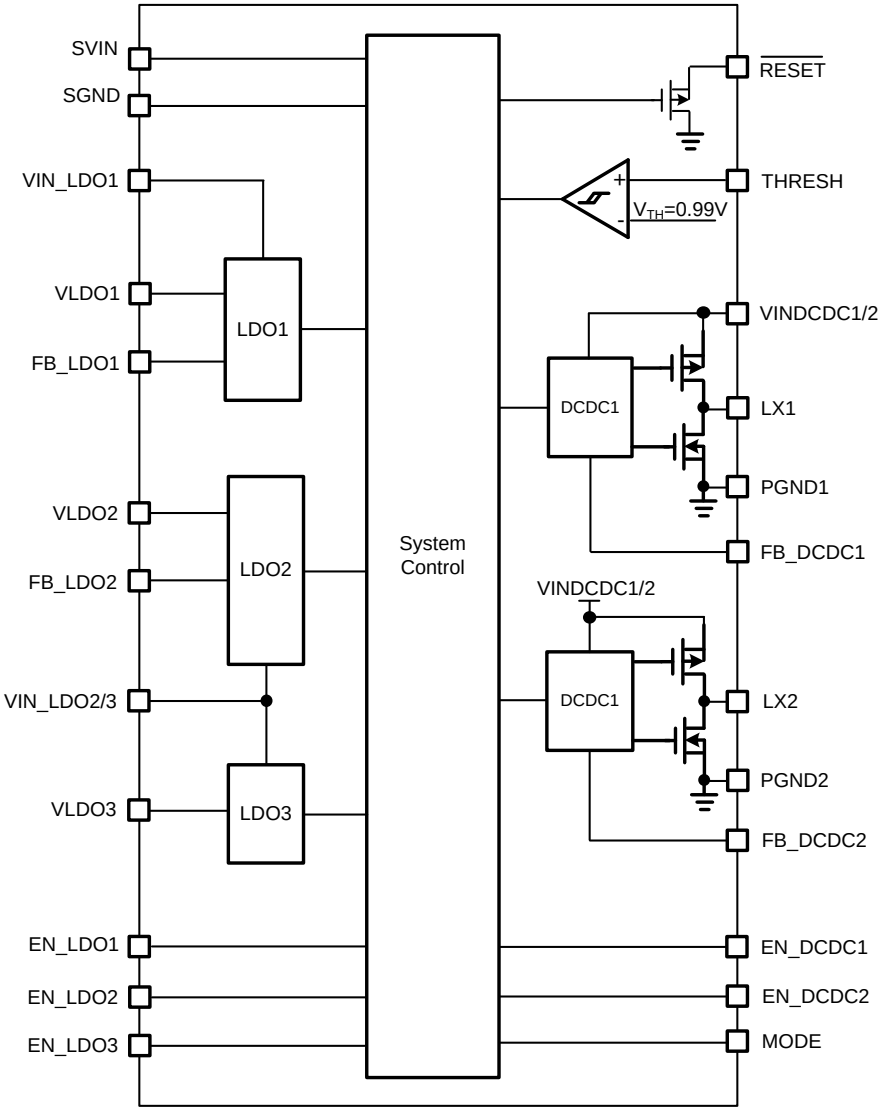
Absolute Maximum Ratings (Note 1)

All pins ---------- 6V
Power Dissipation, PD @ T_A = 25°C QFN4x4-24---------- 4W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 32°C/W
θ_{JC_TOP} ---------- 20°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Block Diagram



Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO threshold	$V_{IN,ON}$	V_{IN} rise, 0→3V			2.45	V
	$V_{IN,OFF}$	V_{IN} fall, 3V→0	2.05			V
Quiescent Current	I_{Q1}	One regulator on, I_{OUT} = 0, Mode = GND, device not switching, EN_DCDC1=Vin or EN_DCDC2=Vin; EN_LDO1/2/3=GND		27		µA
	I_{Q2}	Two regulators on: EN_DCDC1=EN_DCDC2=Vin, Mode = GND, device not switching, I_{OUT1}=I_{OUT2}=0; EN_LDO1/2/3= GND		37		
	I_{Q3}	All regulators on: DCDC1 and DCDC2: EN_DCDC1= EN_DCDC2= Vin, Mode = GND, device not switching, I_{OUT1} = I_{OUT2}=0 , LDO1, LDO2, LDO3: EN_LDO1/2/3=Vin, I_{LDO1}= I_{LDO2}=I_{LDO3}=0		150		
Shutdown Current	I_{SHDN}	EN_DCDC1/2=0 EN_LDO1/2/3=0		9	12	µA
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C
EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, MODE						
Logic rising threshold	V_{ENH}, V_{MODEH}		1.2			V
Logic falling threshold	V_{ENL}, V_{MODEL}				0.4	V
DCDC1 and DCDC2 Regulators						
DCDC1 and DCDC2 Feedback Reference Voltage	V_{REF1}, V_{REF2}		0.591	0.6	0.609	V
DCDC1/2 PFET $R_{DS(ON)}$	$R_{DS(ON),P1}$, $R_{DS(ON),P2}$	V_{IN}=5V		170		mΩ
DCDC1/2 NFET $R_{DS(ON)}$	$R_{DS(ON),N1}$, $R_{DS(ON),N2}$	V_{IN}=5V		130		mΩ
DCDC1/2 peak current limit	I_{LIM1}, I_{LIM2}		1.5			A
Oscillator Frequency	F_{OSC1}, F_{OSC2}			2.2		MHz
Min ON Time	$t_{MIN,ON}$			80		ns
Soft-start time	t_{ss}	Time to ramp from 5% to 95% of V_{OUT}		500		us
DCDC discharge resistor	R_{DIS1}, R_{DIS2}			30		Ω
$\overline{\text{RESET}}$ **Output**						

$\overline{\text{RESET}}$ delay time	t_{RESET}	V_{IN}=5V, V_{TH}: 0-->1.2V.	80	100	120	ms
$\overline{\text{RESET}}$ output low resistance		V_{IN}=5V, V_{TH}=0		100		Ω
THRESH pin threshold to pull low $\overline{\text{RESET}}$ pin	V_{TH}	Falling threshold	0.97	0.99	1.01	V
THRESH hysteresis voltage	$V_{TH,HYS}$			50		mV
LDO Regulators						
LDO input voltage range	V_{INLDO1}, $V_{INLDO2/3}$		1.8		5.5	V
Feedback Reference voltage for LDO1 and LDO2	$V_{REF,LDO1}$, $V_{REF,LDO2}$		0.99	1	1.01	V
LDO3 output voltage	V_{LDO3}		1.485	1.5	1.515	V
Maximum output current for LDO1	$I_{OUT,LDO1}$		400			mA
LDO1 short current limit	$I_{SC,LDO1}$			600		
Maximum output current for LDO2	$I_{OUT,LDO2}$		200			mA
LDO2 short current limit	$I_{SC,LDO2}$			300		mA
Maximum output current for LDO3	$I_{OUT,LDO3}$		200			mA
LDO3 short current limit	$I_{SC,LDO3}$			300		mA
Line regulation for LDO1, LDO2 and LDO3		V_{SVIN}=$V_{INLDO1,2}$ = $V_{LDO1,2}$+0.5V(min. 2.5V) to 5.5V, Io= 10 mA	-1%		1%	
Load regulation for LDO1, LDO2, LDO3		V_{SVIN}=V_{IN_LDO1}=$V_{IN\_LDO2/3}$=5V, Io = 0 to full load	-1%		1%	
LDO1 soft-start time	T_{SS_LDO1}			240		us
LDO2 soft-start time	T_{SS_LDO2}			240		us
LDO3 soft-start time	T_{SS_LDO3}			120		us
LDO discharge resistor	$R_{DIS, LDO1}$, $R_{DIS, LDO2}$, $R_{DIS, LDO3}$	V_{IN}=5V, V_{EN_LDO1}=V_{EN_LDO2}=V_{EN_LDO3}=0		400		Ω
LDO1 Dropout voltage	$V_{DROP,LDO1}$	V_{SVIN} =5V, V_{INLDO1}=1.8V, I_{OUT}=400mA,			280	mV
LDO2 Dropout voltage	$V_{DROP,LDO2}$	V_{SVIN} =5V, $V_{INLDO2/3}$=2.8V, I_{OUT}=200mA,			280	mV
LDO3 Dropout voltage	$V_{DROP,LDO3}$	V_{SVIN} =5V,$V_{INLDO2/3}$=1.5V, I_{OUT}=200mA,			280	mV

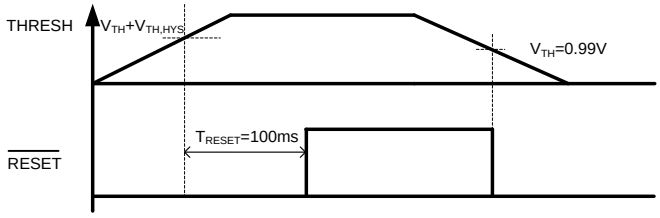
Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ JA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

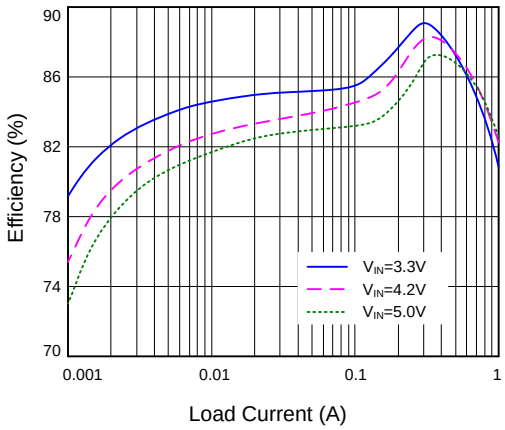
RESET OUTPUT function

SY8631B internally integrates $\overline{\text{RESET}}$ output function for the processor with a 100ms delay time. The input voltage is sensed on THRESH pin. The circuitry is functional as soon as the supply voltage at SVIN exceeds UVLO threshold. When V_{IN}>UVLO and THRESH pin voltage is lower than V_{TH}(0.99V), $\overline{\text{RESET}}$ output is pulled low, if THRESH pin voltage exceeds $V_{TH}+V_{TH,HYS}$ threshold, $\overline{\text{RESET}}$ output goes high after fixed 100ms delay time. The $\overline{\text{RESET}}$ circuitry is active even all DCDC converters and LDOs are disabled.

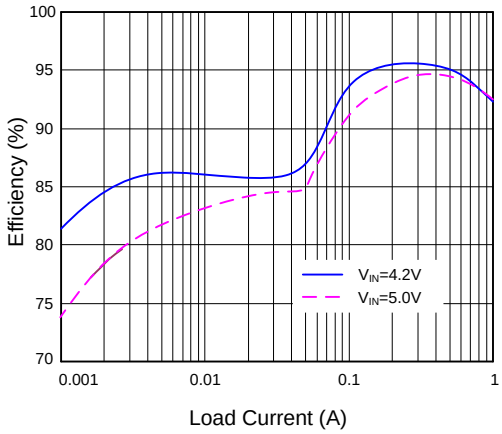


Typical Performance Characteristics

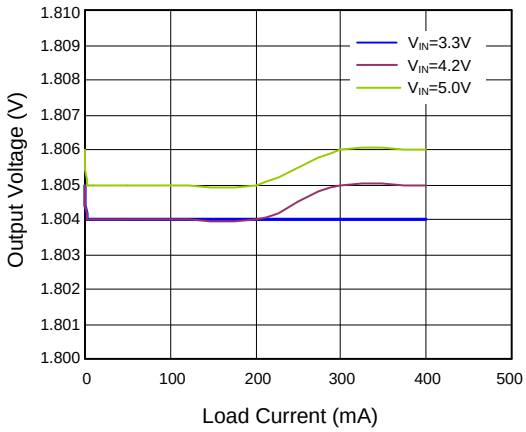
Efficiency vs. Load Current (DCDC1)



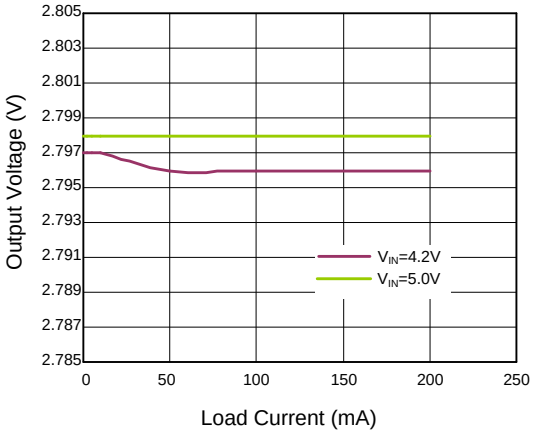
Efficiency vs. Load Current (DCDC2)



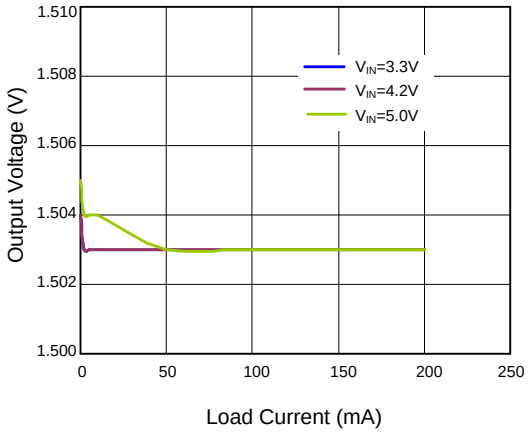
LDO1 Load Regulation



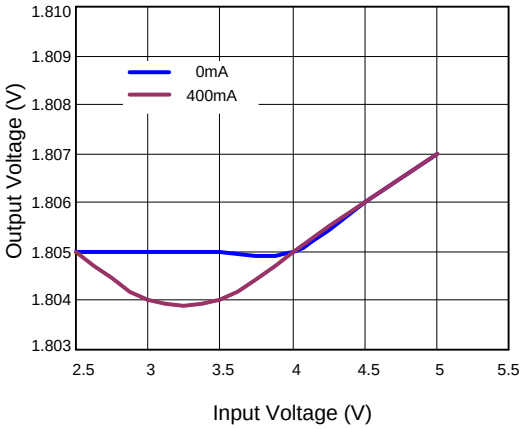
LDO2 Load Regulation



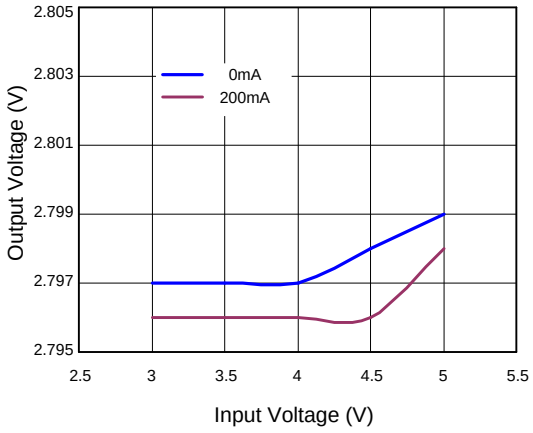
LDO3 Load Regulation



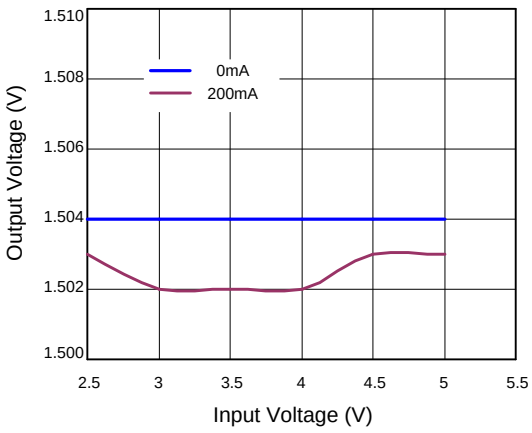
LDO1 Line Regulation



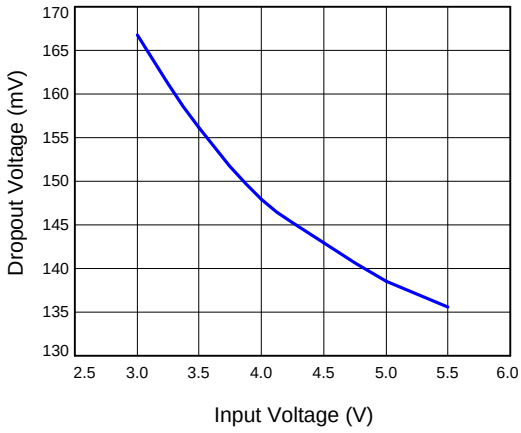
LDO2 Line Regulation



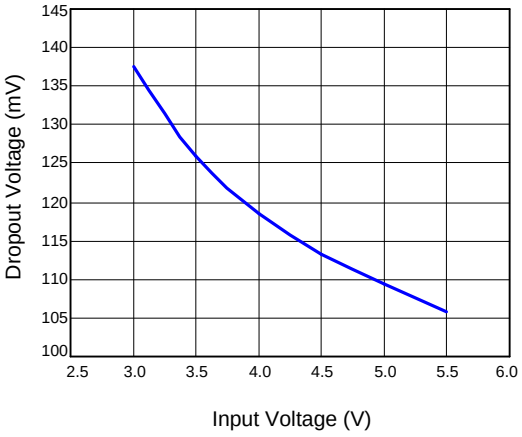
LDO3 Line Regulation



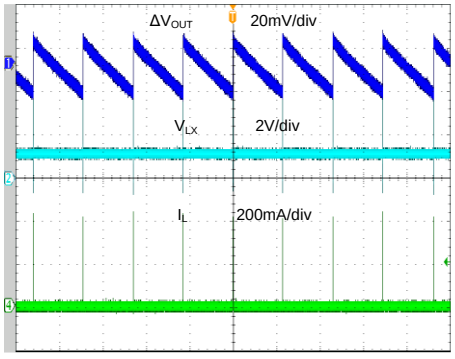
LDO1 Dropout Voltage vs. Input Voltage



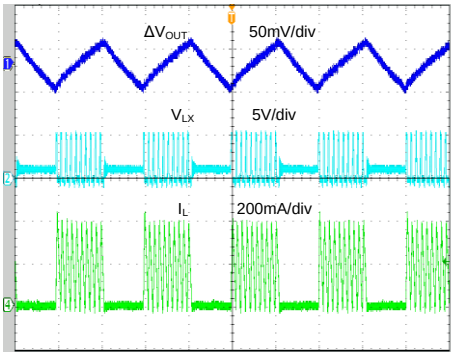
LDO2 Dropout Voltage vs. Input Voltage



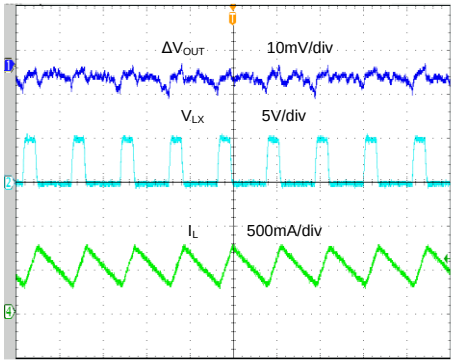
Steady State (DCDC1)
(V_{IN}=5V, V_{OUT}=1.2V, I_O=0)



Steady State (DCDC1)
(V_{IN}=5V, V_{OUT}=1.2V, I_O=0.1A)

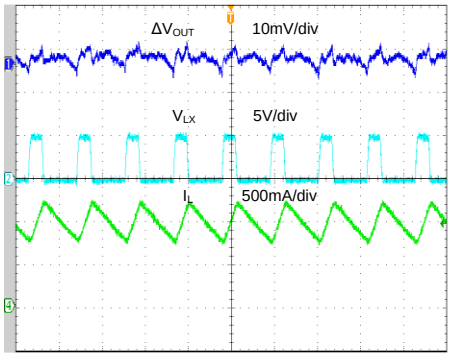


Steady State (DCDC1)
(V_{IN}=5V, V_{OUT}=1.2V, I_O=0.5A)



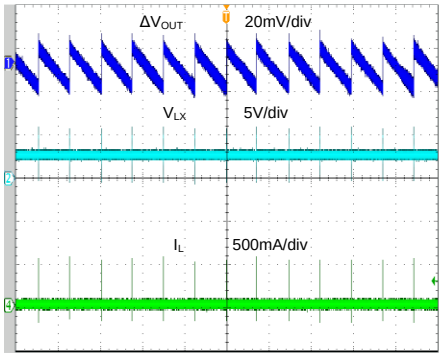
Time (400ns/div)

Steady State (DCDC1)
(V_{IN}=5V, V_{OUT}=1.2V, I_O=1A)



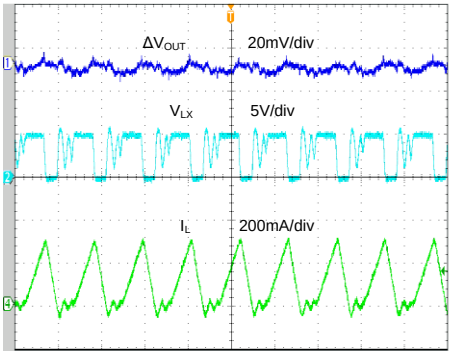
Time (400ns/div)

Steady State (DCDC2)
(V_{IN}=5V, V_{OUT}=3.3V, I_O=0)



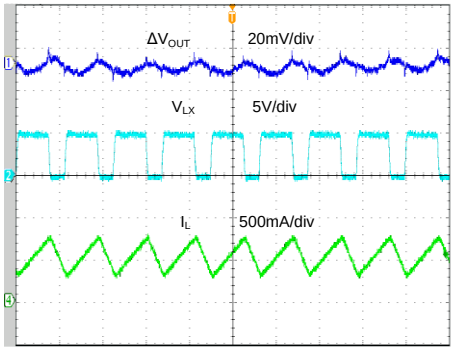
Time (4ms/div)

Steady State (DCDC2)
(V_{IN}=5V, V_{OUT}=3.3V, I_O=0.1A)



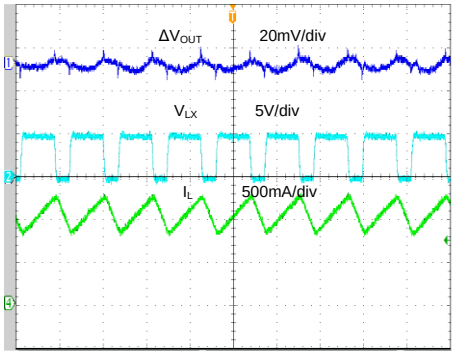
Time (400ns/div)

Steady State (DCDC2)
(V_{IN}=5V, V_{OUT}=3.3V, I_O=0.5A)



Time (400ns/div)

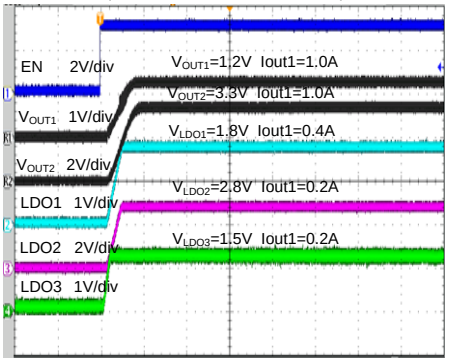
Steady State (DCDC2)
(V_{IN}=5V, V_{OUT}=3.3V, I_O=1A)



Time (400ns/div)

Startup from Enable

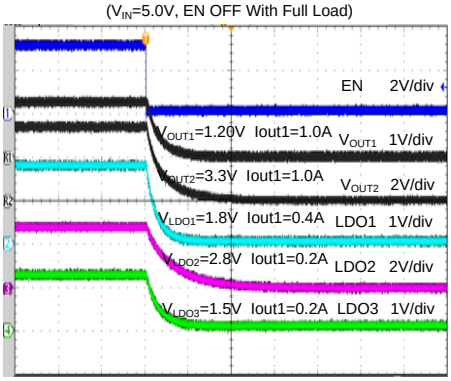
(V_{IN}=5.0V, EN ON With Full Load)



Time (800μs/div)

Shutdown from Enable

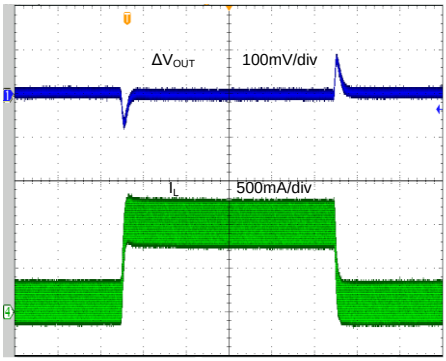
(V_{IN}=5.0V, EN OFF With Full Load)



Time (40μs/div)

Load Transient

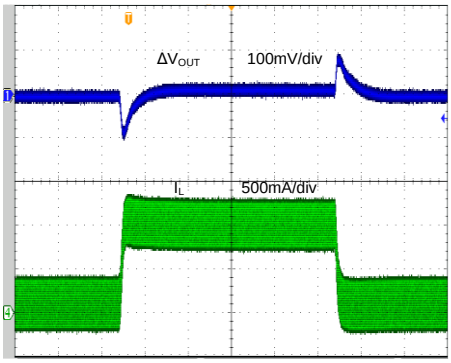
(DCDC1, V_{IN}=5.0V, Vout=1.2V, I_O=0 ~ 1.0A, FCCM)



Time (100μs/div)

Load Transient

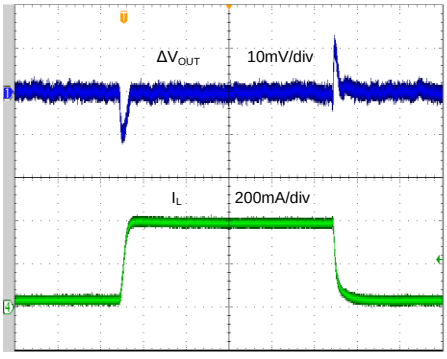
(DCDC2, V_{IN}=5.0V, Vout=3.3V, I_O=0 ~ 1.0A,FCCM)



Time (100μs/div)

Load Transient

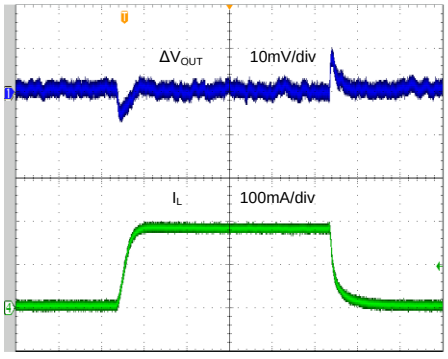
(LDO1, V_{IN}=5V, $V_{IN,LDO1}$=3.3V,V_{LDO1}=1.8V, Io=40 ~ 400mA)



Time (100μs/div)

Load Transient

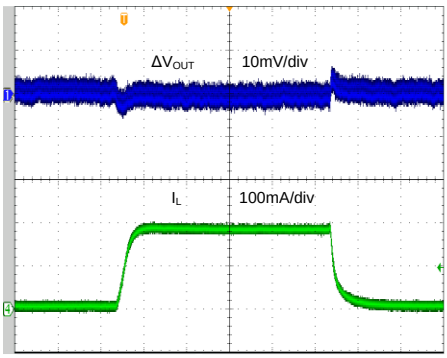
(LDO2, V_{IN}=5V, $V_{IN,LDO2}$=3.3V,V_{LDO2}=2.8V, I_O=20 ~200mA)



Time (100μs/div)

Load Transient

(LDO3, V_{IN}=5V, $V_{IN,LDO3}$=3.3V, V_{LDO3}=1.5V, I_O=20 ~200mA)



Time (100μs/div)

Operation

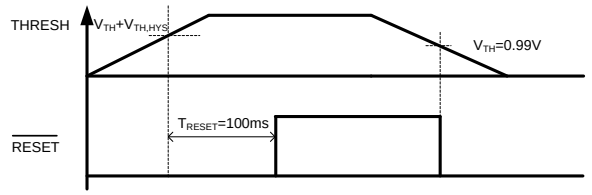
SY8631B is integrated Power Management IC for applications powered by one Li-ion or Li-Polymer cell which require multiple power rails. It integrates with 2 step-down Buck regulators, 3 low dropout LDOs and 1 channel $\overline{\text{RESET}}$ output. The highly efficient, 2.2MHz step-down Buck regulators will target at providing the core voltage and I/O voltage in a processor based system. Each LDO operates with an input voltage range between 1.8V and 5.5V allowing them to be supplied from one of the step-down converters or directly from the Li-ion battery.

SY8631B operates over a wide input voltage range from 2.5V to 5.5V to optimize the device for 5V, 3.3V or Li-ion battery applications.

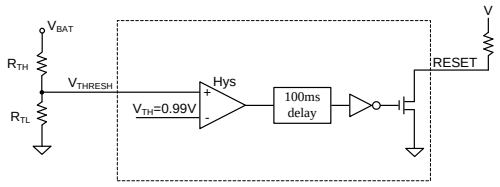
Applications Information

$\overline{\text{RESET}}$ OUTPUT Function:

SY8631B internally integrates $\overline{\text{RESET}}$ output function for the processor with a 100ms delay time. The input voltage is sensed on THRESH pin. The circuitry is functional as soon as the supply voltage at SVIN exceeds UVLO threshold. When V_{IN}>UVLO and THRESH pin voltage is lower than V_{TH}(0.99V), $\overline{\text{RESET}}$ output is pulled low, if THRESH pin voltage exceeds $V_{TH}+V_{TH,HYS}$, $\overline{\text{RESET}}$ pin output goes high after fixed 100ms delay time. The $\overline{\text{RESET}}$ circuitry is active even all DCDC converters and LDOs are disabled.



The resistor divider R_{TH} and R_{TL} connect to THRESH pin are used to program the proper sense voltage. To minimize the power consumption, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 100kΩ and 1MΩ is highly recommended for both resistors. For example, in a battery supply system, 3.0V falling threshold is desired to pull low the $\overline{\text{RESET}}$ pin to reset the system, and choose R_{TL}=500k, since V_{TH}=0.99V, then R_{TH} can be calculated to be 246k.



$$R_{TH} = \frac{V_{TH}}{V_{BAT} - V_{TH}} R_{TL}$$

Mode Selection

The MODE pin is used to select forced PWM Mode or power Save Mode for DCDC1 and DCDC2.

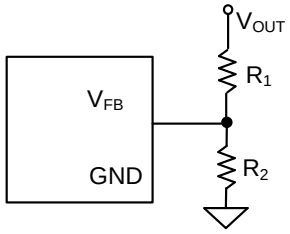
Connect this pin to VIN to enable forced PWM mode operation. And both converters operate in fixed frequency from open load to full load.

Connect this pin to GND to enable PFM mode operation at light load. The converters enter PWM mode automatically depending on the load condition.

Feedback resistor dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper DCDC1/DCDC2/LDO1/LDO2 output voltage. LDO3 is 1.5V fixed output. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 200kΩ is highly recommended for both resistors. If DCDC1 output voltage is 1.20V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 100k:

$$R_2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} R_1$$



V_{REF}=0.6V for DCDC1/DCDC2; V_{REF}=1.0V for LDO1/LDO2.

DCDC1/2 Input capacitor C_{IN}:

The DCDC channel ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} \cdot$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND

pins. In this case, a 10uF low ESR ceramic capacitor is recommended for each DCDC channel.
The minimum input capacitor on VIN_LDO1 is 1uF for LDO1 and 2.2uF for LDO2 and LDO3 on VIN_LDO2/3.

Output capacitor C_{OUT}:
The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 10uF capacitance for each DCDC channel.
LDO1, LDO2 and LOD3 is designed to be stable with an output capacitor of 2.2uF minimum.

Output inductor L:
There are several considerations in choosing this inductor.
1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

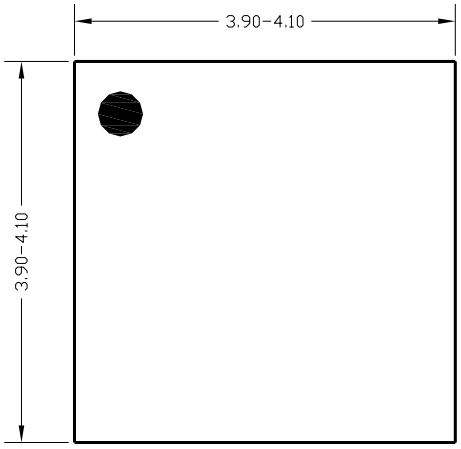
where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.
The SY8631B regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

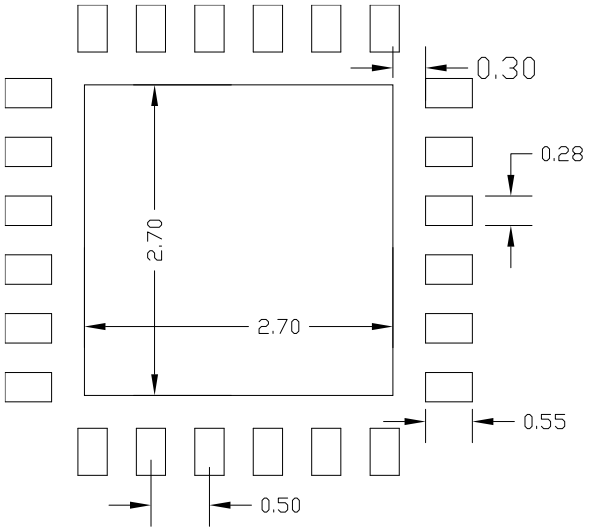
3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Load Transient Considerations:
The SY8631B DCDC1 and DCDC2 regulators integrate the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

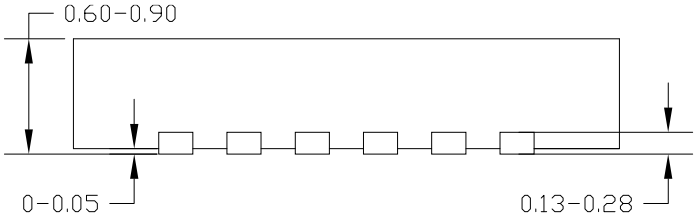
QFN4x4-24 Package Outline & PCB Layout



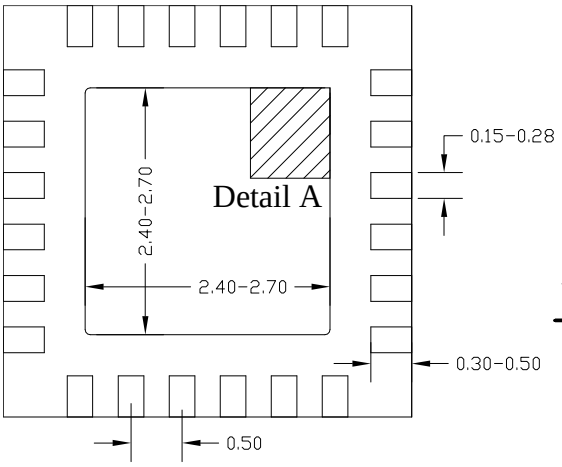
Top View

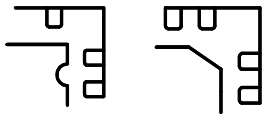


PCB layout (Recommended)



Side View





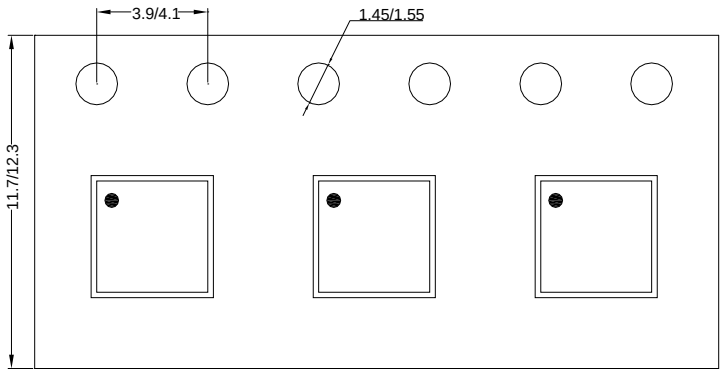
Detail A
Pin1 identifier: two options

Bottom View

Notes: **All dimension in MM and exclude mold flash & metal burr**

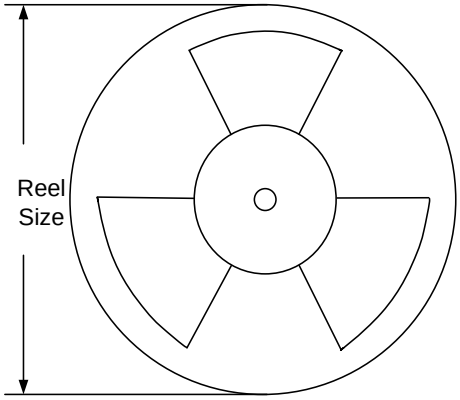
Taping & Reel Specification

1. QFN4x4 Taping Orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4x4	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages Changed
Nov.03, 2016	Revision 0.9	Initial risk production release.	-
Mar.07, 2025	Revision 1.0	Initial production release.	-

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