General Description

The SY21523x is a high efficiency PMIC with five-channel synchronous buck converters and two-channel LDOs. It is a single-chip total power solution for SSD systems.

The processor controls the output voltage of each channel using an I^2C interface, and it supports DVS (Dynamic Voltage Scaling) for each channel. The SY21523x can generate an open-drain reset output for the processor with a set delay time.

The SY21523x operates over a wide input voltage range from 2.8V to 5.5V. It is available in a CSP3.23x3.23-52 package.

Features

- 2.8V to 5.5V Input Voltage Range
- Channel 1 Synchronous Buck:
  - Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 150/150mΩ
  - 0.9A Maximum Output Current Capability
  - Default Output Voltage V_{OUT1} = 1.8V(SY21523C)
  - Default Output Voltage V_{OUT1} = 1.2V(SY21523E)
- Channel 2 LDO1:
  - 0.3A Output Current Capability
  - Default Output Voltage V_{OUT2} = 1.8V
- Channel 3 Synchronous Buck:
  - Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 45/20mΩ
  - 4.0A Maximum Output Current Capability
  - Default Output Voltage V_{OUT3} = 0.8V
  - 0.7V to 1.1V Programmable, 10mV Step
- Channel 4 Synchronous Buck:
  - Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 35/45mΩ
  - 4.0A Maximum Output Current Capability
  - Default Output Voltage V_{OUT4} = 2.625V
  - 2.3625V to 3.15V Programmable, 87.5mV Step
- Channel 5 Synchronous Buck:
  - Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 60/40mΩ
  - 2.0A Output Current Capability
  - Default Output Voltage V_{OUT5} = 1.2V/1.26V, Selected by Pin VSEL6
- Channel 6 LDO2:
  - 0.3A Output Current Capability
  - Default Output Voltage V_{OUT6} = 1.8V/2.5V, Selected by Pin VSEL7
- Channel 7 Synchronous Buck:
  - Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 60/40mΩ
  - 2.0A Output Current Capability
  - Default Output Voltage V_{OUT7} = 1.1V/1.2V, Selected by Pin VSEL7
- Reset Input/Output Function
- 2.0MHz Switching Frequency for Buck Converters
- Auto PWM/PFM Mode or Forced PWM Mode Controlled by I^2C Interface
- I^2C Interface up to 3.4MHz
- Output Voltage Level of CH3/CH4 Controlled by I^2C Interface with DVS Function
- Two Types of Power-On Reset Detection Voltage Level, Selected by PORSEL Pin
- Dedicated Sleep Mode Controlled by GPIO1/GPIO2, PMRST
- Reliable Protections:
  - Over Voltage Protection (OVP)
  - Over Current Protection (OCP)
  - Short Circuit Protection (SCP)
  - Over Temperature Protection (OTP)
- Compact Package: CSP3.23x3.23-52(0.4mm pitch)

Applications

- SSD Power

Typical Applications

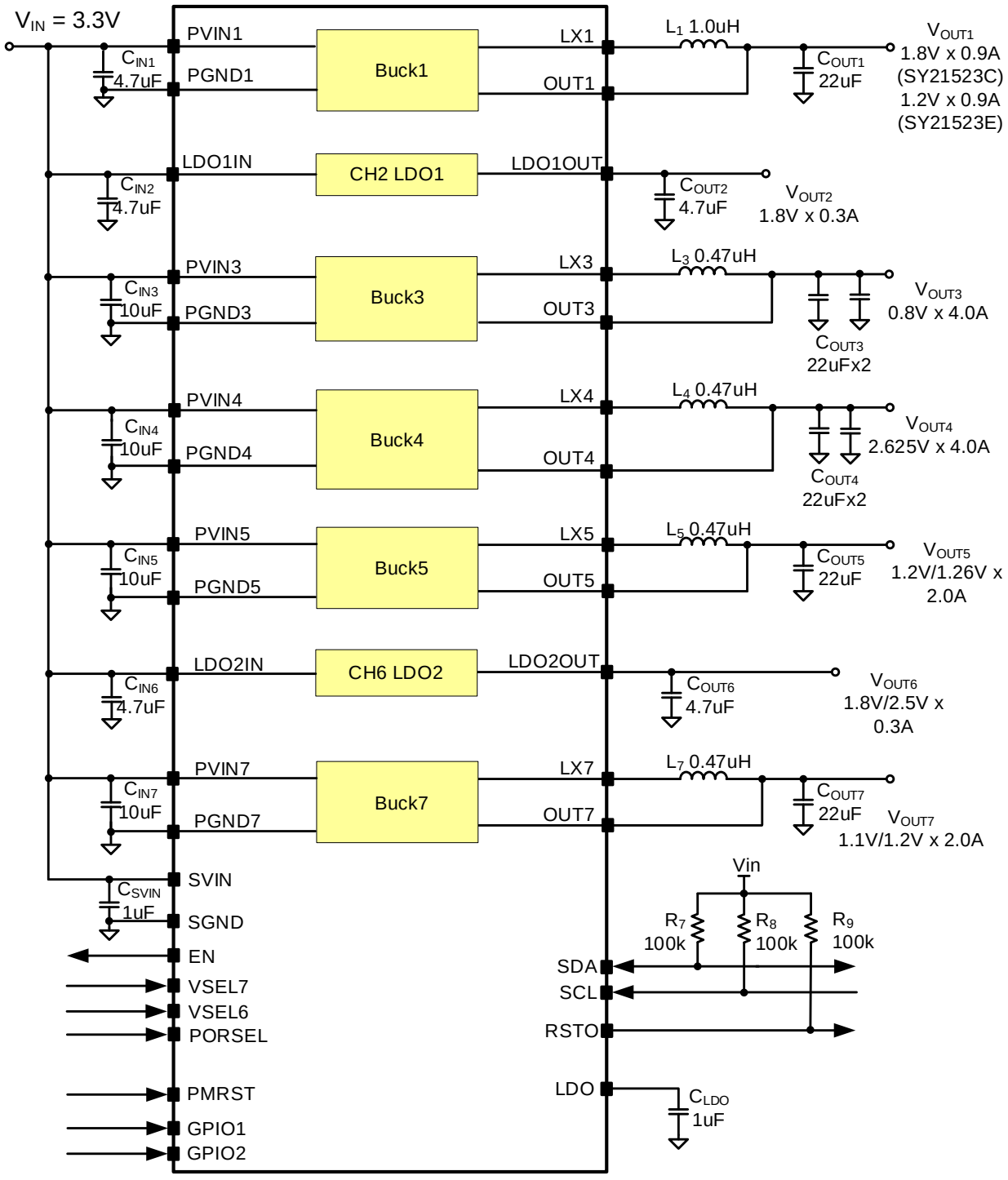


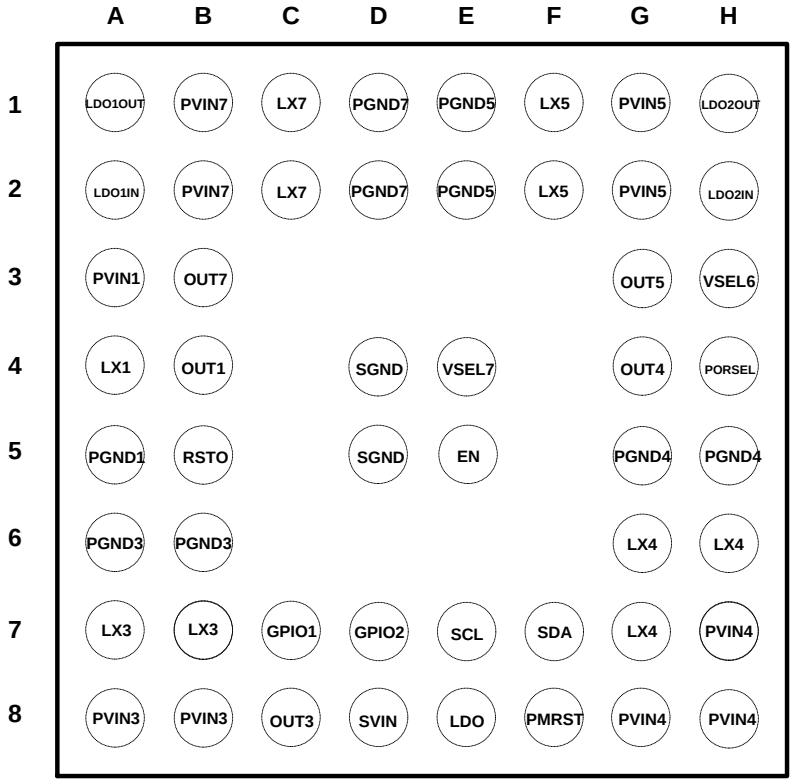
Figure 1. Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21523CPZC	CSP3.23x3.23-52 RoHS-Compliant and Halogen-Free	**DHF*xyz***
SY21523EPZC		**EDD*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



(CSP3.23x3.23-52)

Pin Description

Pin No	Pin Name	Pin Description
A1	LDO1OUT	CH2 LDO1 power output. Decouple this pin to GND with a 4.7μF MLCC capacitor.
A2	LDO1IN	CH2 LDO1 power input. Decouple this pin to GND with a 4.7μF MLCC capacitor.
A3	PVIN1	Power input for Buck 1. Decouple this pin to PGND1 with a 4.7μF MLCC capacitor.
A4	LX1	Switching node for Buck 1. Connect this pin to the switching node of an inductor.
A5	PGND1	Power ground for Buck 1.
B3	OUT7	Output feedback for Buck 7. Connect this pin to V_{OUT7} to regulate the output voltage.
B1,B2	PVIN7	Power input for Buck 7. Decouple this pin to PGND7 with a 10μF MLCC capacitor.
C1,C2	LX7	Switching node for Buck 7. Connect this pin to the switching node of an inductor.
D1,D2	PGND7	Power ground for Buck 7.
E1,E2	PGND5	Power ground for Buck 5.
F1,F2	LX5	Switching node for Buck 5. Connect this pin to the switching node of an inductor.
G1,G2	PVIN5	Power input for Buck 5. Decouple this pin to PGND5 with a 10μF MLCC capacitor.

Pin No	Pin Name	Pin Description
G3	OUT5	Feedback for Buck 5. Connect this pin to V_{OUT5} to regulate the output voltage.
H1	LDO2OUT	LDO2 power output pin. Decouple this pin to GND with a 4.7μF MLCC capacitor.
H2	LDO2IN	LDO2 power input pin. Decouple this pin to GND with a 4.7μF MLCC capacitor.
H3	VSEL6	Channel 5 (Buck 5) default output voltage selection pin.
H4	PORSEL	Leave this floating to select 3.3V input. It is pulled to GND internally.
E4	VSEL7	Channel 6 (LDO2), Channel 7 (Buck 7) default output voltage selection pin.
G4	OUT4	Feedback for Buck 4.Connect this pin to V_{OUT4} to regulate the output voltage.
G5,H5	PGND4	Power ground for Buck 4.
G6,G7,H6	LX4	Switching node for Buck 4. Connect this pin to the switching node of an inductor.
H7,G8,H8	PVIN4	Power input for Buck 4. Decouple this pin to PGND4 with a 10μF MLCC capacitor.
F7	SDA	Data line for the I^2C interface. Open drain.
E7	SCL	Clock input for the I^2C interface. Open-drain input.
E8	LDO	Internal LDO output. Decouple this pin to PGND with 1μF MLCC capacitor.
F8	PMRST	PMIC reset input. All channels will return to their previous value when the PMRST falling edge is detected. An internal 2MΩ resistor will pull this pin low when it is not used.
D4,D5	SGND	Signal power ground.
E5	EN	Enable output to enable/disable external DC/DC.
C7	GPIO1	Sleep mode control pin1.
D7	GPIO2	Sleep mode control pin2.
D8	SVIN	Signal power supply input. Decouple this pin to GND with at least a 1μF MLCC capacitor.
C8	OUT3	Output feedback pin for Buck 3. Connect this pin to V_{OUT3} to regulate the output voltage.
A8,B8	PVIN3	Power input for Buck 3. Decouple this pin to PGND3 with a 10μF MLCC capacitor.
A7,B7	LX3	Switching node for Buck 3. Connect this pin to the switching node of an inductor.
A6,B6	PGND3	Power ground for Buck 3.
B5	RSTO	Reset output.
B4	OUT1	Output feedback for Buck 1.Connect this pin to V_{OUT1} to regulate the output voltage.

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
All Pins	-0.3	6	V
Junction Temperature Range		150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature Range	-55	150	
ESD Susceptibility			
HBM (Human Body Model)	2000		V
CDM (Charged Device Model)	500		
Latch-up	200		mA

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	24	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	1	
P_D Power Dissipation T_J = 25°C	5	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Supply Input Voltage	2.8	5.5	V
Junction Temperature Range	-40	125	°C
Ambient Temperature Range	-40	85	

Block Diagram

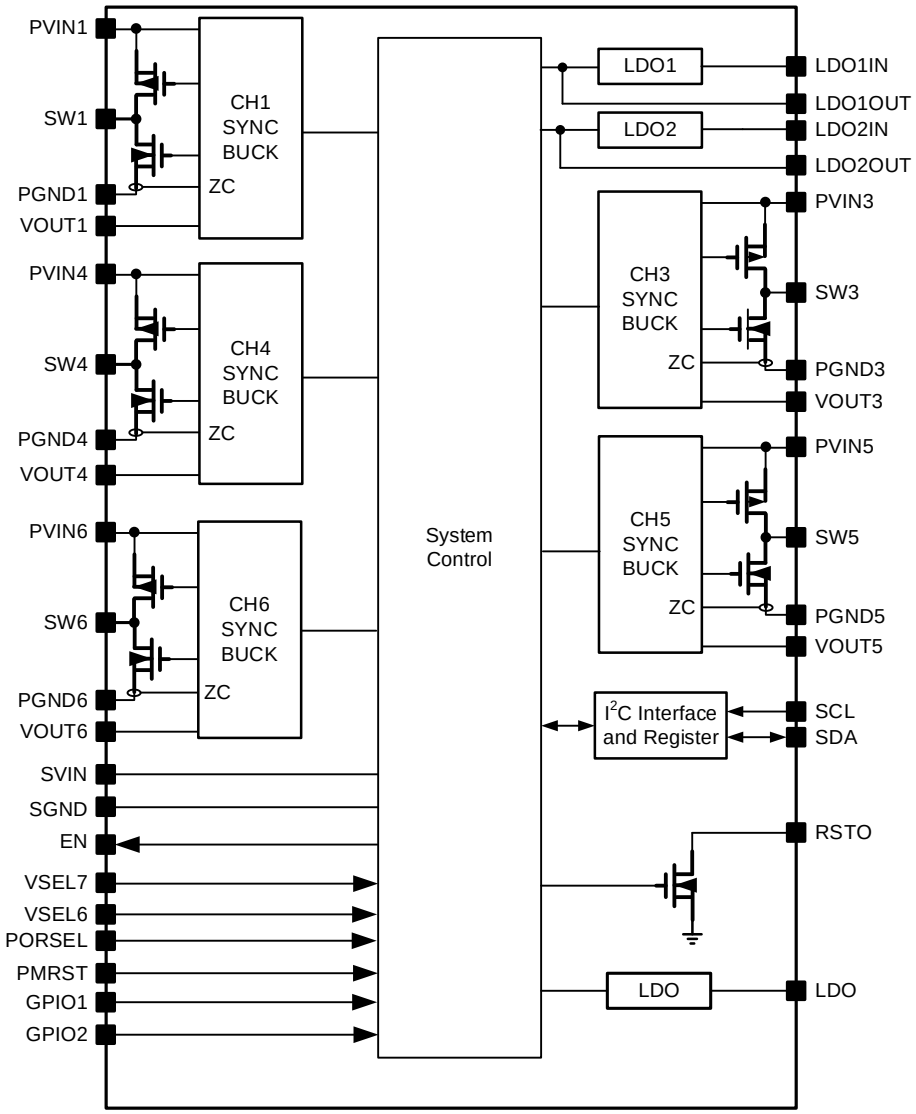


Figure 2. Block Diagram

Electrical Characteristics

(V_{IN} = 3.3V, T_J = 25°C, unless otherwise specified. (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Input Voltage Range	V_{IN}		2.6		5.5	V
	Input Voltage UVLO Threshold	$V_{UVLO,FALLING}$	PORSEL = 0 V_{IN} falling	2.561	2.6	2.639	V
	Input Voltage UVLO Hysteresis	$V_{UVLO,HYS}$	Hysteresis (Note 5)		100		mV
	POR Threshold	$V_{POR,FALLING}$	PORSEL = 0 V_{IN} falling	2.561	2.6	2.639	V
	POR Hysteresis	$V_{POR,HYS}$	Hysteresis (Note 5)		100		mV
	System Delay Time from UVLO	T_{SYS}	(Note 5)		1		ms
	Quiescent Current	I_Q	No load input current, V_{IN} = 3.3V			180	μA
VSEL6, VSEL7, PMRST, GPIO1, GPIO2	Logic Level High	V_{HIGH}		1.2			V
	Logic Level Low	V_{LOW}				0.4	V
EN	Output High Voltage	V_{OH}	R_{EN} = 100k to GND	0.8x		V_{IN}	V
	Output Low Voltage	V_{OL}	R_{EN} = 100k to GND			0.2 x V_{IN}	V
	EN Turn High Delay Time from V_{IN}	T_{EN}	After system delay time (Note 5)		2		ms
Power-On Reset (POR)	POR Deglitch Delay		V_{IN} Falling(Note 5)		2		μs
	RSTO Output Low Resistance		(Note 5)		10		Ω
	RSTO Delay time from UVLO Threshold	$T_{POR,DEL}$	V_{IN} = 3.3V	10.8	12	13.2	ms
I^2C COMPATIBLE I/O (SDA, SCL)	Maximum Operating Frequency	f_{SCL}				3.4	MHz
	I^2C Supply Voltage				1.8	5.5	V
	SDA and SCL Pin Input Logic Thresholds	Logic low				0.5	V
		Logic high		1.2			V
Channel 1 Synchronous Buck Converter	Output Voltage Default Value	$V_{OUT1,DEF}$	SY21523C (Note 5)		1.8		V
			SY21523E (Note 5)		1.2		
	Output Voltage Accuracy, PWM	ΔV_{OUT1}	PWM mode operation, T_J = 25°C	-1		+1	%
			PWM mode operation, T_J = -40°C–125°C	-2		+2	
	Output Voltage Accuracy, PFM	ΔV_{OUT1}	I_{OUT} = 1mA, average ripple voltage T_J = -40°C–125°C	-2.5		+2.5	%
	Switching Frequency	F_{OSC1}	(Note 5)		2.0		MHz
	Main PFET R_{ON}	$R_{DS(ON),P1}$	(Note 5)		150		mΩ
	Synchronous NFET R_{ON}	$R_{DS(ON),N1}$	(Note 5)		150		mΩ
	High Side FET Current Limit	I_{LIM1_HS}		1.6			A
	Maximum Output DC Load Current	I_{OUT1}		0.9			A
	Internal Soft-Start Time	t_{SS1}	V_{OUT} rising from 10% to 90% (Note 5)		200		μs
	Startup Default Delay Time	t_{DELAY1}	After system delay (Note 5)		2		ms

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
	Discharge Resistor	R_{DIS1}	(Note 5)			10		Ω
	SCP Threshold	V_{SCP1}	V_{SCP1} < V_{OUT1} x 30% (Note 5)			30		%
	SCP Deglitch Time	t_{SCP1}	(Note 5)			10		μs
Channel 2 LDO	Output Voltage Default Value	$V_{LDO1OUT}$	(Note 5)			1.8		V
	Output Voltage Accuracy	V_{OUT2}	I_{OUT2} = 10mA	T_J = 25°C	-1		+1	%
				T_J = -40°C–125°C	-2		+2	
	Current Limit	I_{LIM2}			0.3			A
	Maximum Output DC Load Current	I_{OUT2}			0.3			A
	Dropout Voltage		I_{OUT2} = 0.3A				300	mV
	Internal Soft-Start Time	t_{SS2}	V_{OUT} rising from 10% to 90% (Note 5)			200		us
	Startup Default Delay Time	T_{DELAY2}	After system delay (Note 5)			2.0		ms
	Discharge Resistor	R_{DIS2}	(Note 5)			10		Ω
	SCP Threshold	V_{SCP2}	V_{SCP2} < V_{OUT2} x 60% (Note 5)			60		%
	SCP Deglitch Time	t_{SCP2}	(Note 5)			100		μs
Channel 3 Synchronous Buck Converter	Output Voltage Default Value	$V_{OUT3,DEF}$	(Note 5)			0.8		V
	DVS Voltage Step	$V_{OUT3,DVS,STEP}$	Controllable by I^2C interface (Note 5)			10		mV
	DVS Voltage Range	$V_{OUT3,DVS}$	Controllable by I^2C interface		0.7		1.1	mV
	Output Voltage Accuracy, PWM	ΔV_{OUT3}	PWM mode operation	T_J = 25°C	-1		+1	%
				T_J = -40°C–125°C	-2		+2	
	Output Voltage Accuracy, PFM	ΔV_{OUT3}	I_{OUT} = 1mA, average ripple voltage T_J = -40°C–125°C		-2.5		+2.5	%
	Switching Frequency	f_{OSC3}	(Note 5)			2.0		MHz
	Main PFET R_{ON}	$R_{DS(ON),P3}$	(Note 5)			45		mΩ
	Synchronous NFET R_{ON}	$R_{DS(ON),N3}$	(Note 5)			20		mΩ
	High Side FET Current Limit	I_{LIM3_HS}			5.0			A
	Maximum Output DC Load Current	I_{OUT3}			4.0			A
	Internal Soft-Start Time	t_{SS3}	V_{OUT} rising from 10% to 90% (Note 5)			200		μs
	Startup Default Delay Time	t_{DELAY3}	After system delay (Note 5)			0		ms
	Discharge Resistor	R_{DIS3}	(Note 5)			10		Ω
	SCP Threshold	V_{SCP3}	V_{SCP3} < V_{OUT3} x 30% (Note 5)			30		%
	SCP Deglitch Time	t_{SCP3}	(Note 5)			10		μs
Channel 4 Synchronous Buck Converter	Output Voltage Default Value	$V_{OUT4,DEF}$	(Note 5)			2.625		V
	DVS Voltage Step	$V_{OUT4,DVS,STEP}$	Controllable by I^2C interface (Note 5)			87.5		mV
	DVS Voltage Range	$V_{OUT4,DVS}$	Controllable by I^2C interface		2.3625		3.15	V
	Output Voltage Accuracy, PWM	ΔV_{OUT4}	PWM mode operation	T_J = 25°C	-1		+1	%
				T_J = -40°C–125°C	-2		+2	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Output Voltage Accuracy, PFM	ΔV_{OUT4}	I_{OUT} = 1mA, average ripple voltage T_J = -40°C–125°C	-2.5		+2.5	%
	Switching Frequency	f_{OSC4}	(Note 5)		2.0		MHz
	Main PFET R_{ON}	$R_{DS(ON),P4}$	(Note 5)		35		mΩ
	Synchronous NFET R_{ON}	$R_{DS(ON),N4}$	(Note 5)		45		mΩ
	High Side FET Current Limit	I_{LIM4_HS}		5.0			A
	Maximum Output DC Load Current	I_{OUT4}		4.0			A
	Internal Soft-Start Time	t_{SS4}	V_{OUT} rising from 10% to 90% (Note 5)		200		µs
	Startup Default Delay Time	t_{DELAY4}	(Note 5)		7		ms
	Discharge Resistor	R_{DIS4}	(Note 5)		10		Ω
	SCP Threshold	V_{SCP4}	V_{SCP4} < V_{OUT4} x 30% (Note 5)		30		%
	SCP Deglitch Time	t_{SCP4}	(Note 5)		10		µs
Channel 5 Synchronous Buck Converter	Output Voltage Default Value	$V_{OUT5,DEF}$	VSLEL6 = 0 (Note 5)		1.2		V
			VSLEL6 = 1 (Note 5)		1.26		
	Output Voltage Accuracy, PWM	ΔV_{OUT5}	PWM mode operation, T_J = 25°C	-1		+1	%
			PWM mode operation, T_J = -40°C–125°C	-2		+2	
	Output voltage Accuracy, PFM	ΔV_{OUT5}	I_{OUT} = 1mA, average ripple voltage T_J = -40°C–125°C	-2.5		+2.5	%
	Switching Frequency	f_{OSC5}	(Note 5)		2.0		MHz
	Main PFET R_{ON}	$R_{DS(ON),P5}$	(Note 5)		60		mΩ
	Synchronous NFET R_{ON}	$R_{DS(ON),N5}$	(Note 5)		40		mΩ
	High Side FET Current Limit	I_{LIM5_HS}		3.0			A
	Maximum Output DC Load Current	I_{OUT5}		2.0			A
	Internal Soft-Start Time	t_{SS5}	V_{OUT} rising from 10% to 90% (Note 5)		200		µs
	Startup Default Delay Time	t_{DELAY5}	After system delay (Note 5)		9		ms
	Discharge Resistor	R_{DIS5}	(Note 5)		10		Ω
	SCP Threshold	V_{SCP5}	V_{SCP5} < V_{OUT5} x 30% (Note 5)		30		%
	SCP Deglitch Time	t_{SCP5}	(Note 5)		10		µs
Channel 6 LDO	Output Voltage Default Value	$V_{OUT6,DEF}$	VSEL7 = 0 (Note 5)		1.8		V
			VSEL7 = 1 (Note 5)		2.5		V
	Output Voltage Accuracy	V_{OUT6}	I_{OUT6} = 10mA, T_J = 25°C	-1		+1	%
			I_{OUT6} = 10mA, T_J = -40°C–125°C	-2		+2	
	Current Limit	I_{LIM6}		0.3			A
	Maximum Output DC Load Current	I_{OUT6}		0.3			A
	Dropout Voltage		I_{OUT6} = 0.3A			300	mV
	Internal Soft-Start Time	t_{SS6}	V_{OUT} rising from 10% to 90% (Note 5)		200		µs

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Startup Default Delay Time	t_{DELAY6}	After system delay (Note 5)		2		ms
	Discharge Resistor	R_{DIS6}	(Note 5)		10		Ω
	SCP Threshold	V_{SCP6}	V_{SCP6} < V_{OUT6} x 60% (Note 5)		60		%
	SCP Deglitch Time	t_{SCP6}	(Note 5)		100		µs
Channel 7 Synchronous Buck Converter	Output Voltage Default Value	$V_{OUT7,DEF}$	VSEL7 = 0 (Note 5)		1.1		V
			VSEL7 = 1 (Note 5)		1.2		
	Output Voltage Accuracy, PWM	ΔV_{OUT7}	PWM mode operation, T_J = 25°C	-1		+1	%
			PWM mode operation, T_J = -40°–125°C	-2		+2	
	Output Voltage Accuracy, PFM	ΔV_{OUT7}	I_{OUT} = 1mA, average ripple voltage T_J = -40°C–125°C	-2.5		+2.5	%
	Switching Frequency	f_{OSC7}	(Note 5)		2.0		MHz
	Main PFET R_{ON}	$R_{DS(ON),P7}$	(Note 5)		60		mΩ
	Synchronous NFET R_{ON}	$R_{DS(ON),N7}$	(Note 5)		40		mΩ
	High Side FET Current Limit	I_{LIM7_HS}		3.0			A
	Maximum Output DC Load Current	I_{OUT7}		2.0			A
	Internal Soft-Start Time	t_{SS7}	V_{OUT} rising from 10% to 90% (Note 5)		200		µs
	Startup Default Delay Time	t_{DELAY7}	After system delay (Note 5)		5		ms
	Discharge Resistor	R_{DIS7}	(Note 5)		10		Ω
	SCP Threshold	V_{SCP7}	V_{SCP7} < V_{OUT7} x 30% (Note 5)		30		%
	SCP Deglitch Time	t_{SCP7}	(Note 5)		10		µs
Protection	Thermal Shutdown Threshold	t_{SD}	(Note 5)		155		°C
	Thermal Shutdown Hysteresis	t_{HYS}	(Note 5)		20		°C
	External VIN OVP Protection Threshold	VIN_{OVP}	V_{IN} rising	3.7	3.85	4.0	V
	Input OVP Hysteresis	VIN_{OVP_HYS}	V_{IN} falling (Note 5)		0.15		V
	External V_{IN} OVP Deglitch Time		(Note 5)		5		µs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

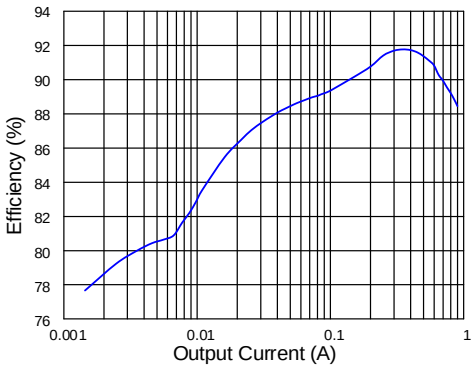
Note 5: Guaranteed by design or statistical correlation and not production tested.

Typical Performance Characteristics

(T_A = 25°C, unless otherwise noted)

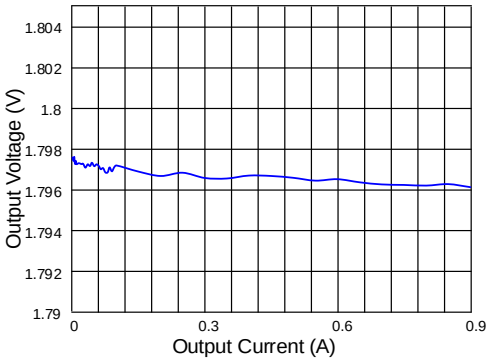
Buck1 Efficiency vs. Output Current

(V_{IN}=3.3V, V_{OUT}=1.8V, L=1μH/ MLP2520S1R0M, C_{OUT}=22μF)



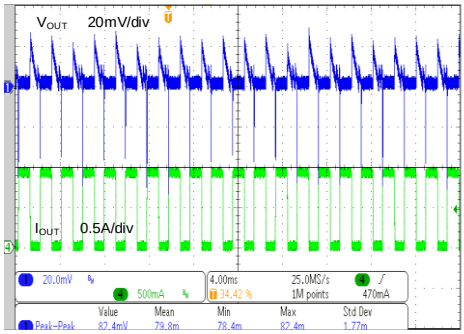
Buck1 Load Regulation

(V_{IN}=3.3V, V_{OUT}=1.8V, L=1μH/ MLP2520S1R0M, C_{OUT}=22μF)



Buck1 Load Transient

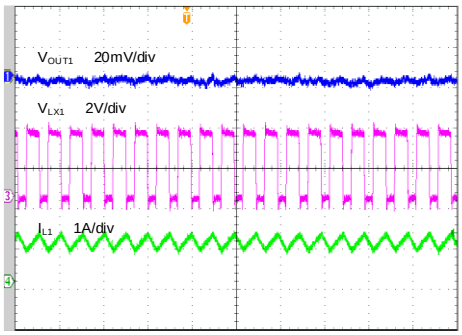
(V_{IN}=3.3V, V_{OUT}=1.8V, L=1μH, C_{OUT}=22μF, I_{OUT}=0~0.9A(10μs))



Time(4ms/div)

Buck1 Waveforms, FCCM Mode

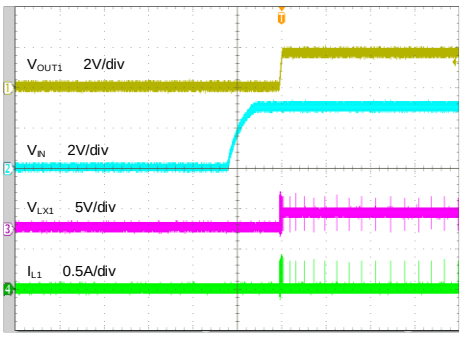
(V_{IN}=3.3V, V_{OUT}=1.8V, L=1μH, C_{OUT}=22μF, I_{OUT}=0.9A)



Time(1μs/div)

Buck1 Power On

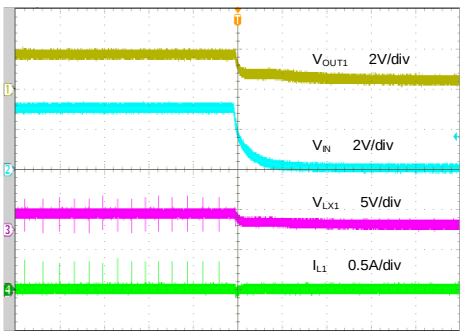
(V_{IN}=3.3V, V_{OUT}=1.8V, L=1μH, C_{OUT}=22μF, I_{OUT}=0A)



Time(4ms/div)

Buck1 Power Off

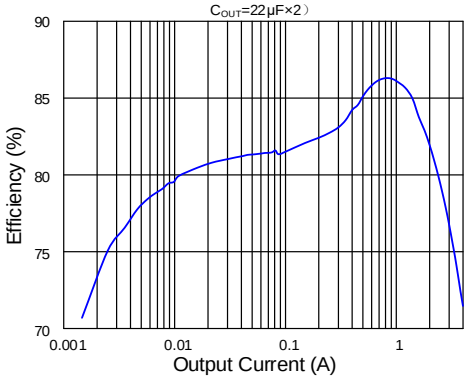
(V_{IN}=3.3V, V_{OUT}=1.8V, L=1μH, C_{OUT}=22μF, I_{OUT}=0A)



Time(4ms/div)

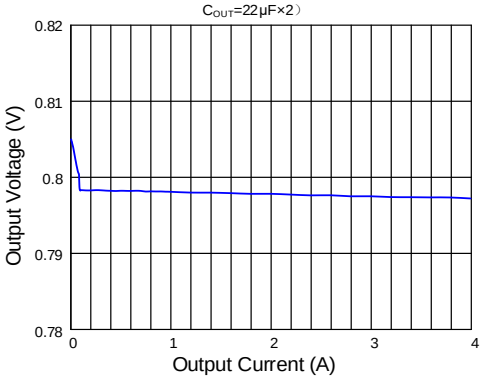
Buck3 Efficiency vs. Output Current

（V_{IN}=3.3V, V_{OUT}=0.8V, L=0.47μH/ WPN252010UFR47MT, C_{OUT}=22μF×2）



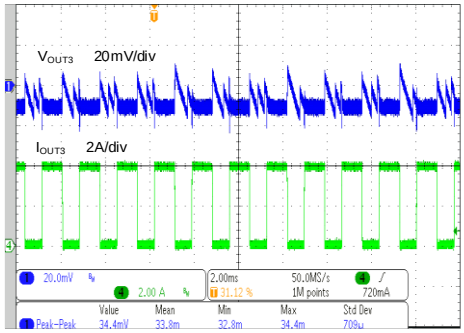
Buck3 Load Regulation

（V_{IN}=3.3V, V_{OUT}=0.8V, L=0.47μH/ WPN252010UFR47MT, C_{OUT}=22μF×2）



Buck3 Load Transient

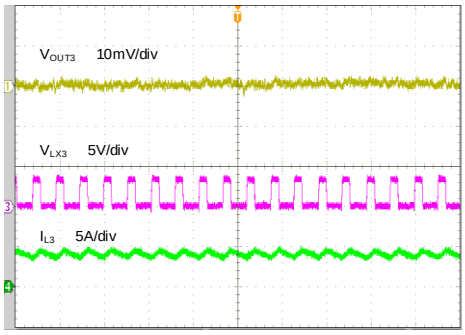
(V_{IN}=3.3V, V_{OUT}=0.8V, L=0.47μH, C_{OUT}=22μF×2，I_{OUT}=0~4A(10μs))



Time(2ms/div)

Buck3 Waveforms, FCCM Mode

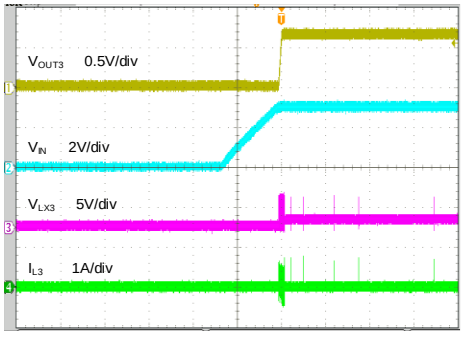
（V_{IN}=3.3V, V_{OUT}=0.8V, L=0.47μH, C_{OUT}=22μF×2，I_{OUT}=4A）



Time(1μs/div)

Buck3 Power On

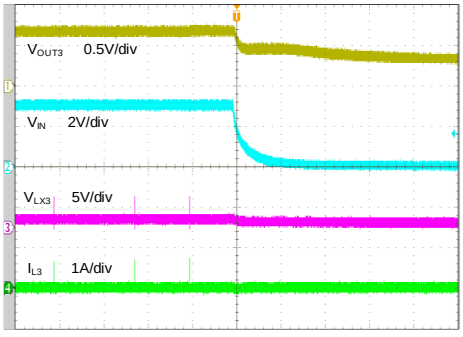
（V_{IN}=3.3V, V_{OUT}=0.8V, L=0.47μH, C_{OUT}=22μF×2，I_{OUT}=0A）



Time(4ms/div)

Buck3 Power Off

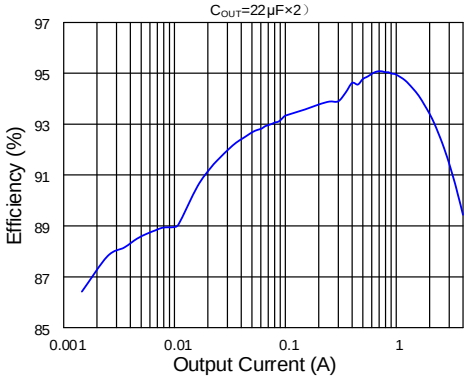
（V_{IN}=3.3V, V_{OUT}=0.8V, L=0.47μH, C_{OUT}=22μF×2，I_{OUT}=0A）



Time(4ms/div)

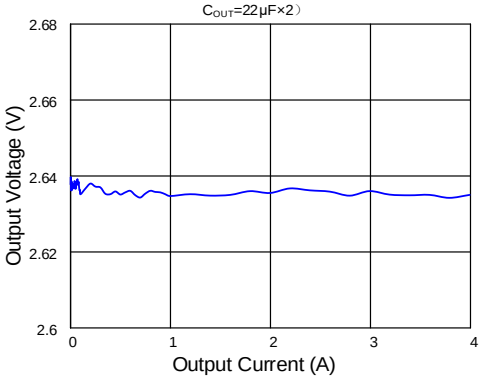
Buck4 Efficiency vs. Output Current

（V_{IN}=3.3V, V_{OUT}=2.625V, L=0.47μH/ WPN252010UFR47MT, C_{OUT}=22μF×2）



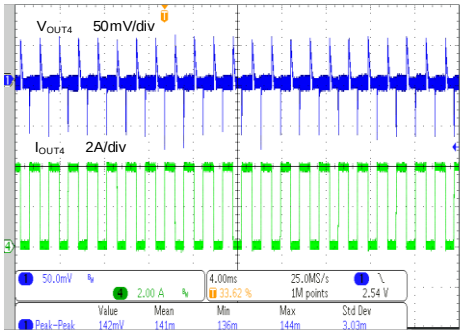
Buck4 Load Regulation

（V_{IN}=3.3V, V_{OUT}=2.625V, L=0.47μH/ WPN252010UFR47MT, C_{OUT}=22μF×2）



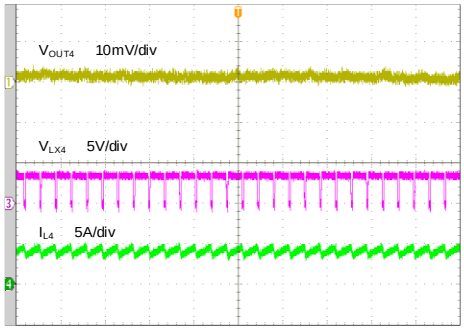
Buck4 Load Transient

(V_{IN}=3.3V, V_{OUT}=2.625V, L=0.47μH, C_{OUT}=22μF×2, I_{OUT}=0~4A(10μs))



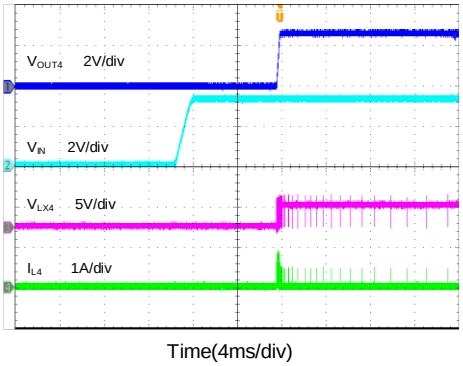
Buck4 Waveforms, FCCM Mode

（V_{IN}=3.3V, V_{OUT}=2.625V, L=0.47μH, C_{OUT}=22μF×2，I_{OUT}=4A）



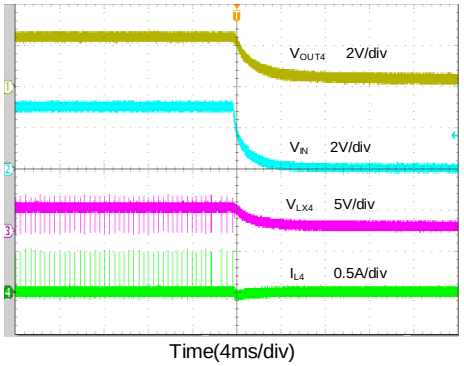
Buck4 Power On

（V_{IN}=3.3V, V_{OUT}=2.625V, L=0.47μH, C_{OUT}=22μF×2，I_{OUT}=0A）



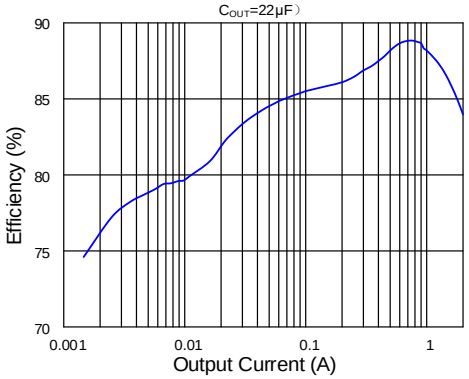
Buck4 Power Off

（V_{IN}=3.3V, V_{OUT}=2.625V, L=0.47μH, C_{OUT}=22μF×2，I_{OUT}=0A）



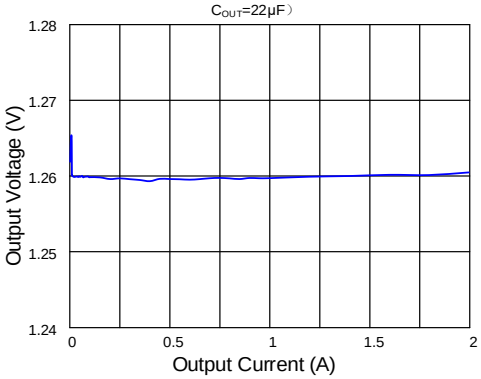
Buck5 Efficiency vs. Output Current

（V_{IN}=3.3V, V_{OUT}=1.26V, L=0.47μH/ WPN252010UFR47MT, C_{OUT}=22μF）



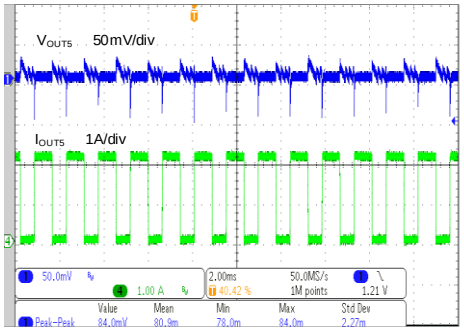
Buck5 Load Regulation

（V_{IN}=3.3V, V_{OUT}=1.26V, L=0.47μH/ WPN252010UFR47MT, C_{OUT}=22μF）



Buck5 Load Transient

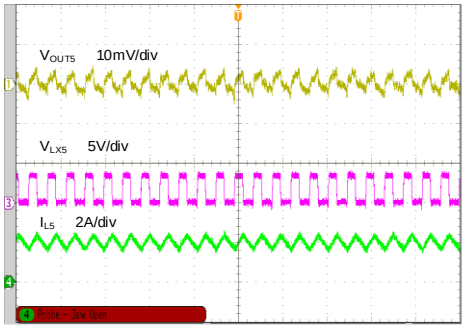
(V_{IN}=3.3V, V_{OUT}=1.26V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~2A(10μs))



Time(2ms/div)

Buck5 Waveforms, FCCM Mode

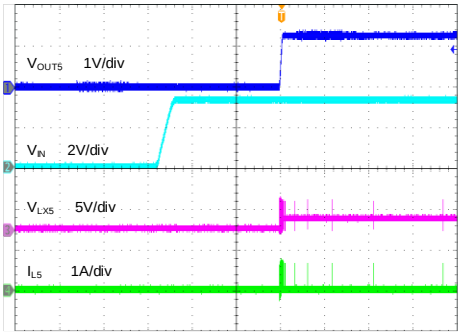
(V_{IN}=3.3V, V_{OUT}=1.26V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=2A)



Time(1μs/div)

Buck5 Power On

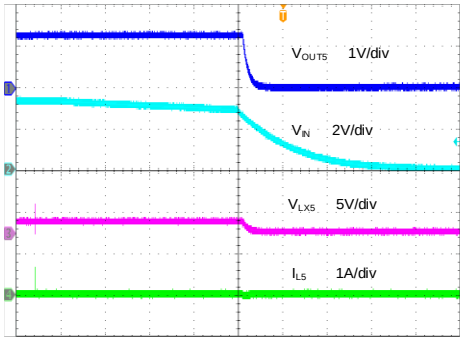
（V_{IN}=3.3V, V_{OUT}=1.26V, L=0.47μH, C_{OUT}=22μF， I_{OUT}=0A）



Time(4ms/div)

Buck5 Power Off

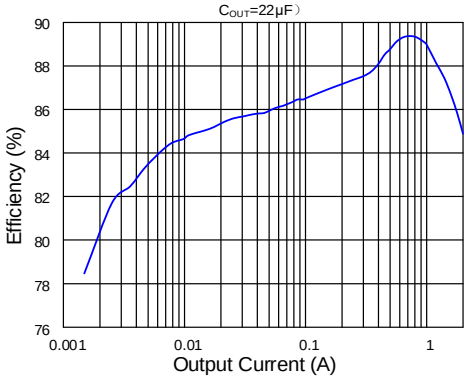
（V_{IN}=3.3V, V_{OUT}=1.26V, L=0.47μH, C_{OUT}=22μF， I_{OUT}=0A）



Time(4ms/div)

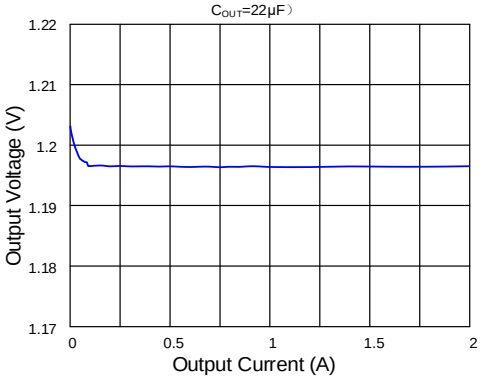
Buck7 Efficiency vs. Output Current

（V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH/ WPN252010UFR47MT, C_{OUT}=22μF）



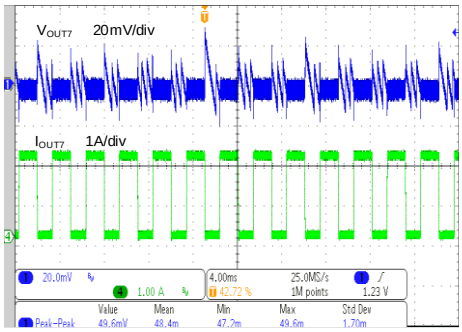
Buck7 Load Regulation

（V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH/ WPN252010UFR47MT, C_{OUT}=22μF）



Buck7 Load Transient

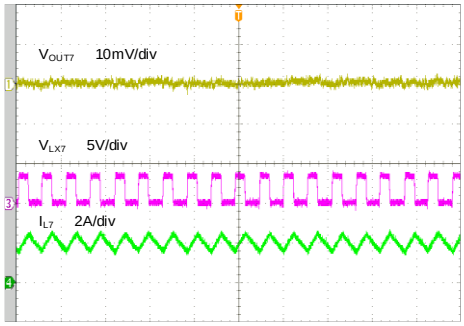
(V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~2A(10μs))



Time(4ms/div)

Buck7 Waveforms, FCCM Mode

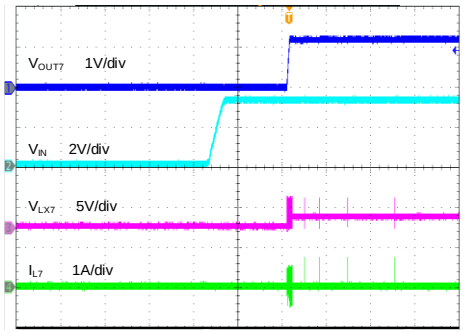
(V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=2A)



Time(1μs/div)

Buck7 Power On

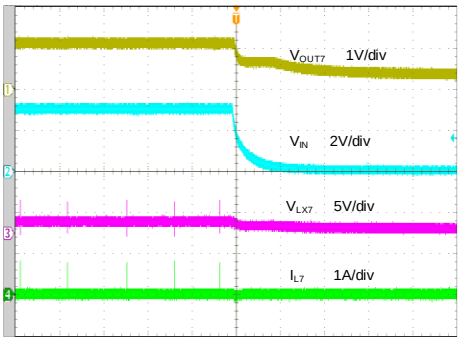
（V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A）



Time(4ms/div)

Buck7 Power Off

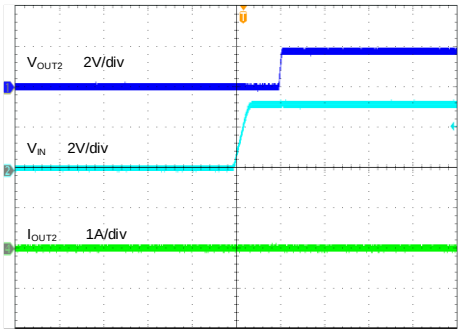
（V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A）



Time(4ms/div)

LDO1 Power On

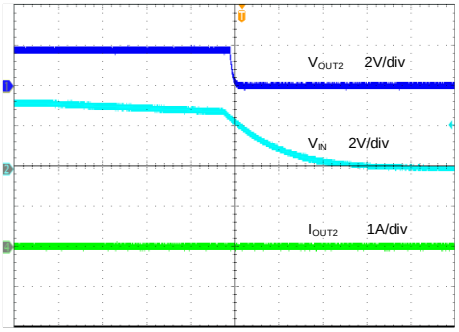
（V_{IN}=3.3V, V_{OUT}=1.8V, C_{OUT}=4.7μF，I_{OUT}=0A）



Time(4ms/div)

LDO1 Power Off

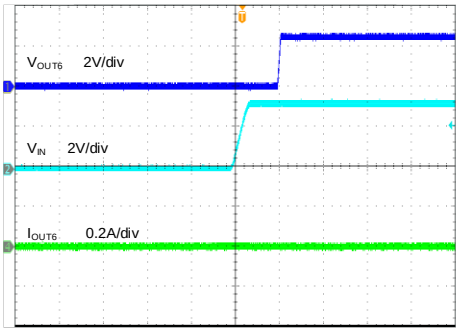
（V_{IN}=3.3V, V_{OUT}=1.8V, C_{OUT}=4.7μF，I_{OUT}=0A）



Time(4ms/div)

LDO2 Power On

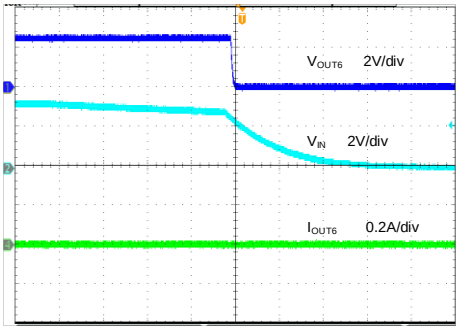
（V_{IN}=3.3V, V_{OUT}=2.5V, C_{OUT}=4.7μF，I_{OUT}=0A）



Time(4ms/div)

LDO2 Power Off

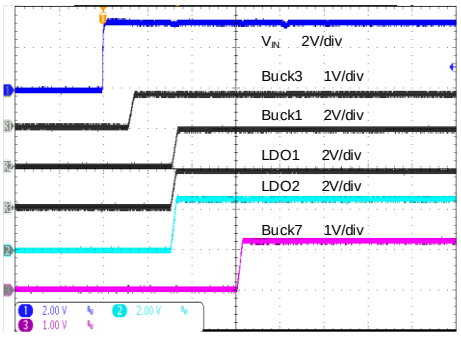
（V_{IN}=3.3V, V_{OUT}=2.5V, C_{OUT}=4.7μF，I_{OUT}=0A）



Time(4ms/div)

Power On Sequence

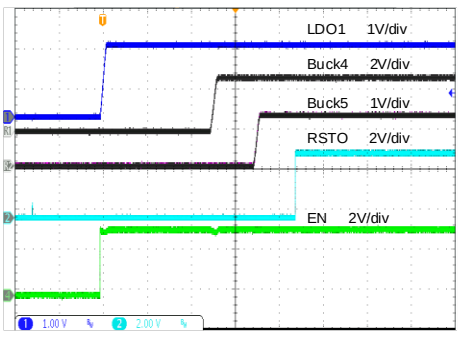
(V_{IN}=3.3V,GPIO1=1,GPIO2=1)



Time(2ms/div)

Power On Sequence

(V_{IN}=3.3V,GPIO1=1,GPIO2=1)



Time(2ms/div)

Functional Description

Table 1. Targeted Output Voltage

Channel	Topology	Default Output Voltage (V)	Output Voltage Range (V)	DVS Step (mV)	$R_{DS(ON)}$ (mΩ)		IOUT MAX (A)	Power On Delay Time (ms)	SS Time (μs)
					High Side	Low Side			
CH1	Buck	1.8(SY21523C) 1.2(SY21523E)	-	-	150	150	0.9	2	200
CH2	LDO	1.8	-	-	-	-	0.3	2	200
CH3	Buck	0.8	0.7-1.1	10	45	20	4	0	200
CH4	Buck	2.625	2.3625-3.15	87.5	35	45	4	7	200
CH5	Buck	VSEL6 = 0, V_{OUT5} = 1.2 VSEL6 = 1, V_{OUT5} = 1.26	1.2/1.26	-	60	40	2	9	200
CH6	LDO	VSEL7 = 0, V_{OUT6} = 1.8 VSEL7 = 1, V_{OUT6} = 2.5	1.8/2.5	-	-	-	0.3	2	200
CH7	Buck	VSEL7 = 0, V_{OUT7} = 1.1 VSEL7 = 1, V_{OUT7} = 1.2	1.1/1.2	-	60	40	2	5	200
RSTO	-	-	-	-	-	-	-	12	-
EN	-	-	-	-	-	-	-	2	-

POR Threshold and RSTO Delay

The default power-on reset (POR) threshold is 2.6V for a 3.3V input application. When V_{IN} exceeds the threshold voltage, RSTO will provide a high-level output signal after a fixed 12ms delay time $T_{POR,DEL}$, as shown in Figure 3.

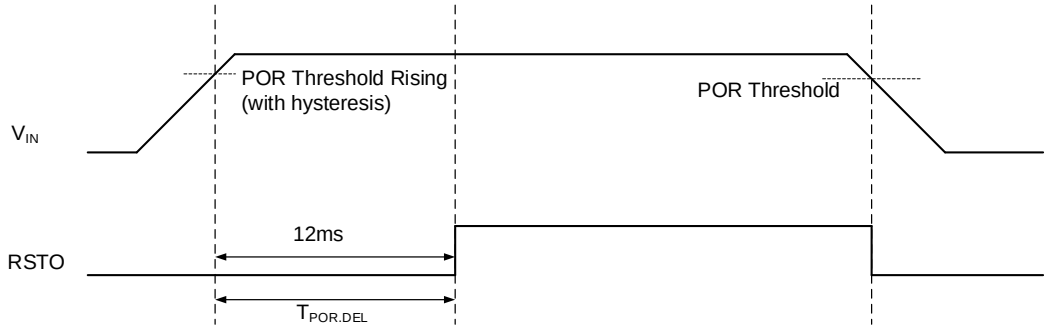


Figure 3. POR Threshold and RSTO Delay

V_{IN} Power-On Sequence

When input voltage V_{IN} exceeds the input UVLO rising threshold, each channel will power on after a 1ms system delay t_{SYS} plus a channel-specific fixed delay t_{DELn}. When V_{IN} exceeds input UVLO threshold, RSTO will provide a high-level output signal after a fixed delay time $t_{DEL,RSTO}$ = 12ms. See Figure 4.

Sleep Mode

To reduce power consumption, the SY21523x can enter sleep mode and turn channels off individually, or adjust CH3/CH4 output voltages. The EN pin is synchronized with the CH2 LDO1 internal EN signal, so the external converter will be turned on or off along with the CH2 LDO1. When the PMRST falling edge is detected, all channels revert to their previous values (prior to sleep mode) at the same time. See Figure 4.

V_{IN} Power-Off Sequence

When the external V_{IN} is lower than the UVLO falling threshold, all channels will be turned off immediately. The discharge resistor is turned on during the power-off sequence if the corresponding discharge register bit ENDIS_CHn is set to 1. See Figure 4.

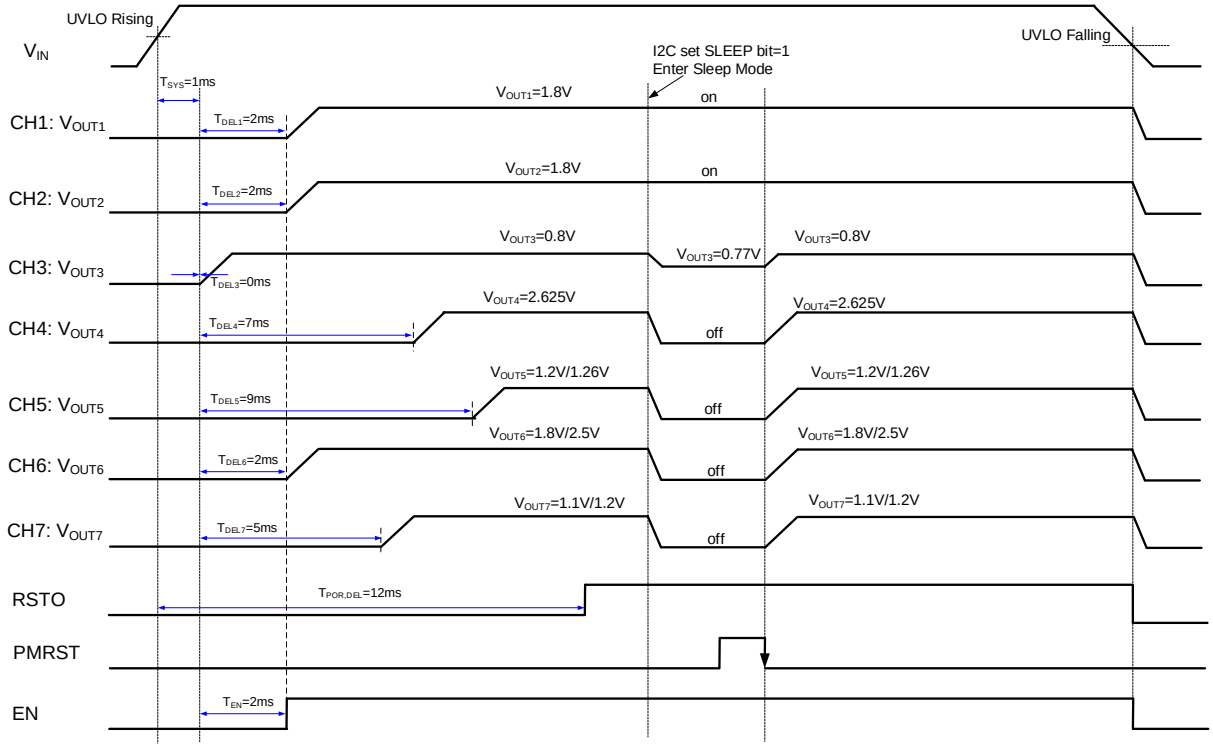


Figure 4. V_{IN} Power-On/Off Sequence

Sleep Mode Controlled by GPIO1/GPIO2

GPIO1 and GPIO2 can be used to make the PMIC enter sleep mode as shown in Table 2. GPIO1 and GPIO2 are active when RSTO is logic level high.

Table 2. GPIO1/GPIO2 Sleep Mode Control

Mode	GPIO1	GPIO2	Channel On/Off State
Active Mode	1	-	On/Off controlled by I^2C
Low Power Mode 1 (PS3.5)	0	1	CH4/CH5 off, other channels on, CH3: set to 0.8V.
Low Power Mode 2 (PS4.0)	0	0	CH4/CH5/CH6/CH7 off, other channels on, CH3: 0.8V→0.77V

Low Power Mode 1 (PS3.5)

When GPIO2 maintains high logic level and GPIO1 is pulled low, the PMIC enters Low Power Mode 1 (PS3.5), CH4/CH5 are turned off, and CH3 output voltage remains at 0.8V as shown in Figure 5.

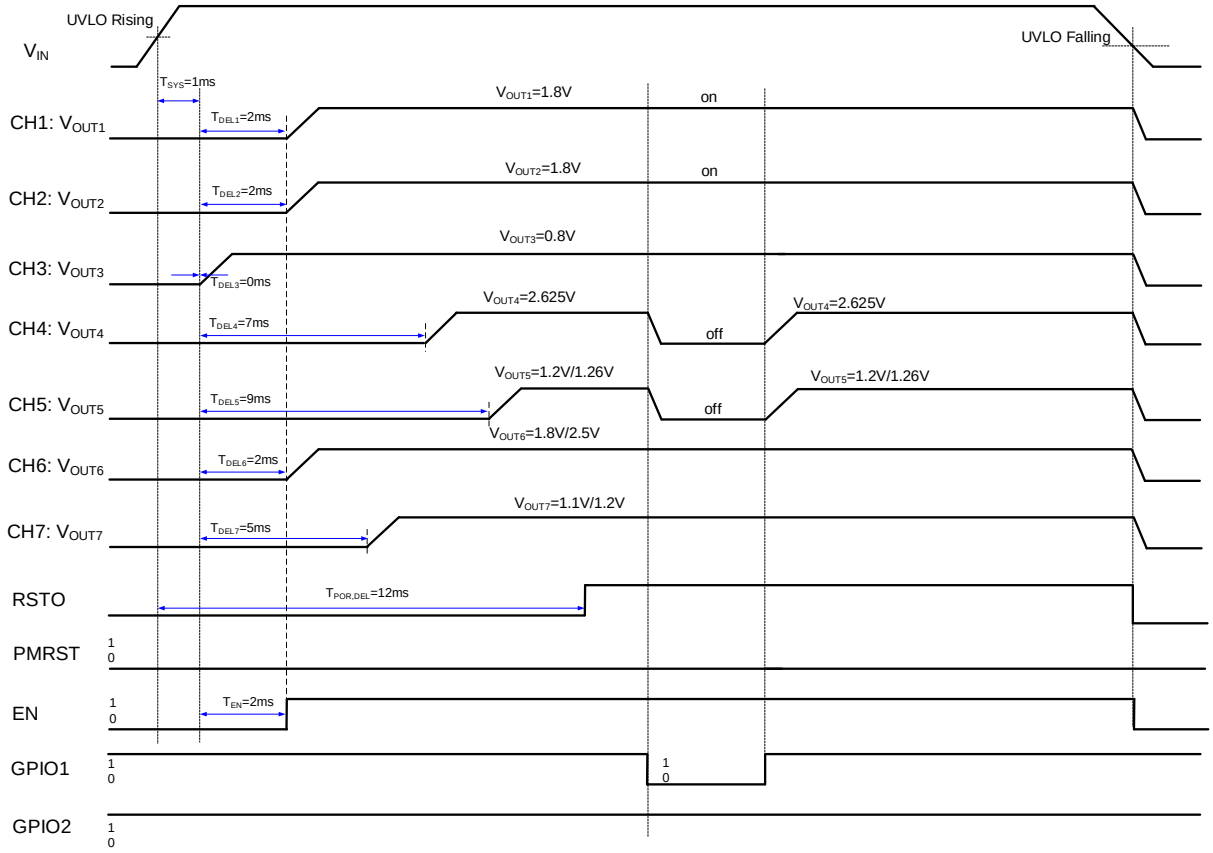


Figure 5. Low Power Mode 1 Controlled by GPIO1

Low Power Mode2 (PS4.0)

When GPIO1 and GPIO2 are pulled low at the same time, the PMIC enters Low Power Mode 2 (PS4.0), CH4/CH5/CH6/CH7 are turned off, and CH3 output voltage changes to 0.77V. When GPIO1 and GPIO2 are pulled high at the same time, the PMIC exists sleep mode and CH4/CH5/CH6/CH7 are turned on at the same time, as shown in Figure 6.

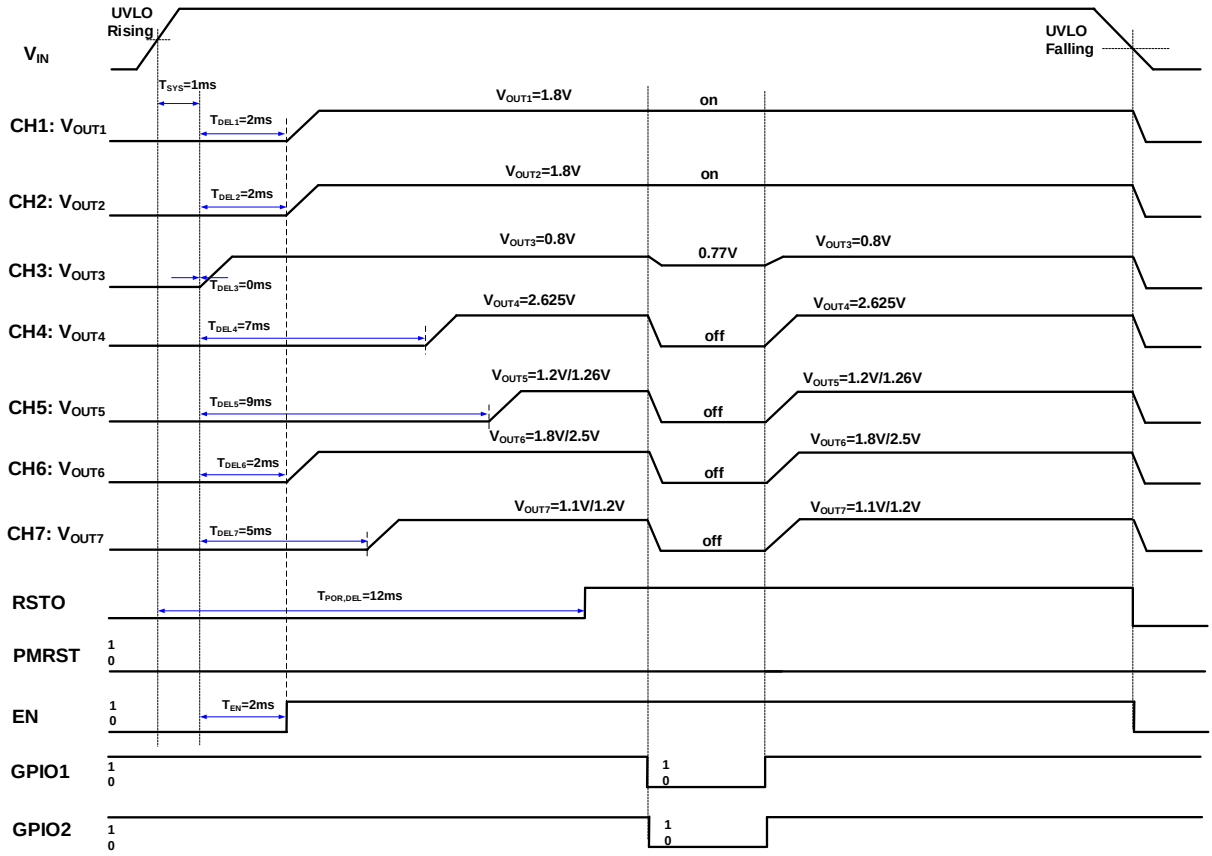


Figure 6. Low Power Mode 2 Controlled by GPIO1 and GPIO2

CH5, CH6, and CH7 Default Output Voltage Selection

VSEL6 is used to select CH5 default output voltage, and VSEL7 is used to select CH6 and CH7 default output voltages. VSEL6 or VSEL7 should be tied to V_{IN} to select high level input, or to GND to select low level input.

Table 3. CH5/6/7 Output Voltage Selection

CH5		CH6		CH7	
VSEL6	V_{OUT5}	VSEL7	V_{OUT6}	VSEL7	V_{OUT7}
0	1.2V	0	1.8V	0	1.1V
1	1.26V	1	2.5V	1	1.2V

Fault-Protection Modes

Buck and LDO Undervoltage Protection and Hard-Short Protection

All buck and LDO channels work in hiccup and auto-retry mode in hard-short protection mode. LDO1 and LDO2 have internal counters that start when a hard-short condition occurs. If a hard-short condition lasts longer than 200μs, the related channel will turn off for 3ms to avoid the thermal dissipation increase, then start again as shown in Figure 7.

LDO1/LDO2 hard-short conditions will not affect other channels' normal operation.

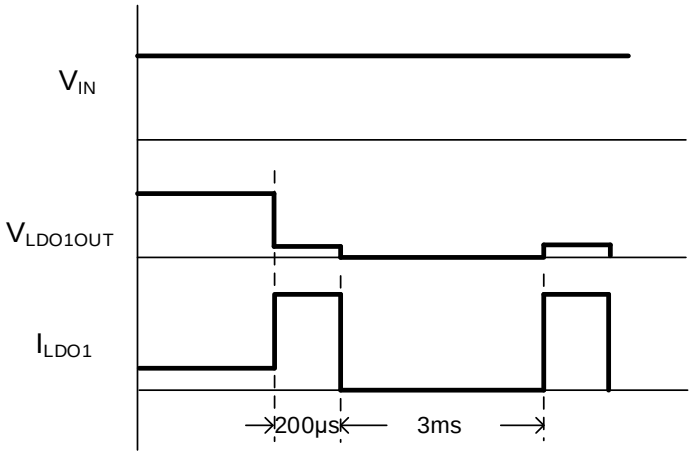


Figure 7. Undervoltage/Hard-Short Protection

V_{IN} Overvoltage Protection

If input voltage exceeds the input overvoltage protection (OVP) threshold of 3.9V, the overvoltage protection is triggered and all channels are turned off. If V_{IN} falls below the threshold, all channels will restart with a predefined delay time.

Overtemperature Protection

If the junction temperature exceeds the t_{SD} threshold (155°C), the device turns off all channels. If the junction temperature falls below the t_{SD} -t_{HYS}, all channels will restart after a predefined delay time.

Table 4. PMIC Protection

Mode	Threshold	Action
Hard-Short	30%	Auto-Retry
Input OVP	3.85V	Entire chip turns off and recovers when V_{IN} falls below VIN_{OVP} -VIN_{OVP_HYS} threshold.
Thermal Shutdown	155°C	Entire chip turns off and recovers when V_{IN} falls below t_{SD} -t_{HYS} threshold.

Application Information

The following paragraphs provide information on selecting the external components for each of the buck converters, to match the application requirements.

Input Capacitor C_{INX}

For the best performance, select typical X5R or better grade ceramic capacitors with a 6.3V or higher rating, and at least 10μF capacitance. The capacitor should be placed as close as possible to the corresponding pin on the device, while also minimizing the loop area formed by C_{INx} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current. The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10μF X5R capacitor is sufficient for each of the buck converters in most applications.

Output Inductor L_X

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21523x has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 20mΩ to achieve good overall efficiency.

Output Capacitor C_{OUTX}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use two X5R or better grade ceramic capacitors with a 10V rating, and capacitance of at least 22μF for each converter output.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔIL) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

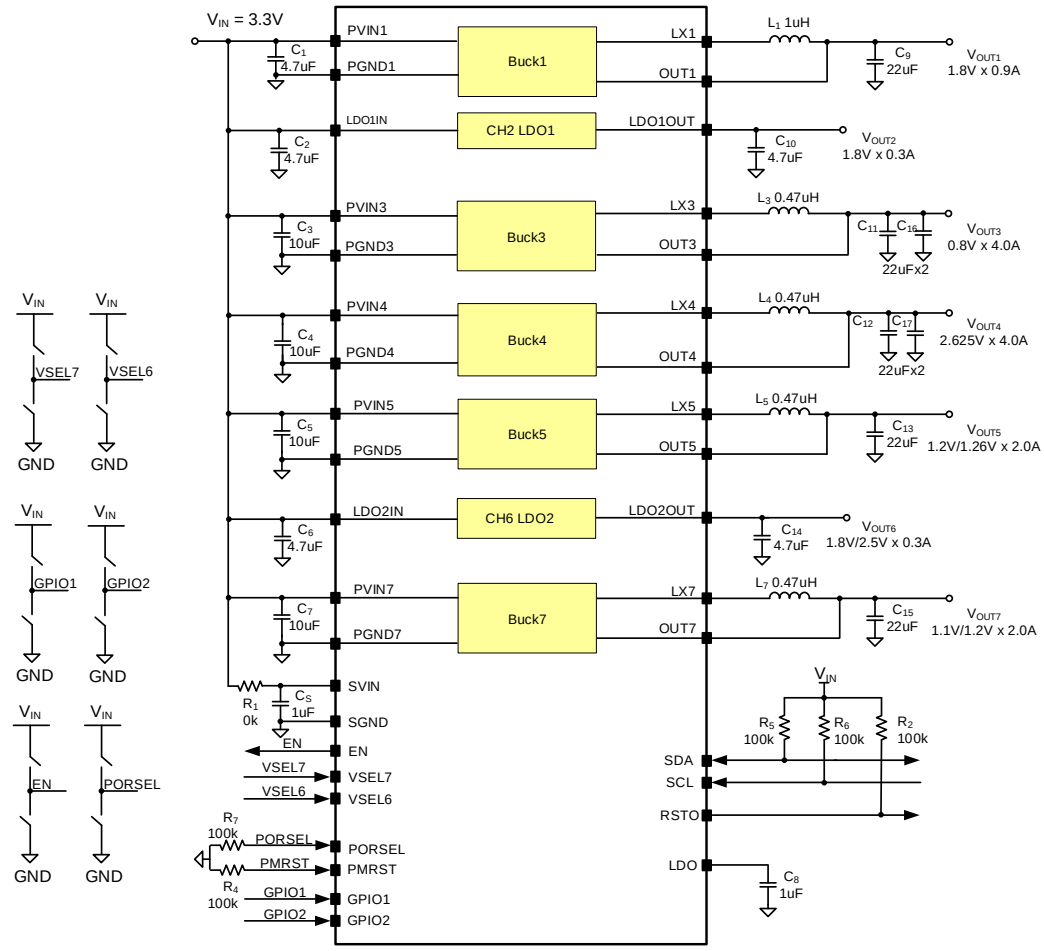
LDO Input Capacitor

A 1μF to 10μF capacitor placed on the input side of the LDO can filter the noise and ensure the stability of the LDO. The input capacitor is recommended to be placed near the input side pin, the closer the better.

LDO Output Capacitor

The SY21523x is designed as a stable standard ceramic capacitor with a recommended output value of 1μF to 10μF. Considering the capacitance tolerance and DC bias effect, the minimum stable working capacitance is 1μF.

Application Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	PMIC	SY21523x	Silergy
L_1	1μH,85mΩ,1.5A	MLP2520S1R0M	TDK
L_3,L_4,L_5,L_7	0.47μH,17mΩ,6A	WPN252010UFR47MT	Sunlord
C_1,C_2,C_6,C_{10},C_{14}	4.7μF/10V,0402	C1005X5R1A475K	TDK
C_3,C_4,C_5,C_7	10μF/10V,0603	C1608X5R1A106K	TDK
C_s ,C_8	1μF/10V,0402	C1005X6S1A105K	TDK
C_9,C_{11},C_{12},C_{13},C_{15},C_{16},C_{17}	22μF/6.3V,0603	C1608X5R0J226M	TDK
R_1	0k,0402		
R_2, R_4, R_5, R_6, R_7	100k, 0603		

Layout Design

Follow these PCB layout guidelines for optimal performance:

- Place C and L as close as possible to the IC to improve efficiency and provide better noise immunity.
- Maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance.
- Place the decoupling capacitor of PVIN1 close to the PVIN1 and PGND1 pins. Minimize the loop area formed by the input capacitors, input pins, and PGND pins. Apply the same principle of decoupling capacitor placement for all bucks and LDOs.
- Place the inductor as close as possible to the chip while keeping the switching node small. Minimize the PCB copper area associated with the LX pin to improve noise immunity, and to reduce parasitic inductance and parasitic resistance.
- Use multiple vias for high current connections when changing the routing layers to provide adequate current carrying capability.
- Avoid routing the feedback lines (VOUT) close to LX(s) or other high-frequency signal lines (SCL/SDA) as much as possible to prevent noise from affecting the output.

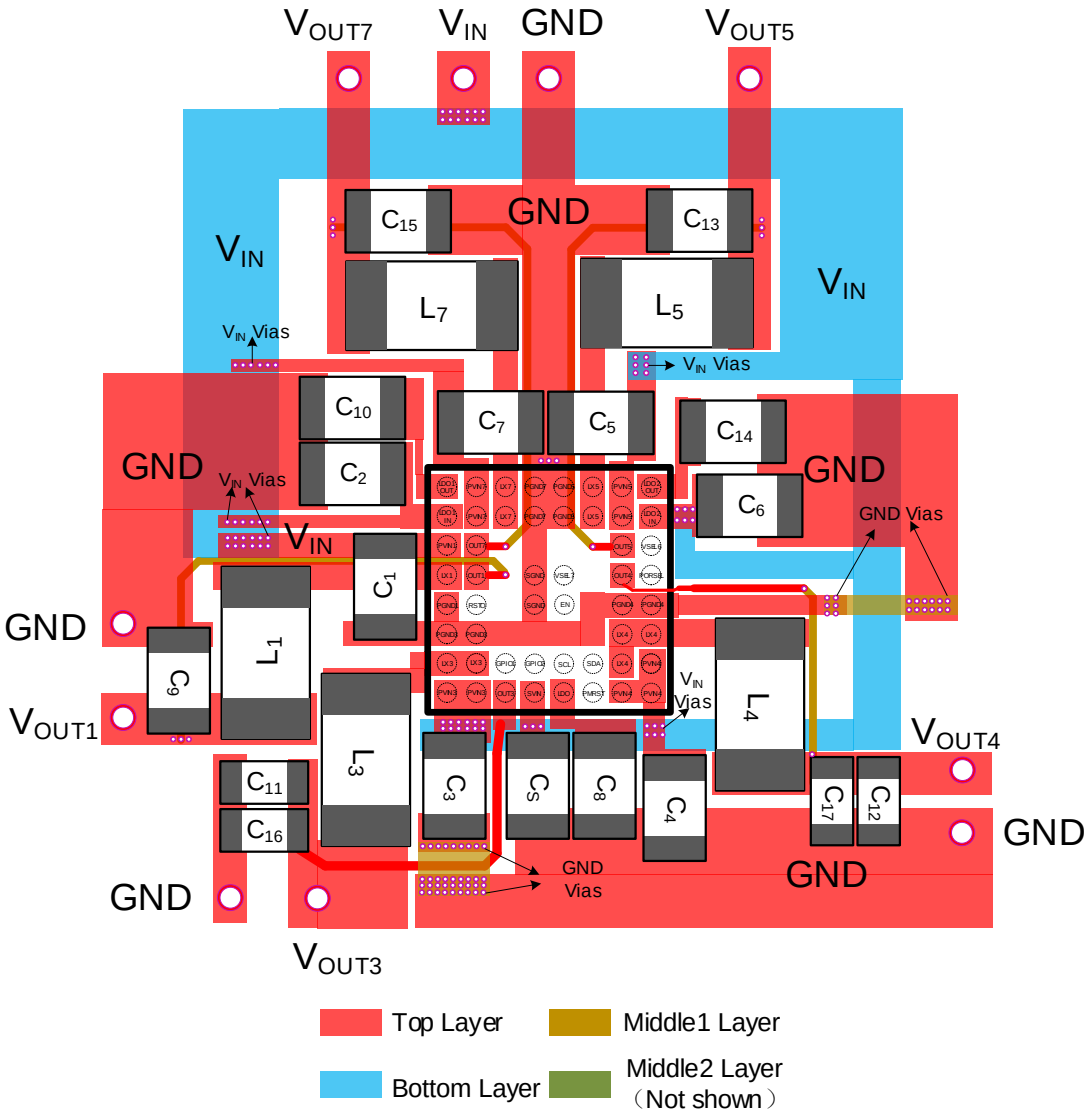


Figure 8. Suggested PCB Layout

I²C Compatible Interface

The SY21523x features an I²C interface that allows the host processor to control the configuration and the output voltage level of all channels for the DVS function. The I²C interface supports clock speeds of up to 3.4MHz and uses standard I²C commands. The SY21523x always operates as a peripheral device and is addressed using a 7-bit peripheral address followed by an eighth bit, which indicates whether the transaction is a read operation or a write operation: LSB = 0 indicates write mode and LSB = 1 indicates read mode.

Table 5. SY21523x Peripheral Address

Binary	Hex	Read/Write
0110 0000	0x60	Write
0110 0001	0x61	Read

START and STOP Conditions

The SY21523x is controlled via an I²C compatible interface. The START condition is a high-to low transition of the SDA line while SCL is high. The STOP condition is a low-to-high transition on the SDA line while SCL is high. A STOP condition must be sent before each START condition. The I²C host always generates the START and STOP conditions.

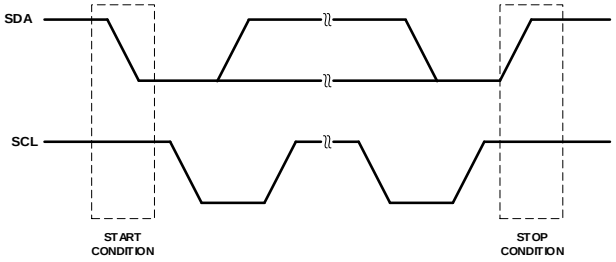


Figure 9. START and STOP

Data Validity

The data on the SDA line must be stable during the high period of the SCL unless generating a START or STOP condition. The high or low state of the data line can only change when the clock signal on the SCL line is low.

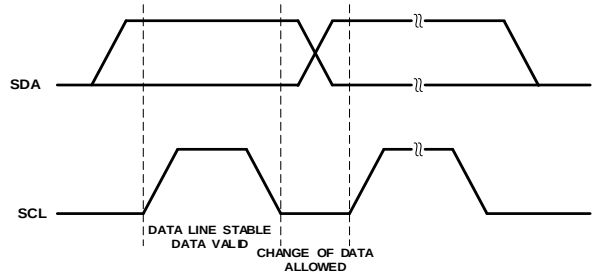


Figure 10. Data Validity

Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the host sends seven peripheral address bits and an R/$\overline{W}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its address holds the data line low to acknowledge. The acknowledge bit is also used by both the host and peripheral to acknowledge receipt of register addresses and data.

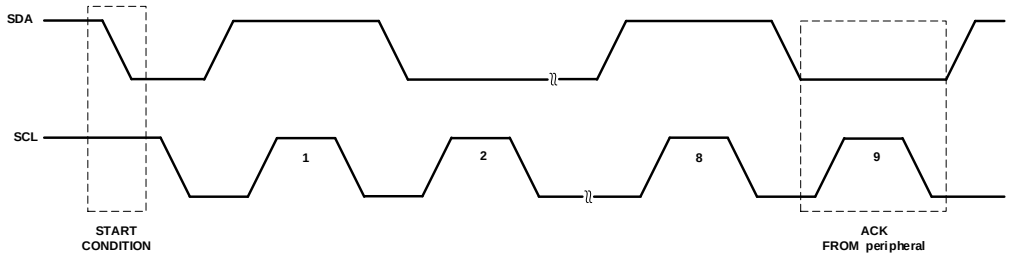


Figure 11. Acknowledge from Peripheral

Data Transactions

All transactions start with a control byte sent from the I²C host device. The control byte begins with a START condition, followed by seven bits of peripheral address (0110000x) for the SY21523x (this address can be changed if necessary) followed by the eighth bit, the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any peripheral devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no peripherals exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SY21523x acknowledges it, the second byte sent by the host must

be a register address byte. The register address byte tells the SY21523x which register the host will write or read.

Once the SY21523x receives a register address byte, it responds with an acknowledgment.

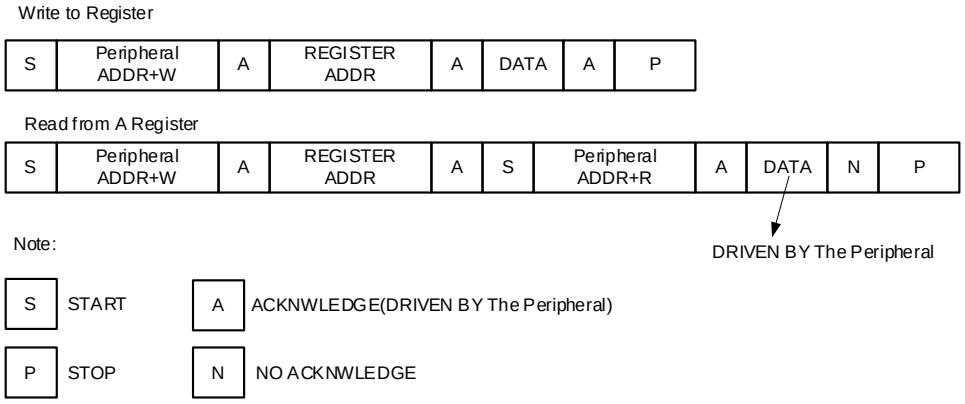


Figure 12. I²C Timing

Register Map

Register Map Summary

Register Address	Register Name	Default Configuration	Default Value (HEX)	Register Description
0x01	OUT3_SET	0.8V	0x0A	Voltage Setting for Buck Channel 3
0x02	OUT4_SET	2.625V	0x03	Voltage Setting for Buck Channel 4
0x03	ENABLE_REG	All Channels ON	0xFF	Channel Enable/Disabled
0x04	DISCHARGE_REG	Discharge ON	0x7F	Channel Discharge Enable/Disable
0x05	MODE_REG	Auto PWM/PFM	0x1F	Auto PWM/PFM Mode or Forced PWM Mode Control
0x06	SLP_OUT3_SET	0.77V	0x07	Sleep Mode Voltage Setting for Buck Channel 3
0x07	SLP_OUT4_SET	2.625V	0x03	Sleep Mode Voltage Setting for Buck Channel 4
0x08	SLP_ENABLE_REG	CH1/CH2/CH3 ON, Other Channels OFF	0x07	Sleep Mode Channel Enable/Disabled, and Sleep Mode Control

Register Settings

Channel 3 Output Voltage Setting Register (0x01)

This register sets Channel 3 output voltage; $V_{OUT3\_DEFAULT}$ = 0.8V

Register Name	OUT3_REG			Output Voltage Setting Register for Channel 3			
Address				0x01			
Field	Bit	R/W	Default	Output voltage setting for OUT3. DVS from 0.7V to 1.1V in 10mV steps.			
VOUT3_SET	5:0	R/W	Default 0x0A = 0.8V	0x00 = 0.70V	0x01 = 0.71V	0x02 = 0.72V	0x03 = 0.73V
				0x04 = 0.74V	0x05 = 0.75V	0x06 = 0.76V	0x07 = 0.77V
				0x08 = 0.78V	0x09 = 0.79V	0x0A = 0.80V	0x0B = 0.81V
				0x0C = 0.82V	0x0D = 0.83V	0x0E = 0.84V	0x0F = 0.85V
				0x10 = 0.86V	0x11 = 0.87V	0x12 = 0.88V	0x13 = 0.89V
				0x14 = 0.90V	0x15 = 0.91V	0x16 = 0.92V	0x17 = 0.93V

				0x18 = 0.94V	0x19 = 0.95V	0x1A = 0.96V	0x1B = 0.97V
				0x1C = 0.98V	0x1D = 0.99V	0x1E = 1.00V	0x1F = 1.01V
				0x20 = 1.02V	0x21 = 1.03V	0x22 = 1.04V	0x23 = 1.05V
				0x24 = 1.06V	0x25 = 1.07V	0x26 = 1.08V	0x27 = 1.09V
				0x28 = 1.10V	0x29 = 1.10V	0x2A = 1.10V	0x2B = 1.10V
				0x2C = 1.10V	0x2D = 1.10V	0x2E = 1.10V	0x2F = 1.10V
Reserved	7:6	R/W	0	Reserved			

Channel 4 Output Voltage Setting Register (0x02)

This register sets Channel 4 output voltage; $V_{OUT4\_DEFAULT}$ = 2.625V

Register Name	OUT4_REG			Output Voltage Setting Register for Channel 4			
Address				0x02			
Field	Bit	R/W	Default	Output voltage setting for OUT4. DVS from 2.3625V to 3.15V in 87.5mV steps.			
VOUT4_SET	3:0	R/W	Default 0x03 = 2.625V	0x00 = 2.3625V	0x01 = 2.45V	0x02 = 2.5375V	0x03 = 2.625V
				0x04 = 2.7125V	0x05 = 2.8V	0x06 = 2.8875V	0x07 = 2.975V
				0x08 = 3.0625V	0x09 = 3.15V	0x0A = 3.15V	0x0B = 3.15V
				0x0C = 3.15V	0x0D = 3.15V	0x0E = 3.15V	0x0F = 3.15V
Reserved	7:4	R/W	0	Reserved			

ON/OFF Control Register (0x03)

Register Name	ON/OFF_CONTROL			Channel ON/OFF Control Register	
Address				0x03	
Field	Bit	R/W	Default	Description	
EN1	0	R/W	1	CH1 ON/OFF control	
				0: Disable	1: Enable
EN2/EN	1	R/W	1	CH2 and external DC/DC ON/OFF control	
				0: Disable	1: Enable
EN3	2	R/W	1	CH3 ON/OFF control	
				0: Disable	1: Enable
EN4	3	R/W	1	CH4 ON/OFF control	
				0: Disable	1: Enable
EN5	4	R/W	1	CH5 ON/OFF control	
				0: Disable	1: Enable
EN6	5	R/W	1	CH6 ON/OFF control	
				0: Disable	1: Enable
EN7	6	R/W	1	CH7 ON/OFF control	
				0: Disable	1: Enable
Reserved	7	R/W	0	Reserved	

Discharge Function Control Register (0x04)

This register controls the output discharge function during PMIC shutdown mode. DC/DC converter discharge function operates during the power-off sequence and when V_{IN} is turned off, when the value is set to 1.

Register Name	Discharge Control			Channel Discharge Control	
Address				0x04	
Field	Bit	R/W	Default	Description	
ENDIS_CH1	0	R/W	1	CH1 discharge control	
				0: Disable	1: Enable
ENDIS_CH2	1	R/W	1	CH2 discharge control	
				0: Disable	1: Enable
ENDIS_CH3	2	R/W	1	CH3 discharge control	
				0: Disable	1: Enable
ENDIS_CH4	3	R/W	1	CH4 discharge control	
				0: Disable	1: Enable
ENDIS_CH5	4	R/W	1	CH5 discharge control	
				0: Disable	1: Enable
ENDIS_CH6	5	R/W	1	CH6 discharge control	
				0: Disable	1: Enable
ENDIS_CH7	6	R/W	1	CH7 discharge control	
				0: Disable	1: Enable
Reserved	7	R/W	0	Reserved	

DC/DC Mode Control Register (0x05)

This register controls Buck DC/DC Regulator PWM/PFM mode operation during light load conditions. If MODE(n) bit is set to 1, CH(n) buck converters operate in forced PWM mode. If MODE(n) bit is set to 0, CH(n) operate in PFM mode under light load conditions.

Register Name	PWM/PFM_REG			PWM/PFM Mode Selection Register	
Address				0x05	
Field	Bit	R/W	Default	Description	
MODE1	0	R/W	1	Channel 1 mode control bit	
				0 = Forced PWM	1 = Auto PFM/PWM
MODE3	1	R/W	1	Channel 3 mode control bit	
				0 = Forced PWM	1 = Auto PFM/PWM
MODE4	2	R/W	1	Channel 4 mode control bit	
				0 = Forced PWM	1 = Auto PFM/PWM
MODE5	3	R/W	1	Channel 5 mode control bit	
				0 = Forced PWM	1 = Auto PFM/PWM
MODE7	4	R/W	1	Channel 7 mode control bit	
				0 = Forced PWM	1 = Auto PFM/PWM
Reserved	7:5	R/W	0	Reserved	

Ch3 Sleep Mode Output Voltage Setting Register (0x06)

This register sets Channel 3 sleep mode output voltage; $V_{OUT3\_DEFAULT}$ = 0.77V

Register Name	SLP_OUT3_REG			Output Voltage Setting Register for Channel 3			
Address				0x06			
Field	Bit	R/W	Default	Output voltage setting for OUT3. DVS from 0.7V to 1.1V in 10mV steps.			
SLP_VOUT3_SET	5:0	R/W	Default 0x07 = 0.77V	0x00 = 0.70V	0x01 = 0.71V	0x02 = 0.72V	0x03 = 0.73V
				0x04 = 0.74V	0x05 = 0.75V	0x06 = 0.76V	0x07 = 0.77V
				0x08 = 0.78V	0x09 = 0.79V	0x0A = 0.80V	0x0B = 0.81V
				0x0C = 0.82V	0x0D = 0.83V	0x0E = 0.84V	0x0F = 0.85V
				0x10 = 0.86V	0x11 = 0.87V	0x12 = 0.88V	0x13 = 0.89V
				0x14 = 0.90V	0x15 = 0.91V	0x16 = 0.92V	0x17 = 0.93V
				0x18 = 0.94V	0x19 = 0.95V	0x1A = 0.96V	0x1B = 0.97V
				0x1C = 0.98V	0x1D = 0.99V	0x1E = 1.00V	0x1F = 1.01V
				0x20 = 1.02V	0x21 = 1.03V	0x22 = 1.04V	0x23 = 1.05V
				0x24 = 1.06V	0x25 = 1.07V	0x26 = 1.08V	0x27 = 1.09V
				0x28 = 1.10V	0x29 = 1.10V	0x2A = 1.10V	0x2B = 1.10V
				0x2C = 1.10V	0x2D = 1.10V	0x2E = 1.10V	0x2F = 1.10V
Reserved	7:6	R/W	0	Reserved			

Sleep Mode Channel 4 Output Voltage Setting Register (0x07)

This register sets Channel 4 output voltage at sleep mode. $V_{SLP\_OUT4\_DEFAULT}$ = 2.625V

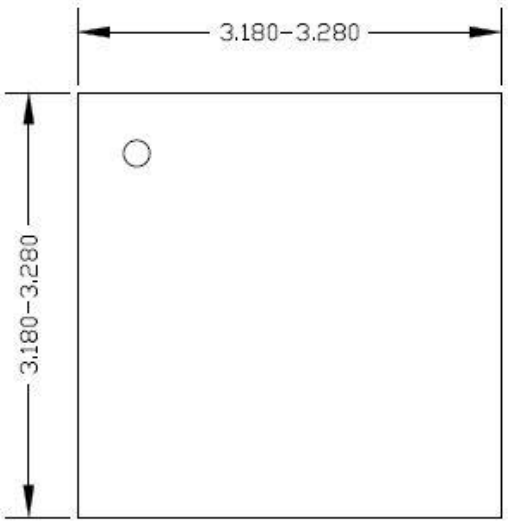
Register Name	SLP_OUT4_REG			Output Voltage Setting Register for Channel 4			
Address				0x07			
Field	Bit	R/W	Default	Output voltage setting for OUT4. DVS from 2.3625V to 3.15V in 87.5mV steps.			
SLP_VOUT4_SET	3:0	R/W	Default 0x03 = 2.625V	0x00 = 2.3625V	0x01 = 2.45V	0x02 = 2.5375V	0x03 = 2.625V
				0x04 = 2.7125V	0x05 = 2.8V	0x06 = 2.8875V	0x07 = 2.975V
				0x08 = 3.0625V	0x09 = 3.15V	0x0A = 3.15V	0x0B = 3.15V
				0x0C = 3.15V	0x0D = 3.15V	0x0E = 3.15V	0x0F = 3.15V
Reserved	7:4	R/W	0	Reserved			

Sleep Mode ON/OFF Control Register (0x08)

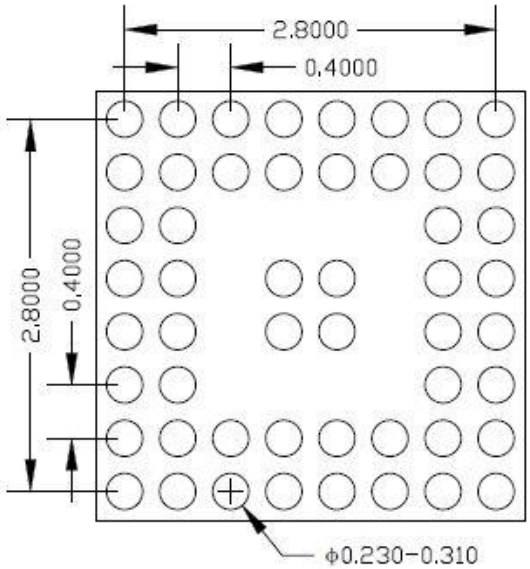
Register Name	SLP_ON/OFF_CONTROL			Channel Sleep Mode ON/OFF Control Register	
Address				0x08	
Field	Bit	R/W	Default	Description	
SLP_EN1	0	R/W	1	Sleep mode CH1 ON/OFF control	
				0: Disable	1: Enable
SLP_EN2	1	R/W	1	Sleep mode CH2/EN ON/OFF control	
				0: Disable	1: Enable
SLP_EN3	2	R/W	1	Sleep mode CH3 ON/OFF control	
				0: Disable	1: Enable
SLP_EN4	3	R/W	0	Sleep mode CH4 ON/OFF control	
				0: Disable	1: Enable
SLP_EN5	4	R/W	0	Sleep mode CH5 ON/OFF control	

				0: Disable	1: Enable
SLP_EN6	5	R/W	0	Sleep mode CH6 ON/OFF control	
				0: Disable	1: Enable
SLP_EN7	6	R/W	0	Sleep mode CH7 ON/OFF control	
				0: Disable	1: Enable
SLEEP	7	R/W	0	Sleep mode control bit	
				0: PMIC exit sleep mode	1: PMIC enter sleep mode

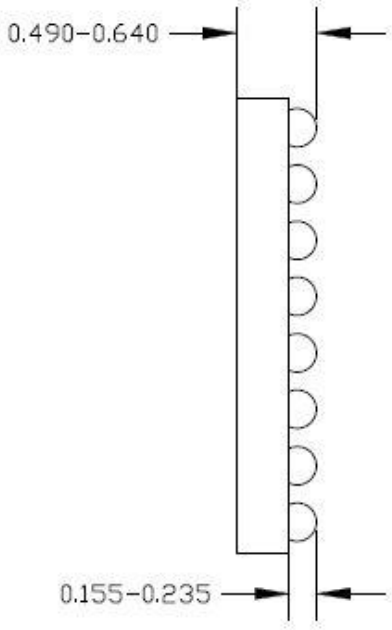
CSP3.23×3.23-52 Package Outline Drawing



Top view



Bottom view



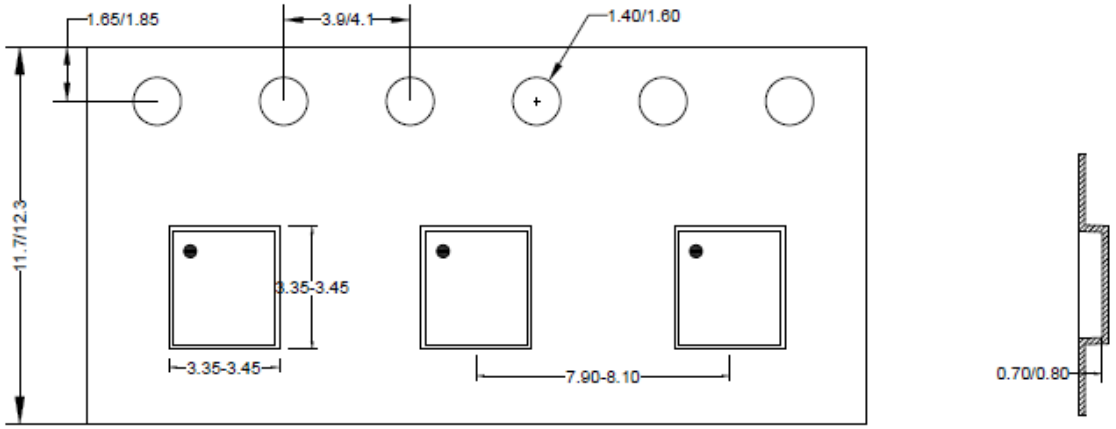
Side View

Notes: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Tape and Reel Information

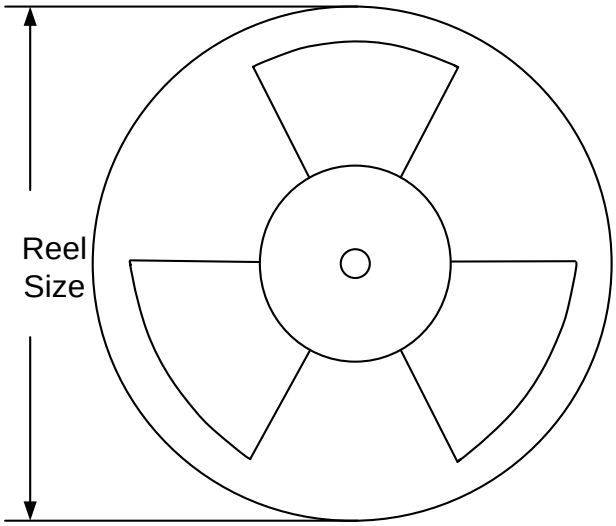
Tape Dimensions and Pin 1 Orientation

CSP3.23×3.23



Direction of feed ⟶

Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
CSP3.23×3.23	12	8	13"	400	400	5000

All Dimension are nominal

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr. 08, 2021	Revision 0.9	Initial release.
Aug. 13, 2024	Revision 1.0	Combine specification of SY21523C and SY21523E.

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license.** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com