

General Description

The SY205209ABC is a quad, low capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 1.2pF, the SY205209ABC is designed to protect against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD) ($\pm 30\text{kV}$ air, $\pm 30\text{kV}$ contact discharge), IEC 61000-4-5 (surge) (7.5A, 8/20 μs).

The low capacitance, small size and high ESD robustness makes SY205209ABC ideal for high-speed lines used in high-frequency interface applications (e.g., VGA & DVI). The low clamping voltage of the SY205209ABC guarantees minimum stress on the protected IC.

Each SY205209ABC device can protect four high-speed data lines. The SY205209ABC is available in a compact SOT23-6 package.

Features

- Transient Protection for High-Speed Data Lines
 - IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (Air) $\pm 30\text{kV}$ (Contact)
 - IEC 61000-4-5 (Surge) 7.5A (8/20 μs)
- Protects Four Data Lines
- Low Capacitance: 1.2pF Typical (I/O-GND)
- Low Leakage Current: 0.01mA @ V_{RWM} (Typical)
- Low Clamping Voltage
- Back-Drive Protection for Power-Down Mode

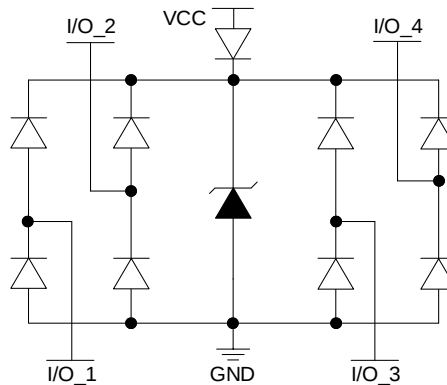
Applications

- Desktops, Servers, and Notebooks
- USB 2.0 Power and Data Line Protection
- Display Ports
- Video Graphics Cards
- Digital Visual Interfaces (DVI)

Mechanical Characteristics

- SOT23-6 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

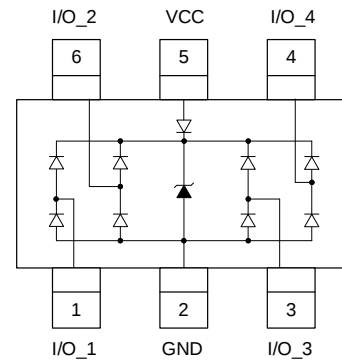
Circuit Diagram



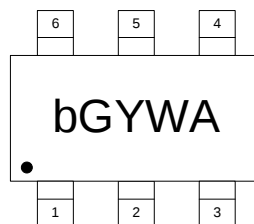
Ordering Information

Part Number	Package Type	Top Mark
SY205209ABC	SOT23-6 RoHS Compliant and Halogen Free	bGYWA

Pinout (Top View)



Marking Codes



Note 1: “bG” is device code, fixed.

Note 2: “YWA” is date code.

Absolute Maximum Rating				
Parameter	Symbol	Min	Max	Unit
Maximum Peak Pulse Current (8/20μs) (VCC&I/O pins)	I_{PP}		7.5	A
Maximum Peak Pulse Power (8/20μs) (VCC&I/O pins)	P_{PK}		100	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	-30	30	kV
Operating Temperature	T_{OPT}	-40	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics $T_A = 25^{\circ}\text{C}$						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	V_{RWM}				5.0	V
Reverse Leakage Current @ V_{RWM}	I_R	$V_{RWM} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$ From Pin1/3/4/5/6 to Pin2		0.01	0.1	μA
Reverse Breakdown Voltage @ I_T	V_{BR}	$I_T = 1\text{mA}$ From Pin1/3/4/5/6 to Pin2	6.0	8.0	10.0	V
Forward Voltage @ I_F	V_F	$I_F = 1\text{mA}$ From Pin2 to Pin1/3/4/5/6	0.4	0.7	1.2	V
Clamping Voltage @ I_{PP}	$V_C (1)$	$I_{PP} = 7.5\text{A}$, $t_p = 8/20\mu\text{s}$ From Pin1/3/4/5/6 to Pin2		11	13	V
Clamping Voltage @ I_{PP}	$V_C (1)$	$I_{PP} = 16\text{A}$, $t_p = 10/100\text{ns}$ From Pin1/3/4/5/6 to Pin2		12		V
Dynamic Resistance	$R_{DYN} (1,2)$	$t_p = 10/100\text{ns}$ From Pin1/3/4/5/6 to Pin2		0.25		Ω
Parasitic Capacitance	$C_{ESD} (1)$	$V_R = 2.5\text{V}$, $f = 1\text{MHz}$ From Pin1/3/4/5/6 to Pin2		1.20	1.50	pF
Parasitic Capacitance	$C_{ESD} (1)$	$V_R = 2.5\text{V}$, $f = 1\text{MHz}$ Between I/O and I/O		0.60	0.75	pF

Note 1: The device is not guaranteed to function outside its operating conditions.

Note 2: R_{DYN} calculated based on $I_{PP}=8\text{A}$ to $I_{PP}=16\text{A}$, $t_p = 10/100\text{ns}$.

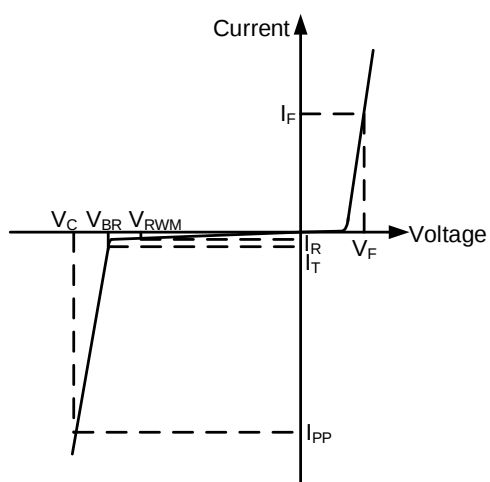
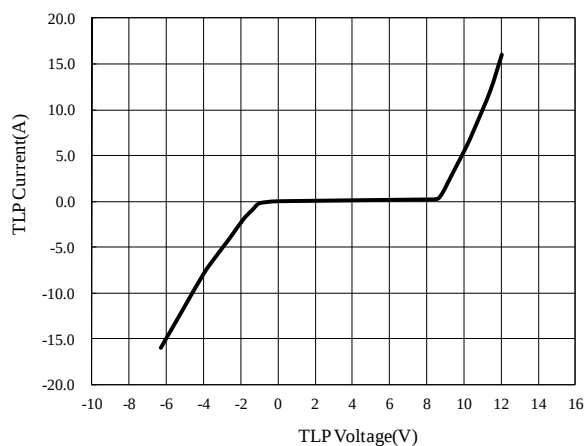


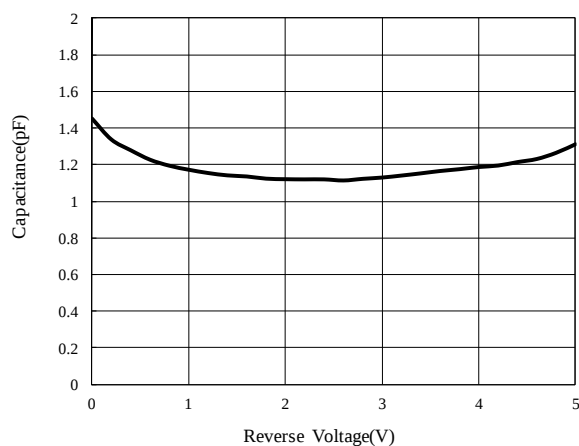
Figure 1. Uni-Directional TVS

Typical Characteristics

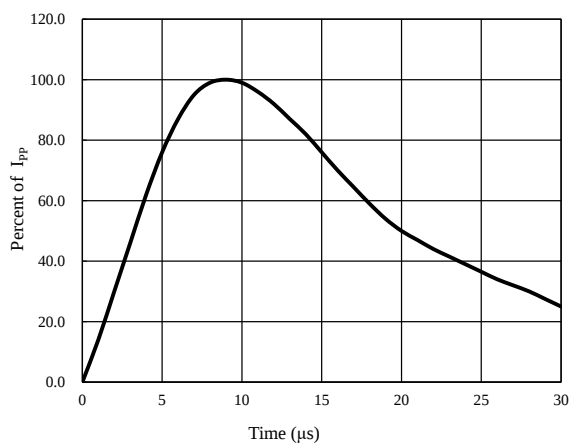
TLP Testing of I/O to GND



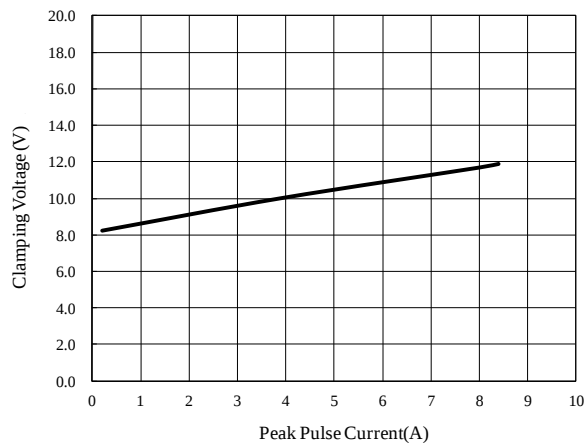
Capacitance vs. Voltage of I/O to GND



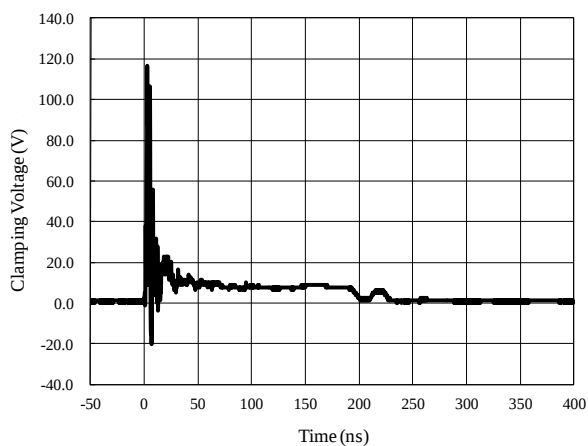
Pulse Waveform



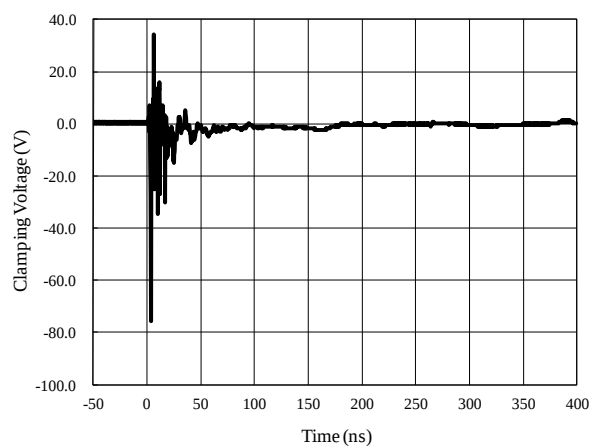
Clamping Voltage vs. Peak Pulse Current (8/20 μ s)



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Universal Serial Bus (USB) ESD Protection

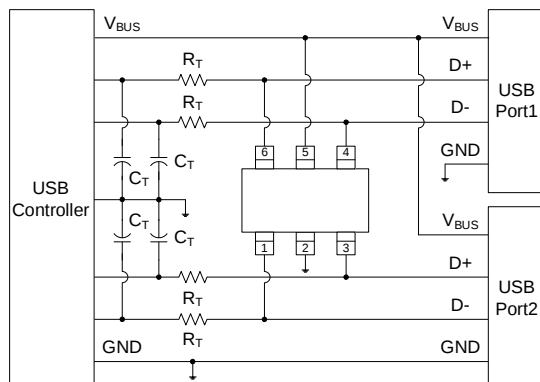


Figure 2. Typical ESD Protection for USB 2.0

Pin1 of SY205209ABC is connected to the D+ of one USB port, and Pin3 is connected to the D- of the same port. Similarly, Pin6 is connected to the D+ of the second USB port, and Pin4 is connected to the D-. To ensure power line protection, connect Pin5 directly to V_{BUS} .

SY205209ABC is designed to offer ESD protection solutions for various interface applications. By connecting the I/O to the data lines and attaching Pin2 to the ground, any positive transient line-to-ground ESD event can be discharged via the forward steering diode and Zener diode. Additionally, negative line-to-ground transients can be directly discharged to ground through the steering diode. Line-to-line discharges are managed through the Zener diode in combination with two forwarded steering diodes.

Back-Drive Protection

Back-drive protection protects against reverse current flowing from a high potential voltage node toward a lower potential voltage node through the interface cable.

For example, consider a VGA source connected to a VGA monitor via a VGA interface. If the VGA source is switched off and the VGA monitor is left on, there is a possibility of reverse current flow back into the main power supply rail of the VGA source. Typically, the power supply of the VGA source has some form of associated bulk supply capacitance, and it is possible over time to charge that bulk supply capacitance to some intermediate level. If that level rises above the voltage level of some of the integrated circuits, the VGA source may not reset properly when the VGA source is turned on. To avoid this situation, the SY205209ABC with the integrated back-drive protection diode was designed to block back-drive current for power-down mode.

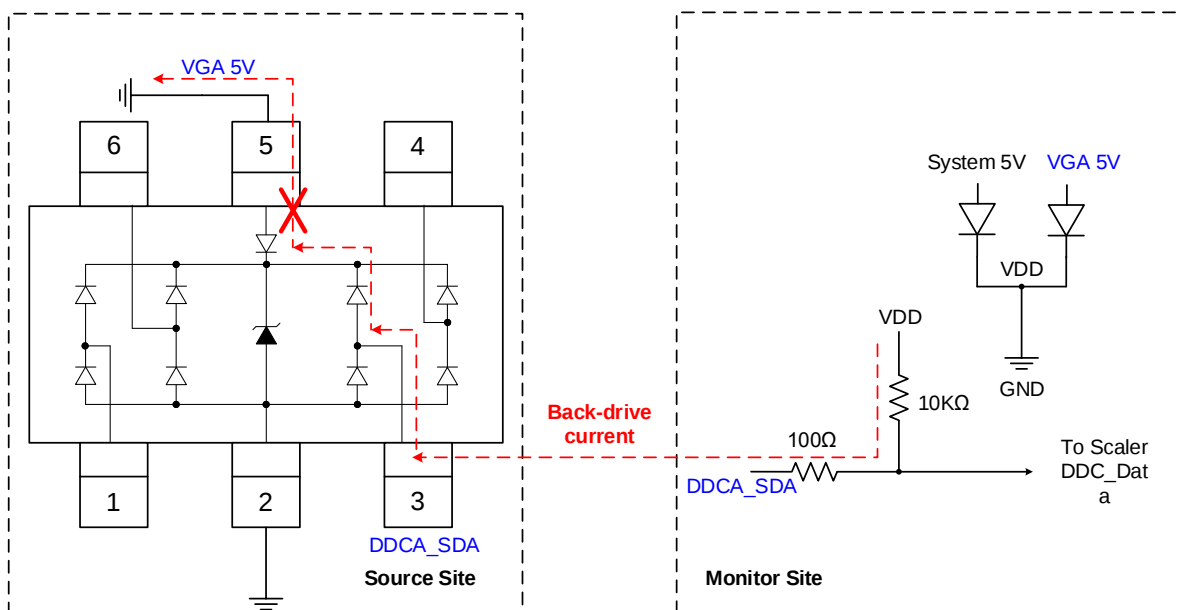


Figure 3. TVS Array with Back-drive Protection

PCB Layout Guidelines

SY205209ABC is able to provide ESD protection for four data lines simultaneously. The pin connections are shown in Figure 4.

Four parallel data lines, from driver IC to the I/O port connector, can connect to the SY205209ABC four I/O pins directly. Pin 2 of SY205209ABC is the negative reference pin, which should connect to the GND. The connection wires should be as short as possible to minimize the parasitic inductance.

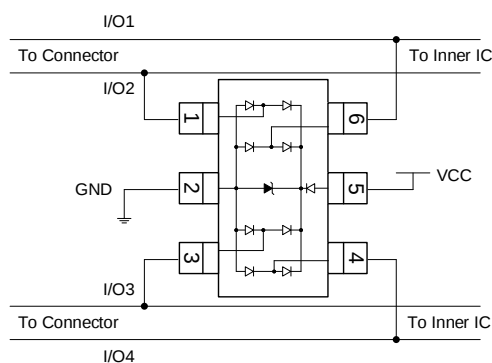


Figure 4. SY205209ABC Pin Connection in PCB

PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205209ABC as close to the connector port as possible.
- The distance between the SY205209ABC ground pin and the GND reference path should be as short as possible.
- Use a large via to connect the SY205209ABC VCC and GND pins to the PCB VCC and GND, respectively.
- Avoid running critical signals near board edges.

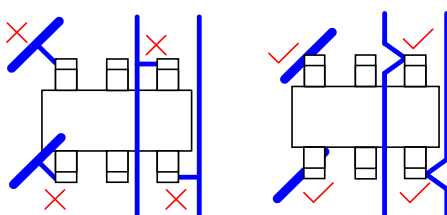
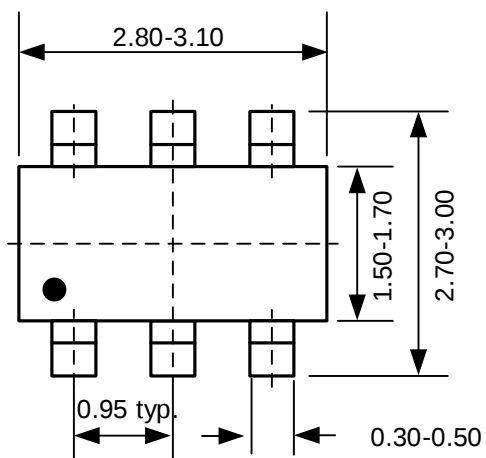
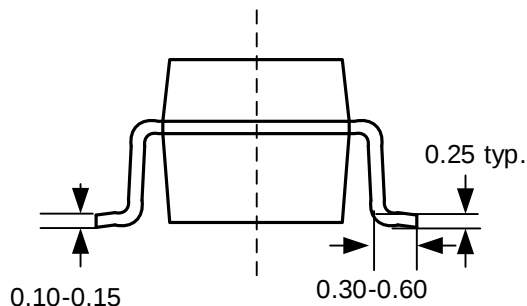


Figure 5. SY205209ABC Layout Guideline

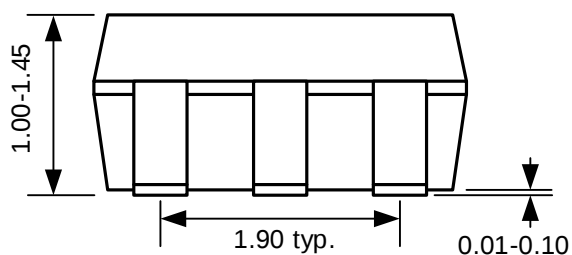
SOT23-6 Package Outline



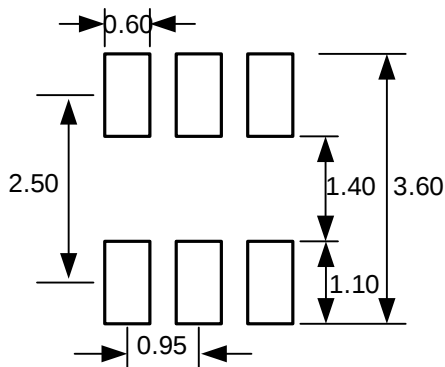
Top View



Side View



Side View

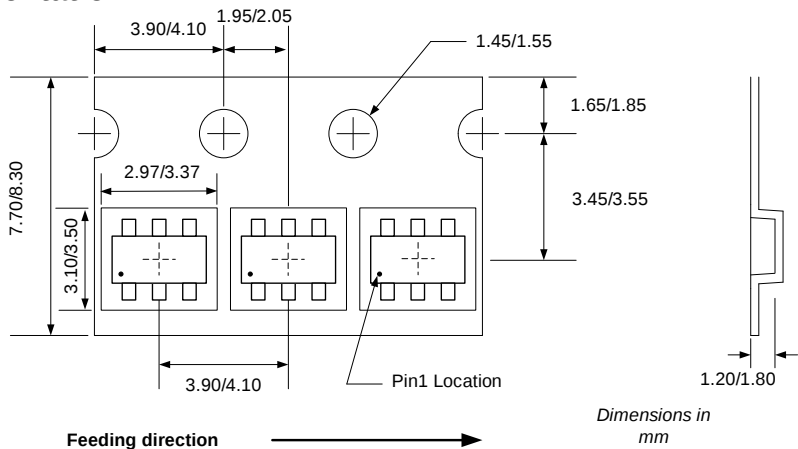


**Recommended PCB Layout
(Reference only)**

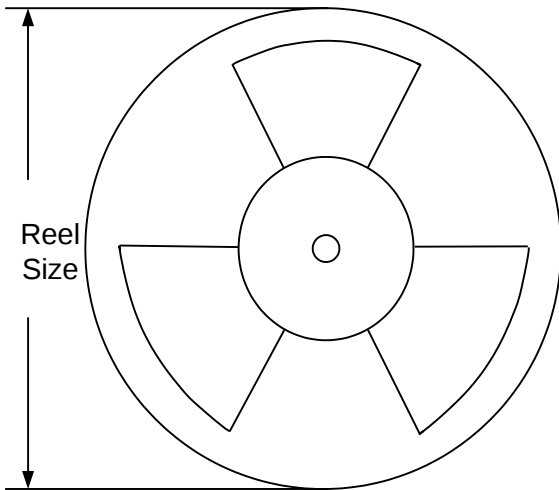
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Specification

SOT23-6 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Qty per Reel (pcs)
SOT23-6	8	4	7"	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	03/02/2018	Initial Release	
1.0	03/02/2019	Production Release	

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