SY205232

Low Capacitance TVS Protection

General Description

SY205232 is a low-capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With a typical capacitance of 1.0pF, SY205232 is designed to protect against over-voltage and over-current transient events. It complies with IEC61000-4-2 (ESD) (±30kV air, ±30kV contact discharge), IEC61000-4-5 (surge) (12A, 8/20μs).

Each SY205232 device can protect one data line. The SY205232 is available in small DFN1.0mm×0.6mm or DFN0.6mm×0.3mm packages.

Features

- Protects One Data, Control, or Power Line
- For Operating Voltage of 3.3V and Below
- Low Capacitance: 1.0pF (Typical)
- Low Leakage Current: 0.1μA @ V_{RWM} (Typical)
- Low Clamping Voltage
- Transient Protection for High-Speed Data Lines
  - IEC 61000-4-2 (ESD) ±30kV (Air) ±30kV (Contact)
  - IEC 61000-4-5 (Surge) 12A (8/20 μs)
- Package Optimized for High-Speed Lines
- Ultra Small Packages:DFN0.6×0.3-2/DFN1.0×0.6-2
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge.

Applications

- USB 2.0
- Portable Electronics
- Desktops, Servers, and Notebooks
- Cellular Phones
- MP3 Ports
- Digital Camera Ports

Mechanical Characteristics

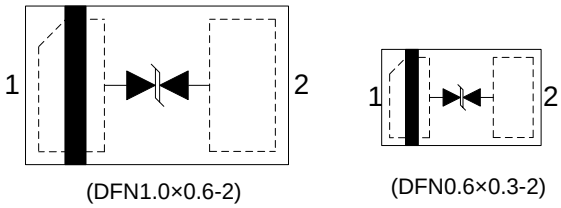
- Package: DFN0.6×0.3-2 or DFN1.0×0.6-2
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

Circuit Diagram

Ordering Information

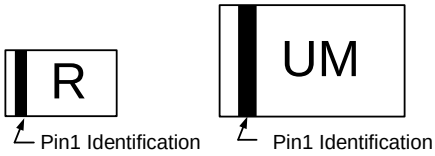
Part Number	Package Type	Top Mark
SY205232DXC	DFN0.6×0.3-2 RoHS Compliant and Halogen Free	R
SY205232DWC	DFN1.0×0.6-2 RoHS Compliant and Halogen Free	UM

Pinout (Top View)



(DFN1.0×0.6-2) (DFN0.6×0.3-2)

Marking Codes



Note 1: "R", "U" is device code, fixed.

Note 2: "M" is date code

Absolute Maximum Rating				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Peak Pulse Current (8/20μs)	I_{PP}		12	A
Peak Pulse Power (8/20μs)	P_{PK}		120	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	-30	30	kV
Operating Temperature	T_{OPT}	-40	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics T_A = 25°C						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Nominal Reverse Working Voltage	V_{RWM}		-3.3		3.3	V
Reverse Leakage Current @ V_{RWM}	I_R	V_{RWM} = 3.3V, T = 25°C		0.1	1.0	μA
Triggering Voltage @ I_{t1}	V_{t1}	I_{t1} = 1mA	3.65			V
Holding Voltage @ I_h	V_h	I_h = 100mA	3.65		5.6	V
Clamping Voltage @ I_{PP}	V_C (1)	I_{PP} = 12A, t_p = 8/20μs			10	V
Clamping Voltage @ I_{PP}	V_C (1)	I_{PP} = 16A, t_p = 10/100ns		7.5		V
Dynamic Resistance	R_{DYN} (1,2)	t_p = 10/100ns		0.15		Ω
Parasitic Capacitance	C_{ESD} (1)	V_R = 0V, f = 1MHz		1.0	3.0	pF

Note 1: Guaranteed by design and not subject to production test.

Note 2: R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns.

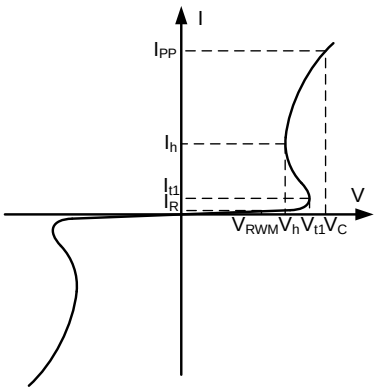
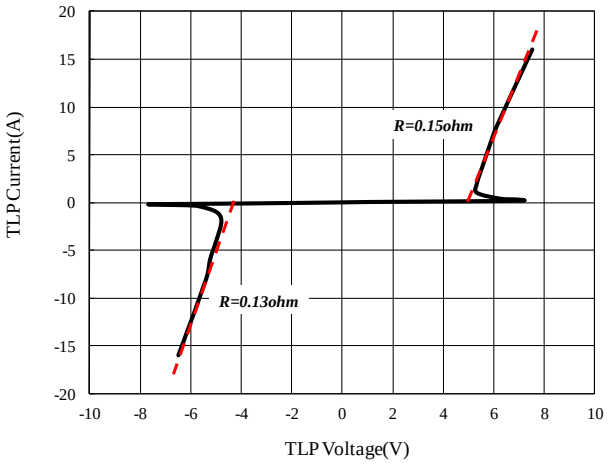


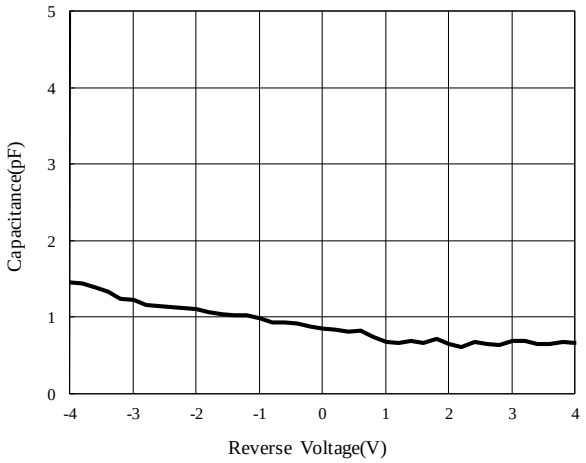
Figure 1. Bi-directional TVS

Typical Characteristics

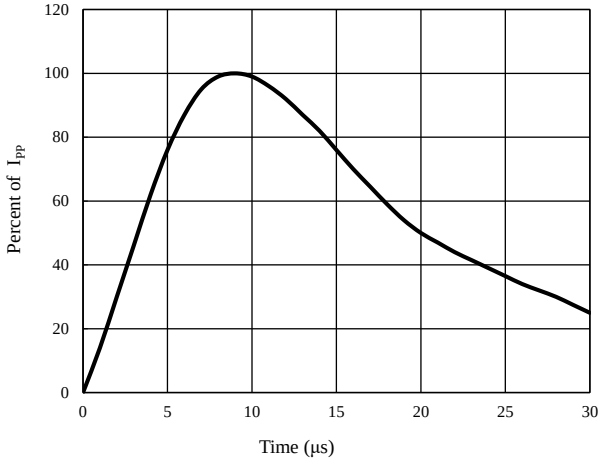
TLP Measurement



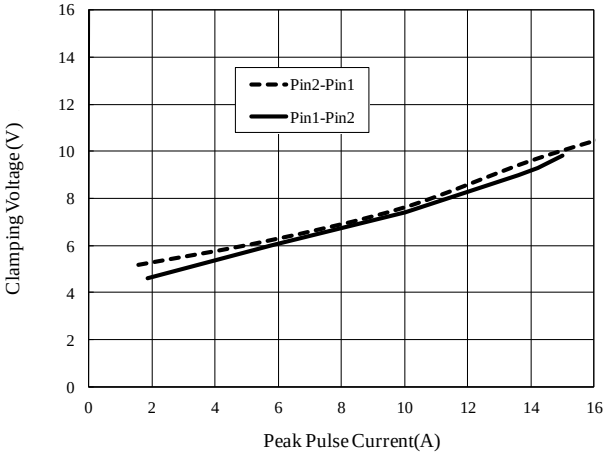
Capacitance vs. Voltage



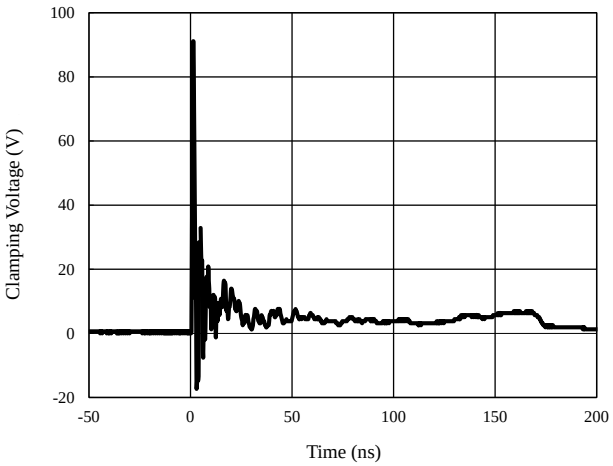
Pulse Waveform



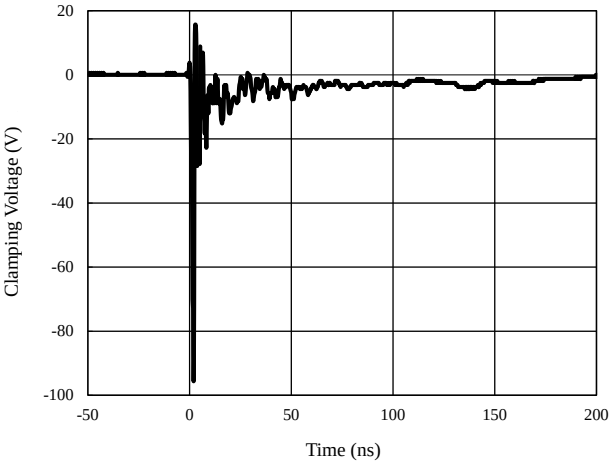
Clamping Voltage vs. Peak Pulse Current



ESD Clamping of I/O_1 to I/O_2 (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O_1 to I/O_2 (-8kV Contact per IEC 61000-4-2)



Application Information

The SY205232 protects one bidirectional data line against over-voltage and over-current transient events by clamping it to an acceptable reference.

The SY205232 pin connections are shown in Figure 2. The protected line is connected at Pin1 while Pin2 is connected to GND, which should connect to a ground plane on the board. All path lengths connected to pins of SY205232 should be as short as possible to minimize the parasitic inductance.

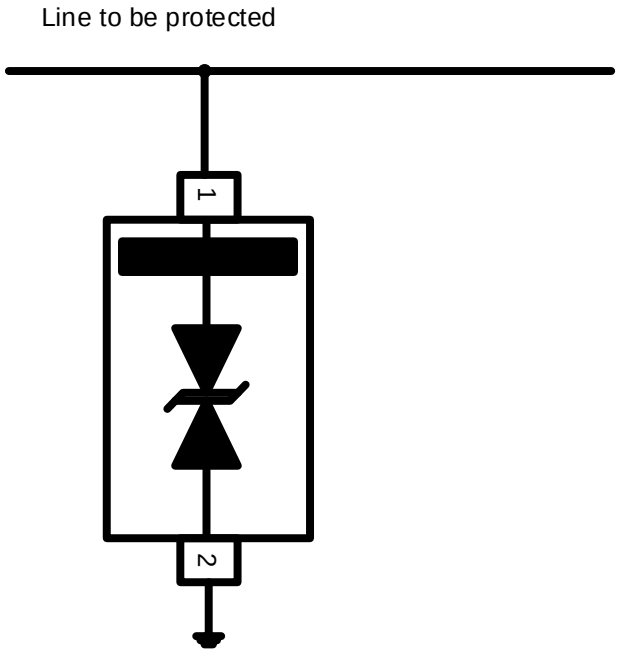


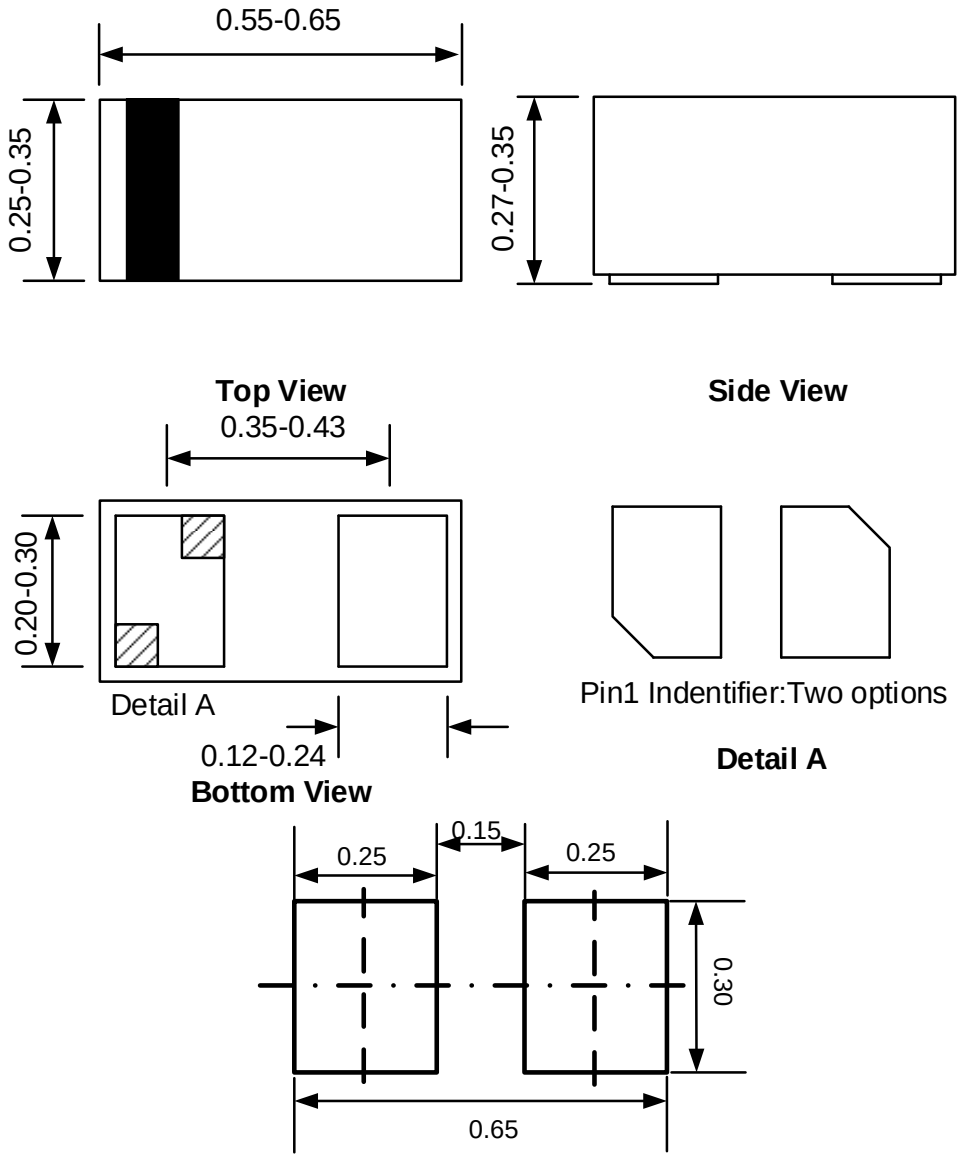
Figure 2. ESD/Surge Protection Circuit

PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following circuit board guidelines are recommended:

- Place SY205232 as close to the connector or terminal ports as possible.
- Use a large via to connect the SY205232 pin to the ground.
- Avoid running signals near board edges.
- The SY205232 should be placed near the protected line.
- The distance between the SY205232 ground pin and the GND reference path should be as short as possible.

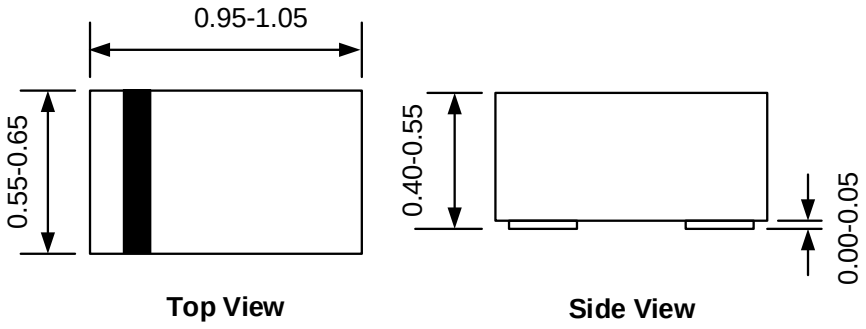
DFN0.6×0.3-2 Package Outline



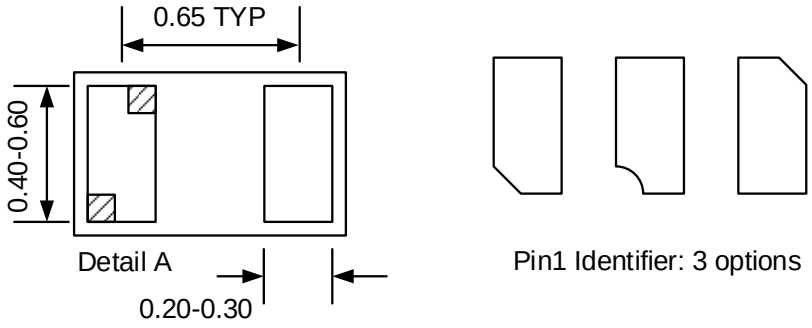
Recommended PCB Layout
(Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

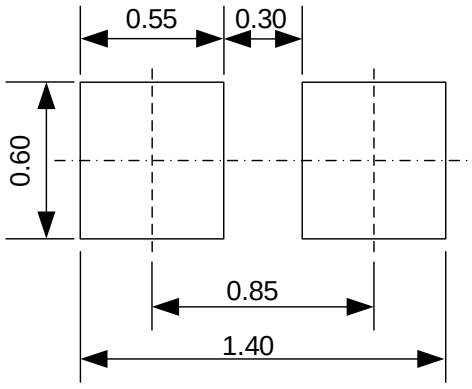
DFN1.0×0.6-2 Package Outline



Top View **Side View**



Bottom View **Detail A**

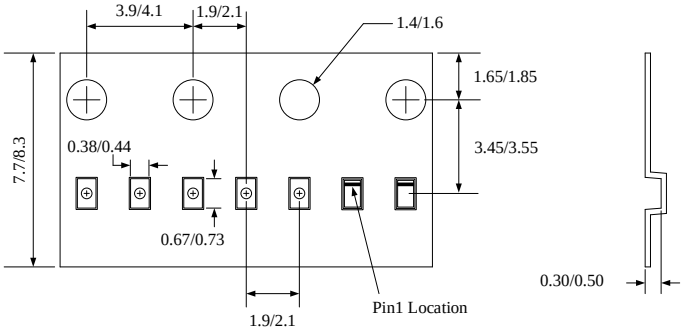


Recommended PCB Layout
(Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Tape and Reel Specification

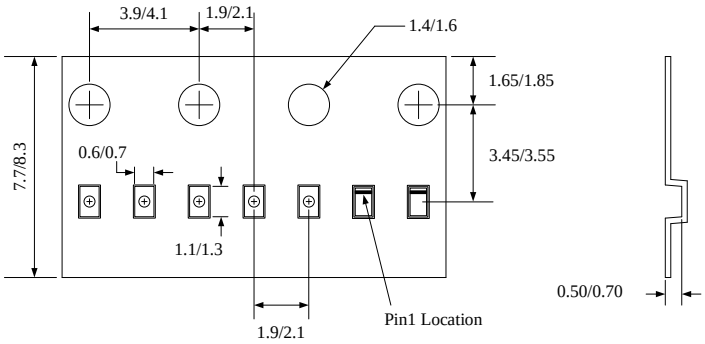
DFN0.6×0.3-2 Taping Orientation



Dimensions In mm

Feeding direction ⟶

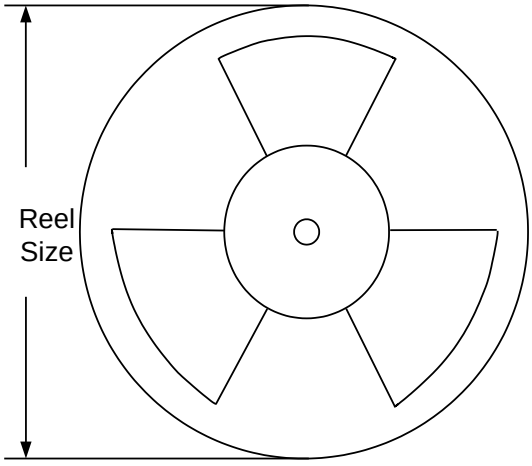
DFN1.0×0.6-2 Taping Orientation



Dimensions In mm

Feeding direction ⟶

Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer * Length(mm)	Leader * Length (mm)	Qty per Reel (pcs)
DFN0.6×0.3-2	8	2	7"	400	400	10000
DFN1.0×0.6-2	8	2	7"	400	400	10000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	08/01/2019	Initial Release	
1.0	08/01/2020	Production Release	
1.0A	01/26/2024	Update POD& Tap Reel	6,7,8

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