SY20753

Wide Input, High Current, Bi-directional Regulator for Single Cell Li-Ion Battery Power Bank Application

General Description

SY20753 is a 4.0-13.5VIN bi-directional regulator for Li-Ion battery power bank application. Advanced bi-directional energy flow control with automatic input power source detection is adopted to achieve battery charging mode and battery power supply mode alternately. If the external power supply is present, SY20753 will run in battery charging mode with fully protection function; if the external power supply is absent, SY20753 will run in battery power supply mode with output current capability up to 2.25A at 12V or 4.5A at 5V in OUTFB mode.

SY20753 has an integrated reverse blocking switch to prevent current leaking from the system side or battery side to the input side and an integrated linear switch to achieve over voltage/current protection at the system side. A half bridge with quasi-fixed 0.5MHz switching frequency is integrated to achieve power conversion for battery charging mode and battery power supply mode. All of them adopt N-channel MOSFET with 16V rating and extremely low R_{DSON} to optimize operation efficiency and extend battery lifetime.

SY20753 is available in QFN4x4 package to minimize the PCB layout size for wide portable applications.

Ordering Information

SY20753 □(□,□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20753QYC	QFN4x4-20	

Features

- Integrated N-Channel MOSFETs with 16V Voltage Rating and Extremely Low R_{DSON}
- High Switching Frequency to Minimize Peripheral Circuit Design
- Trickle Current / Constant Current / Constant Voltage Charging Mode
- Maximum 5A Battery Charging Current
- Maximum 4.5A/5V or 2.25A/12V System Current in Battery Power Supply Mode
- USB Port Identifier for Various Input Current Limit
- Automatic Input Power Source Detection
- I^2C controls
  - Programmable Battery Charge Voltage
  - Programmable Constant Current Charging
  - Programmable Over Current Limit for SYS load
  - Programmable Input Current DPM
  - Programmable Input Voltage DPM
  - Programmable Battery Charging Timeout
- Charging Shutdown Control
- Charging Mode CV Tolerance +/-0.5%
- DO+/DO- Divider Mode Compliant
- DO+/DO- QC3.0 Compliant
- OUTPUT MTK PE Compliant
- Host Enable Control for Standby Mode in Supply Mode
- Over Temperature Protection
- Battery UTP/OTP in Charging Mode and Supply Mode
- Charge Status Indication
- Light load Status Indication

Applications

- Single Cell Li-Ion Power Bank
- Portable Device with 1-cell Battery Pack

Typical Applications

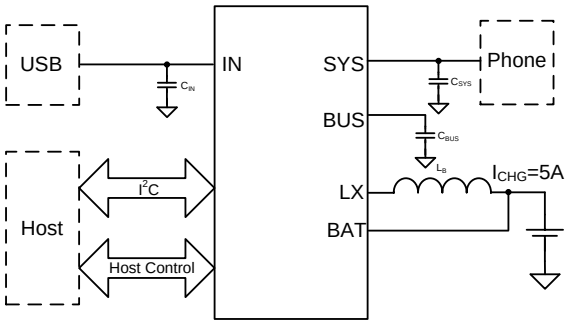
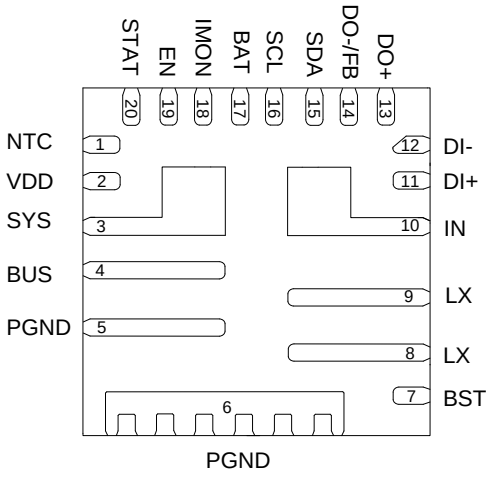


Figure1. Simplified Schematic

Pinout (Top view)



(QFN4x4-20)

Top Mark: BSU*xyz* (device code: **BSU**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Description
NTC	1	Thermal protection and battery detection pin. In charging mode, UTP threshold is about 65% of VDD and OTP threshold is about 35% of VDD. In discharging mode, UTP threshold is about 81% of VDD and OTP threshold is about 30% of VDD.
VDD	2	Internal linear regulator output. VDD is the output of 3.3V linear regulator. Connect a 1μF ceramic capacitor from VDD to GND.
SYS	3	System load pin. Connect a MLCC from this pin to ground to decouple the high frequency noise.
BUS	4	Connection point for reverse blocking FET and bypass linear switch. Connect a MLCC from this pin to ground to decouple the high frequency noise.
PGND	5,6	Power ground pin.
BST	7	Boot strap pin. Connect a MLCC from this pin to LX.
LX	8,9	Switch node pin. Connect an external inductor from this pin to BAT pin.
IN	10	Positive power supply input pin. V_{IN} ranges from 4V to 13.5V for normal operation and up to 16V surge. Connect a MLCC from this pin to ground to decouple high frequency noise.
DI+	11	Host USB D+ connection. For USB input identification.
DI-	12	Host USB D- connection. For USB input identification.
DO+	13	USB D+ for system connection. Support Divider mode and BC1.2 handshake.
DO-/FB	14	When FB_EN is 0: USB D- for system connection. Support Divider mode and BC1.2 handshake. When FB_EN is 1: SYS voltage feedback pin. Program the external resistor divider to program the SYS voltage. $V_{SYS}=1\times(1+R_{FB1}/R_{FB2})$, refer to “SYS Voltage Set” in general function description.
SDA	15	I^2C Interface data.
SCL	16	I^2C Interface clock.
BAT	17	Battery positive pin. Also connect it to inductor terminal.
IMON	18	Buffered current pin. In Buck mode, IMON outputs the input current of Buck converter. In Boost mode, IMON outputs the current of LNFET. $V_{IMON}=I\times R_{IMON}/80k$

EN	19	Whole chip enable pin. When V_{IN} is absent, if it is high, it will enable the IC, or else, it will shut down the IC. When V_{IN} is present, the chip will always be enabled.
STAT	20	Charging status indication pin. It is an open-drain output pin and can be used to turn on a LED to indicate the charge in process. When the charge is done, the LED will be off. STAT pin will be pulled low for 200μs to generate an INT when DI+, DI-, DO+, DO- pins handshake is done.

Absolute Maximum Ratings (Note 1)

IN, STAT, LX, BUS, SYS, EN ---------- -0.5~18V
BAT, SCL, SDA, DI+, DI-, DO+, DO-/FB ---------- -0.5~ 6V
VDD, NTC, IMON ---------- -0.5~ 4V
BST-LX ---------- -0.5~4V
Power Dissipation, P_D @ T_A = 25°C, ---------- 2.5 W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 30 °C/W
θ_{JC} ---------- 15 °C/W
Junction Temperature Range ---------- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 125°C

Recommended Operating Conditions (Note 3)

IN, STAT, LX, BUS, SYS, EN ---------- less than 16V
BAT, SCL, SDA, DI+, DI-, DO+, DO-/FB ---------- -0.3~5.5V
VDD, NTC, IMON ----------0~3.6V
BST-LX ----------0~3.6V
Junction Temperature Range ---------- -20°C to 100°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

T_A=25°C, T_A=T_J, V_{IN}=5V, GND=0V, C_{IN}=20μF, L_B=2.2μH, R_{IMON}=20kΩ, C_{BAT}=20μF, C_{BUS}=40μF, C_{SYS}=10μF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Current						
Battery Leakage Current	I_{BAT}	EN pull down		5	10	μA
Input Quiescent Current	I_{IN}	NTC=0V		1.2		mA
Boost Null-load Battery Discharge Current	I_{BOOST}	V_{BAT}=4.35V,V_{SYS}=5V, I_{SYS}=0V, converter switching		2		mA
Input Power Supply						
Input Voltage UVLO Threshold	V_{INUVLO}			3.9		V
Input Voltage UVLO Hysteresis	V_{UVHYS}	Falling edge		200		mV
Input Voltage OVP Threshold in 5V Mode	V_{INOVP_5V}	Rising edge	5.7			V
Input Voltage OVP Hysteresis in 5V Mode	$V_{INOVPHYS\_5V}$	Falling edge		0.25		V
Input Voltage OVP Threshold in 12V Mode	V_{INOVP_12V}	Rising edge	12.9			V
Input Voltage OVP Hysteresis in 12V Mode	$V_{INOVPHYS\_12V}$	Falling edge		0.5		V
LDO Output						
VDD Voltage	V_{VDD}	V_{BUS}=5V		3.3		V
VDD Source Current	I_{VDD}	V_{VDD}=2.8V	70		210	mA
Linear FET						
$R_{DS(ON)}$ of the Linear NFET	R_{LNFT}			20		mΩ
System Current Limit Tolerance	I_{SYSMAX}	V_{SYS}=4.5V, V_{BAT}=3.5V, I_{SYS_LIMIT}=1A	-10		10	%
System Clamp Voltage Tolerance	V_{SYSMAX}	LV		5.8		V
		HV		13		V
Blocking FET						
$R_{DS(ON)}$ of Reverse Blocking NFET	R_{BKFT}			25		mΩ
Half-bridge in Buck Mode						
Voltage and Current Bias						
BUS Supply Voltage for Battery Charging	V_{BUS}		4.5		13.5	V
BUS Voltage OVP Threshold in LV Mode	$V_{BOVP\_LV\_BK}$	Rising edge	7.5			V
BUS Voltage OVP Hysteresis in LV Mode	$V_{BOVPHYS\_LV\_BK}$	Falling edge		0.5		V
BUS Voltage OVP Threshold in HV Mode	$V_{BOVP\_HV\_BK}$	Rising edge	13.5			V
BUS Voltage OVP Hysteresis in HV Mode	$V_{BOVPHYS\_HV\_BK}$	Falling edge		1		V

Switching Frequency						
Buck Switching frequency	f_{SWBK}			0.5		MHz
Min on Time for Charging Mode, HS FET	$T_{ONMINHS}$			100		ns
Max on Time for Charging Mode, HS FET	$T_{ONMAXHS}$	In low dropout mode		7		µs
Battery Charging						
Battery CV Voltage Tolerance	V_{CV}	Voltage on BAT pin	-0.5		0.5	%
Battery Voltage Threshold Hysteresis for Recharge	ΔV_{RCH}	Falling edge		100		mV
Battery Trickle Charging Mode Voltage Threshold	V_{TRK}	Rising edge	2.7	2.8	2.9	V
Charging Current Accuracy for Constant Current Mode	I_{CC}	REG03[2:0]=101, Icc=3A,V_{IN}=5V,V_{BAT}=3.5V	-20		10	%
		Reg03[2:0]=111, Icc=5A,V_{IN}=5V,V_{BAT}=3.5V	-20		10	%
Charging Current Accuracy for Trickle Current Mode		REG 03[2:0]=101, I_{TC}=300mA		10%		I_{CC}
		REG 03[2:0]=111, I_{TC}=500mA		10%		I_{CC}
Termination Current Tolerance	I_{TERM}	REG 03[2:0]=101 , I_{TERM}=150mA	-50		40	%
		REG 03[2:0]=111 , I_{TERM}=250mA	-40		30	%
Battery Voltage OVP Threshold	V_{BTOVP}		105 %	110 %	115 %	VCV
Battery Short Circuit Protection						
Battery Short Circuit Protection Threshold	$V_{SHORTBT}$			2		V
Dynamic Input Power Management						
Input Current Limit Tolerance	I_{DPM}	REG 02[7:5]=011, I_{DPM}=1.5A	-10		+10	%
Input Voltage Regulation During Input Voltage Dynamic Power Management	V_{DPM}	REG 03[7:5]=100,LV mode	-2.5		1.5	%
		REG 03[7:5]=100,HV mode	-3		1.5	%
USB Port Identification and Current Limit Reference (Proposal 1)						
SDP Input Current Limit	I_{SDP}	I_{DPM}=0.5A	-15		+15	%
DCP Input Current Limit	I_{DCP}	I_{DPM}=1.5A	-10		+10	%
Half-bridge in Boost Mode						
Voltage and Current Bias						
Battery Depletion Voltage Tolerance	V_{BATDEP}	Falling edge	2.5	2.6	2.7	V
Battery Depletion Voltage	$V_{BATDEPHYS}$	Rising edge		0.28		V

BUS Voltage OVP Threshold In LV Mode	$V_{BOVPHYS\_LV\_BT}$	Rising edge	7.5			V
BUS Voltage OVP Hysteresis in LV Mode	$V_{BOVPHYS\_LV\_BT}$	Falling edge		0.5		V
BUS Voltage OVP Threshold In HV Mode	$V_{BOVP\_HV\_BT}$	Rising edge	13.5			V
BUS Voltage OVP Hysteresis in HV Mode	$V_{BOVPHYS\_HV\_BT}$	Falling edge		1		V
SYS Voltage Tolerance	V_{SYS}		-2.5		2	%
Feedback Reference of SYS Voltage	V_{SYS_FB}		0.985	1	1.015	V
OTG Light Load Threshold	I_{SYS_LOW}	REG01[4]=1,I_{SYS_LOW}=50mA,falling edge	15	50	75	mA
		REG01[4]=0,I_{SYS_LOW}=100mA,falling edge	75	100	125	mA
Boost Mode Max Peak Current Tolerance	$I_{PEAK\_MAX\_BT}$	REG02[1:0]=11, $I_{PEAK\_MAX\_BT}$=12A	-22		18	%
Switching Frequency						
Boost Switching Frequency	f_{SWBST}			0.5		MHz
Min on Time for Discharging Mode, LS FET	T_{ONMINL}			200		ns
Other General Parameters						
Battery Thermal Protection NTC						
Battery Removed	Battery Detection	Rising edge	87%			
Under Temperature Protection	UTP_CHG	Rising edge, charging mode	63%	65%	67%	
Under Temperature Protection Hysteresis		Falling edge, charging mode		5%		
Over Temperature Protection	OTP_CHG	Falling edge, charging mode	33%	35%	37%	
Over Temperature Protection Hysteresis		Rising edge, charging mode		2%		
Under Temperature Protection	UTP_DCHG	Rising edge, discharging mode	79%	81%	83%	
Under Temperature Protection Hysteresis		Falling edge, discharging mode		5%		
Over Temperature Protection	OTP_DCHG	Falling edge, discharging mode	28%	30%	32%	
Over Temperature Protection Hysteresis		Rising edge, discharging mode		2%		
Power MOSFET						
$R_{DS(ON)}$ of High-side NFET	R_{HSFT}			10		mΩ
$R_{DS(ON)}$ of Low-side NFET	R_{LSFT}			5		mΩ
Logic Level and Timing						
EN,SCL,SDA Low Level Threshold	V_{LOW}				0.4	V
EN,SCL,SDA Low Level Threshold	V_{HIGH}		1.3			V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

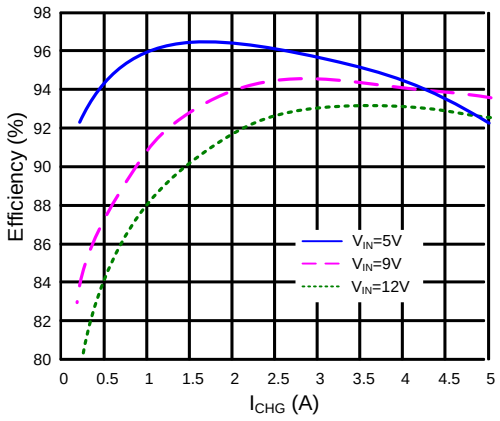
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

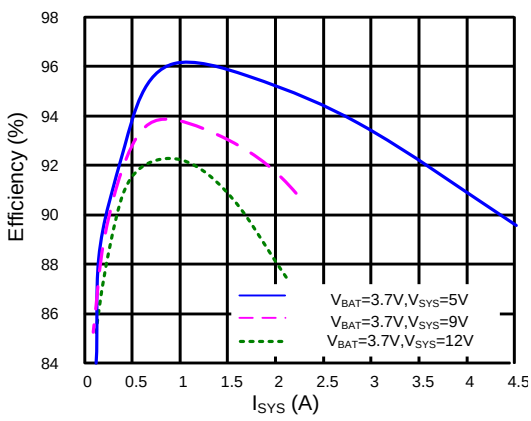
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V, unless otherwise specified.)

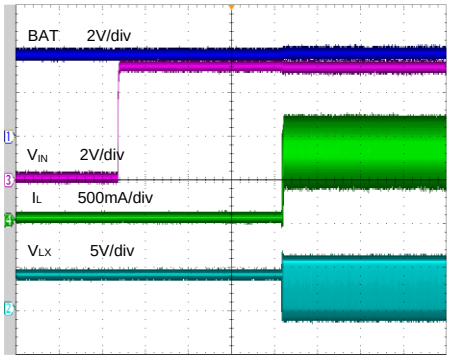
Efficiency vs. Charging Current (CV Mode)



Efficiency vs. I_{SYS} (Boost Mode, BAT=3.7V)

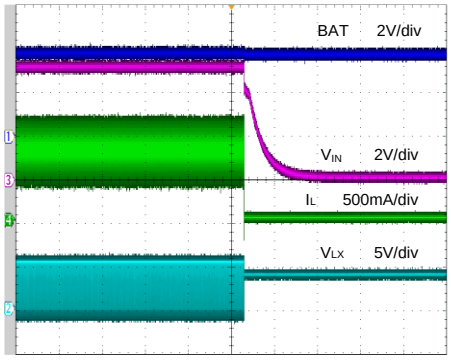


5V V_{IN} Power ON(Adapter)



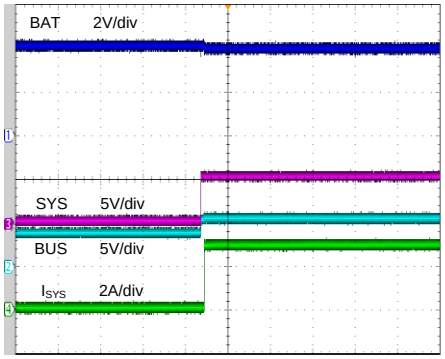
Time (200ms/div)

5V V_{IN} Power OFF(Adapter)



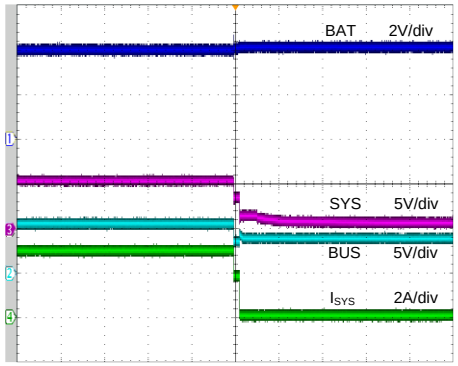
Time (200ms/div)

5V Boost Mode OTG ON by I^2C



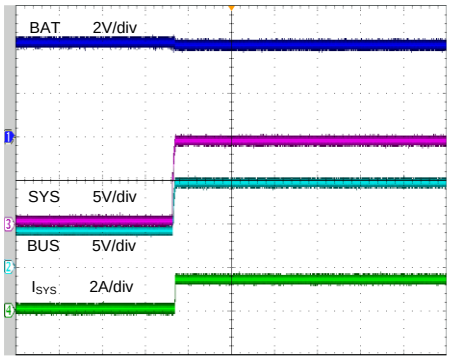
Time (200ms/div)

5V Boost Mode OTG OFF by I^2C



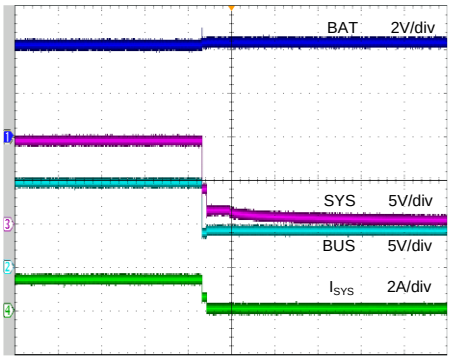
Time (200ms/div)

9V Boost Mode OTG ON by I^2C



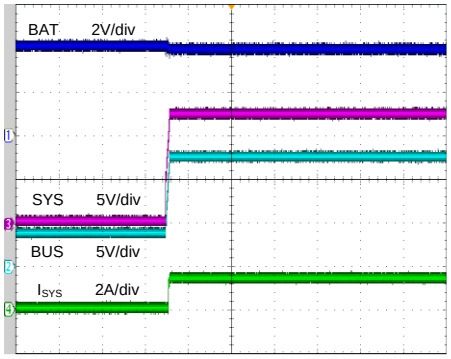
Time (200ms/div)

9V Boost Mode OTG OFF by I^2C



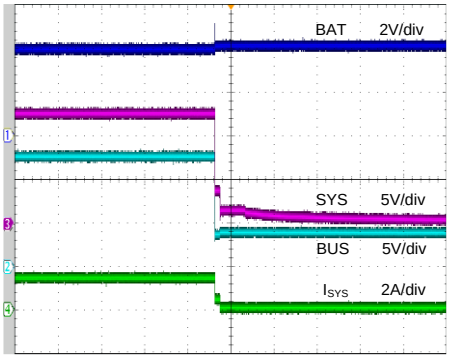
Time (200ms/div)

12V Boost Mode OTG ON by I^2C



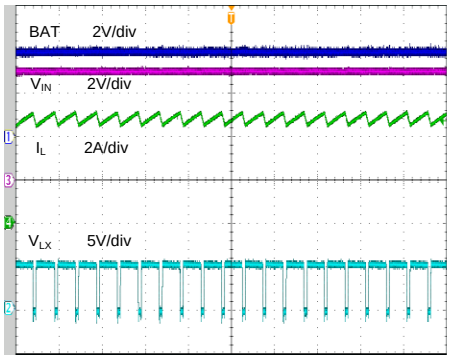
Time (200ms/div)

12V Boost Mode OTG OFF by I^2C



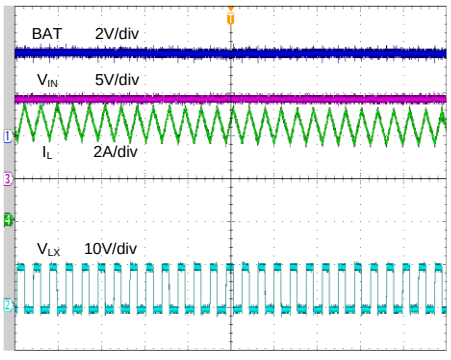
Time (200ms/div)

5V Buck Steady State



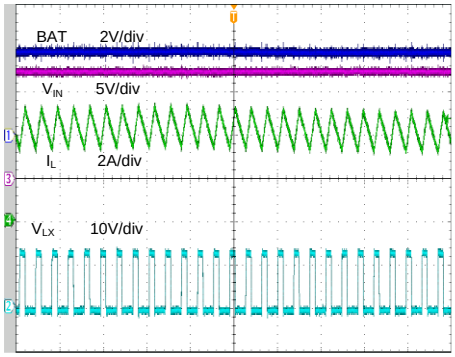
Time (4μs/div)

9V Buck Steady State



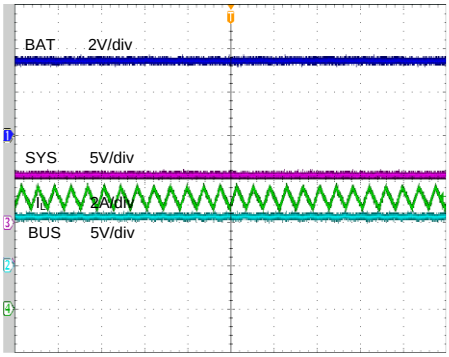
Time (4μs/div)

12V Buck Steady State



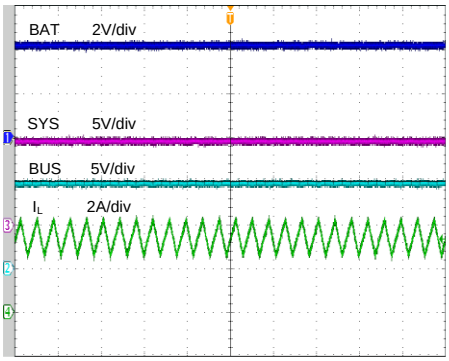
Time (4μs/div)

5V Boost Steady State



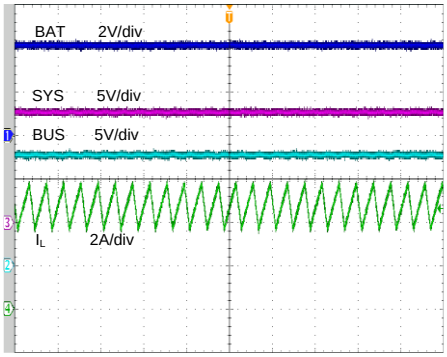
Time (4μs/div)

9V Boost Steady State



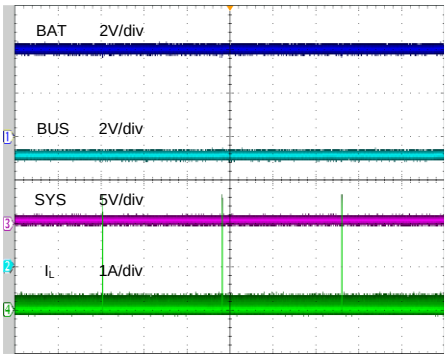
Time (4μs/div)

12V Boost Steady State



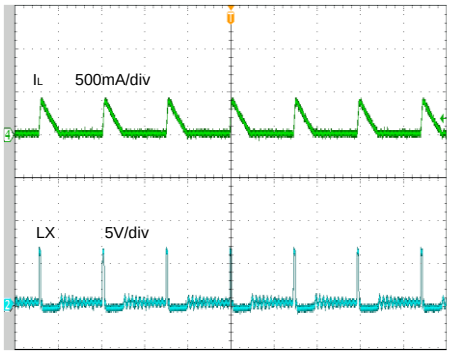
Time (4μs/div)

Boost SYS Short



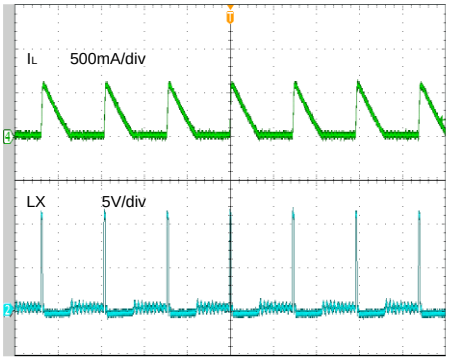
Time (200ms/div)

Battery Short in 5V Charging Mode



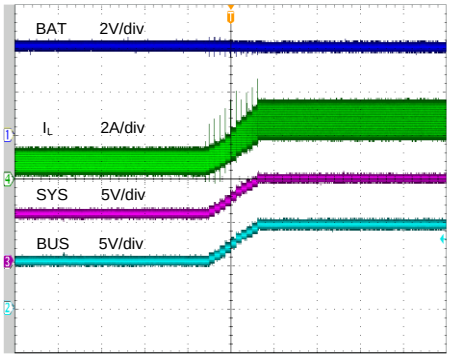
Time (4μs/div)

Battery Short in 12V Charging Mode



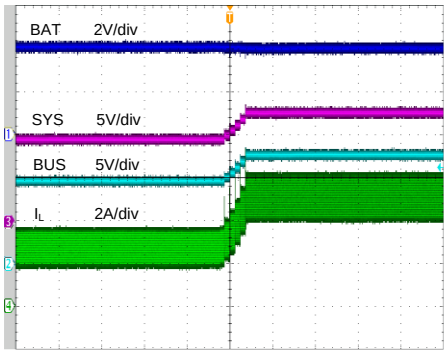
Time (4μs/div)

Boost 5V to 9V



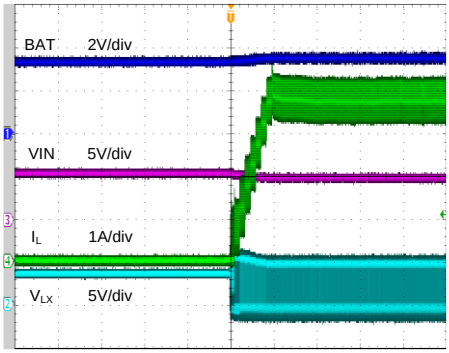
Time (10ms/div)

Boost 9V to 12V



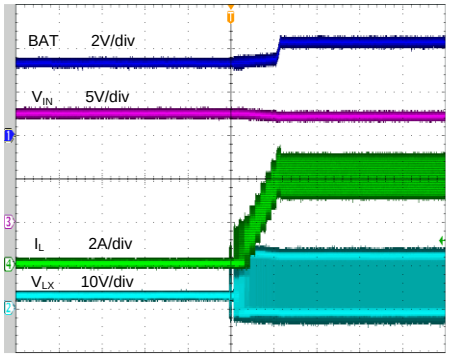
Time (10ms/div)

Inductor Current Soft Start
in 5V Charging Mode



Time (10ms/div)

Inductor Current Soft Start
in 12V Charging Mode



Time (10ms/div)

Detailed Description

SY20753 is a highly integrated 5A switch mode charger for single cell Li-Ion and Li-polymer battery. When input source is absent, it can automatically switch to discharging mode to supply power to SYS from the battery. It is highly integrated with reverse-blocking FET(RBFET), linear FET(LNFET), high-side switching FET(HSFET), low-side switching FET(LSFET).

1 Functional Block Diagram

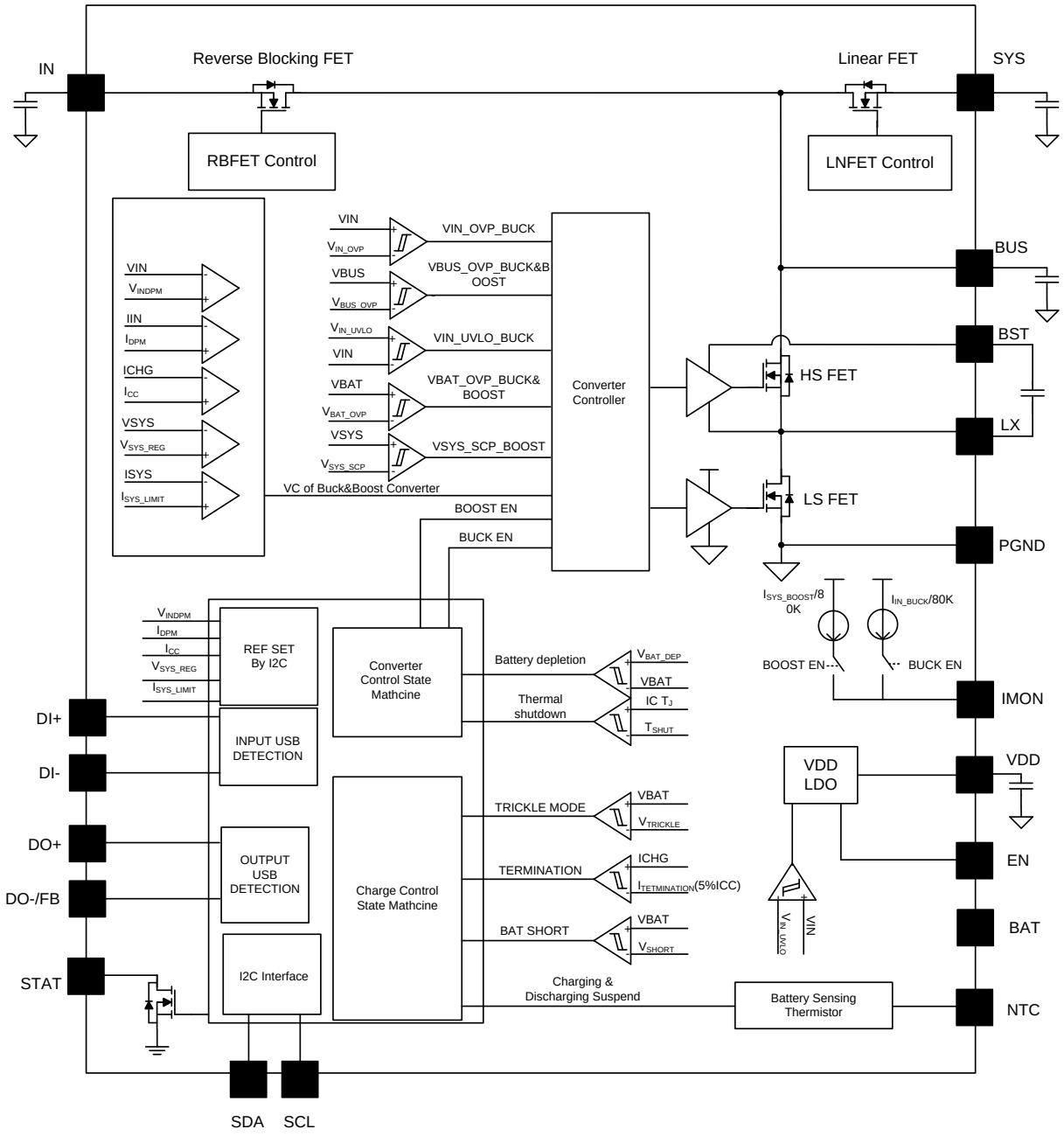


Figure2. Functional Block Diagram

General Function Description

Device Power-on-reset (POR)

The internal bias circuits are powered from the higher voltage of V_{BUS} and V_{BAT}. When V_{IN} rises above V_{IN_UVLO} or BAT rises above V_{BAT_DEP} and EN is high, the IC will be active, VDD LDO will be powered on. I^2C interface will be ready for communication and all the registers will be reset to default value. The host can access all the registers after POR.

Device Power Up from Battery without Input Source

Only if battery is present and the voltage is above depletion threshold (V_{BAT_DEP}), VDD LDO will stay off until EN is high. When EN is low, the IC will be shut down to save power. The Boost converter will turn on if both EN is high and OTG_Enable(REG01[5]) is set to 1. SY20753 always monitors the SYS voltage and the current of LNFET. When V_{SYS} is lower than $V_{SHORTSYS}$, the linear FET will modulate the current to be saw tooth shape from 0A to 1.7A for short circuit protection recovery. SY20753 tries recovery for 5ms per 0.7s when SYS is shorted. When the current of LNFET exceeds the SYS current limit (set by REG02[4:2]), the Boost converter will decrease the duty cycle to limit the output current of Boost converter.

Device Power Up from Input Source

When an input source is plugged in, the device will check the input source voltage to turn on VDD LDO and all the bias circuits. It detects and sets the input current limit before the Buck converter is started.

The power up sequence from input source is as listed:

1. Power Up VDD LDO

2. Automatic Input Power Supply Detection

3. Input Source Type Detection based on D+/D- to set default Input Current Limit (IDPM) register and input source type

4. Input Voltage Dynamic Power Management set (VINDPM set)

5. Converter Power-up

Power Up VDD Regulation (LDO)

The VDD LDO supplies internal bias circuits as well as the HSFET and LSFET gate drivers. The LDO also provides bias rail to NTC external resistors. The pull-up rail of STAT can be connected to VDD as well. The VDD will be enabled when V_{IN} is above V_{IN_UVLO}.

Automatic Input Power Supply Detection

After VDD LDO powers up, SY20753 will adopt an internal current source with 10mA maximum capability to discharge the IN pins for 100ms. When a good input source is present, V_{IN} should keep being higher than V_{IN_UVLO} even after 100ms discharging.
Once the input source passes the automatic input power supply detection, V_{IN}_PRES (REG00[0]) will be set to 1 and the STAT pin generate an INT to host.

Input Source Type Detection

After the V_{IN}_PRES bit is set to 1, the charger device will run input source type detection.

SY20753 follows the USB battery charging specification 1.2 (BC1.2) to detect input source (SDP/CDP/DCP) and non-standard adapter through USB DI+/DI- lines. In addition, when USB DCP is detected, it can do adjustable high voltage adapter handshake by setting and monitoring the voltage of DI+/DI- through I^2C.

After input source type detection, the following registers are changed:

1. Input current limit (IDPM) register is changed to set current limit.

2. Upstream_USB_type bit is updated to indicate the input source USB type.

The host can over-write IDPM register to change the input current limit if needed.

Input Voltage Dynamic Power Management Set

SY20753 sets the VDPM to (1-8%) $\times$ V_{IN_SET}(Set by REG07[7:6]) after input source power up. The percentage can be changed by VDPM (REG03[7:5]).

Converter Power-up

After the VDPM is set, the converter will be enabled and the HSFET and LSFET will start switching.

As a battery charger, the device deploys a highly efficient 0.5MHz step-down switching regulator. The constant-off peak current converter keeps tight control of input voltage, input current, battery voltage, charge current, which simplifies output filter design.

An internal compensation network allows using ceramic capacitors at the output of the converter. The peak current of IL sensed by HSFET is compared to the internal error control signal to vary the duty cycle of the converter. The cycle-by-cycle current limit is implemented due to the peak current control mode.

Boost Mode Operation

SY20753 supports Boost converter operation to deliver power from the battery to other portable devices through SYS pin. The Boost mode output current rating supports maximum output current up to 4.5 A to charge smart phone and tablet.

In Boost mode, SY20753 deploys a 300kHz or 500kHz peak current mode step up converter to deliver power from battery to SYS. The Boost mode state can be monitored by reading the Boost bit (REG00[6]).

Supply Mode

When input is absent, SY20753 will deliver power to SYS from battery and it will work as a Boost converter. Supply mode can be enabled if all the following conditions are valid:

1. Input source is absent.
2. V_{BAT} is higher than $V_{BAT\_DEP.}$
3. OTG is enabled (OTG_Enable bit is 1).
4. EN is high.

Battery Charging Management

SY20753 charges 1-cell Li-Ion by deploying a step down converter with 5A capability. The integrated NMOS with extremely low R_{DSON} optimizes the efficiency.

Charging Mode Enable Control

The charger can be enabled or disabled by Charge_Enable bit(REG01[7]).

Programmable Input Current Dynamic Power Management

When input current reaches I_{DPM}, it will be limited to IDPM by regulating the duty cycle of the Buck converter. The IDPM loop takes control of the Buck converter until the input current decreases under I_{DPM}. The input current limit is programmed by IDPM bit(REG02[7:5]).

Programmable Input Voltage Dynamic Power Management

When input voltage drops to VDPM, the input voltage is limited to VDPM by regulating the duty of Buck convertor. The VDPM loop takes control of the Buck converter until the input voltage rises above V_{DPM}.
The input voltage limit is programmed by VDPM bit(REG03[7:5]).
The VDPM state is monitored by SY20753 and is recorded in REG00[1]. The host can read the VDPM_STATE bit (REG00[1]) to monitor whether VDPM loop works.

Programmable Charging Current

The max charging current of SY20753 is limited to I_{CC}(set by Charge_Current bit), when the charging current exceeds I_{CC}, charging current will be limited to I_{CC} by regulating the duty cycle of Buck converter. The constant current loop takes control of Buck converter.

Charging current is programmed by Charge_Current bit (REG03[2:0]).

Programmable Termination Current

A charging cycle is terminated while battery voltage is above the recharging threshold and charging current is lower than termination current. After termination, only when battery voltage drops below recharging threshold, SY20753 can exit termination state.

Termination current is set to 5% of I_{CC} internally.

Programmable Charging Voltage

The max charging voltage is limited by SY20753 to prevent the over-charging to Li-Ion. When the battery voltage reaches max charging voltage, the battery voltage will be limited to V_{CV}(set by Charge_Voltage bit) by regulating the duty cycle of Buck converter. The charging voltage loop takes control of Buck converter until battery voltage drops below V_{CV}.

Charging voltage is programmed by Charing_Voltage bit(REG03[4:3]).

Charging Status Indication Description

1. Charging-in-process – Pull and keep STAT pin low;
2. Charging Done – Pull and keep STAT pin to High;
3. Fault Mode – Output high and low voltage alternatively at 10Hz frequency, fault mode includes VIN OVP, BAT OVP, BAT SCP, BAT UTP/OTP, charging time out.

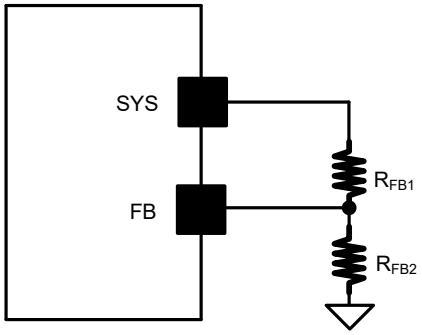
Connect a LED from VDD to STAT pin, LED ON indicates charging-in-process, LED OFF indicates charging done, LED flash indicates fault mode. Charging status is recorded in REG00[5:4]

SYS Output Management

SYS Voltage Set

In supply mode, the Boost converter modulates the SYS voltage according to the handshake of DO+/DO- or Downstream_Voltage_Set bit(REG05[4:2]).The Boost converter works in CV mode until the SYS current exceeds the SYS Current Limit.
When Downstream_OUT_SEL is 1, SYS voltage is set by Downstream_Voltage_Set bit(REG05[4:2]). When

Downstream_OUT_SEL is 0, SYS voltage is set by DO+/DO-.
When FB_EN is set to 1, SYS voltage is set by external resister. V_{SYS}=1× (1+R_{FB1}/R_{FB2}).



SYS Current Limit

In supply mode, once SYS current exceeds I_{SYS_Limit}, SYS current will be limited to I_{SYS_Limit} by regulating the duty cycle of Boost converter. The SYS current limit loop takes control of Boost converter until the SYS current decreases under I_{SYS_Limit}.
SYS current limit is programmed by I_{SYS_Limit} bit(REG02[4:2]).

The Monitor of Current

The host can monitor the current of SY20753 by measuring the voltage of IMON.

In Buck mode, IMON outputs the input current of Buck converter. In Boost mode, IMON outputs the current of LNFET. The max voltage of IMON must be lower than 2V, the proper R_{IMON} can be derived from the following formula:

V_{IMON}=I×R_{IMON}/80k

Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 200μs INT pulse.

- After "Input Source Type Detection", and V_{IN}_PRES is set to 1.
- Upstream BC1.2 detection is done.
- DO+ DO- detection is done.
- The request voltage of DO+ DO- changed.

After INT is inserted, the MCU must read I^2C to clear the INT, otherwise an INT will be sent every 800ms.

Protection Description

Thermal Protection-Thermal protection for battery is achieved through NTC pin in charging and discharging mode. The basic scheme is shown in application information. Thermal shutdown is active for the device itself. The IC will return to normal work when the temperature returns into normal range again. Charging timer will stop and maintain the result during thermal protection.

Short Circuit Protection- There are BAT short circuit protection and SYS short circuit protection in SY20753. When V_{SYS} is lower than $V_{SHORTSYS}$, the linear FET will modulate the current to be saw tooth shape from 0A to 1.7A for short circuit protection recovery. SY20753 tries recovery for 5ms per 0.7s. In charging mode, once V_{BAT} is lower than $V_{SHORTBT}$, the switching frequency will be folded back to 20% of the default value.

Over Voltage Protection- When V_{BUS} or V_{BAT} is higher than the over voltage protection threshold, the half bridge will stop Boost operation or Buck operation immediately. It will return to normal work when the monitored voltage returns to normal level. Input voltage has UVLO and OVP, which would make the device shut down, SY20753 will return to normal work when the V_{IN} returns to normal range.

Battery Over Discharge Protection
In Supply mode, once battery voltage is lower than V_{BAT_DEP}, SY20753 will turn off Boost and LNFET.

Timeout Protection-Programmable timeout protection for the trickle current charge mode and the constant current and CV charge mode both. Time out time is set by REG01[2:1]. Once timeout, the device will stop the charge operation and latch off. Only re-plug in power source can reset the latch logic and restart the normal charging.

Applications Information

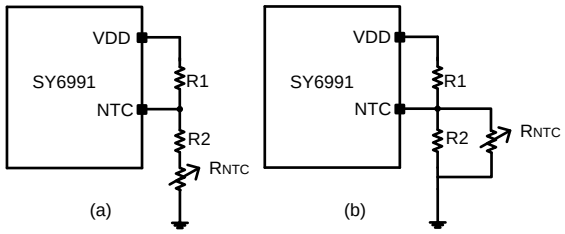
Applications Information

Because of the high integration of SY20753, the application circuit based on this regulator is rather simple. Only input capacitor C_{IN}, BUS capacitor C_{BUS}, battery capacitor C_{BAT}, inductor L, NTC resistors R1, R2, need to be selected for the targeted applications specifications.

NTC Resistor:

SY20753 monitors battery temperature by measuring the VDD voltage and NTC voltage. The controller will trigger the UTP or OTP when the rate K (K= V_{NTC}/V_{VDD}) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.

Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps of figure (a) are:

1. Define K_{UT}, K_{UT} =65%
2. Define K_{OT}, K_{OT} =35%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2

$$R2 = \frac{K_{OT}(1-K_{UT})R_{UT} - K_{UT}(1-K_{OT})R_{OT}}{K_{UT} - K_{OT}}$$

5. Calculate R1

$$R1 = (1/K_{OT} - 1)(R2 + R_{OT})$$

If choose the typical values K_{UT} =65% and K_{OT}=35%, then

$$R2 = 0.408\,R_{UT} - 1.408\,R_{OT}$$
$$R1 = 1.857(R2 + R_{OT})$$

Input Capacitor C_{IN}:

Input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency-switching current from passing to the input.

To minimize the potential noise problem, we place a typical X7R or a better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. At least a 20µF ceramic capacitor is suggested.

BUS Capacitor C_{BUS}:

1. Buck mode

The capacitor acts as the input capacitor of the Buck converter. The input current ripple rms value is larger than:

$$I_{CIN\_MIN} = I_{CHG}\sqrt{D(1-D)}$$

Where I_{CHG} is the charge current.

2. Boost mode

C_{BUS} is the output capacitor of Boost converter. C_{BUS} reduces the BUS voltage ripple and ensures the stability of Boost. The output current ripple rms value is :

$$I_{CBUS\_RMS} = \frac{\Delta I}{2\sqrt{3}}$$

Where ΔI is the current ripple of inductor.

At least a 40µF ceramic capacitor is suggested.

Battery Capacitor C_{BAT}:

1. Buck mode

Battery capacitor acts as the output capacitor of Buck converter. C_{BAT} is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor. The output voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Buck} = \frac{(1-D)\times V_{BAT}}{8C_{BAT}F_{SW}{}^2L}$$

Where F_{SW} is the switching frequency.

2. Boost mode

C_{BAT} acts as the input capacitor of Boost converter. The input voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Boost} = \frac{D\times V_{BAT}}{8C_{BAT}F_{SW}{}^2L}$$

Where F_{SW} is the switching frequency.

At least a 20µF ceramic capacitor is suggested.

Inductor L:

Inductor selection trades off between cost, size, and efficiency. A lower inductance value corresponds with smaller size, but results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. However, a higher inductance value benefits from lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss. An inductor must not saturate under the worst-case condition.

1. Buck mode

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{BAT}(1 - V_{BAT}/V_{IN,MAX})}{F_{SW} \times I_{CHG,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{CHG,MAX}$ is the maximum charge current.
SY20753 is quite tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{CHG,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{IN\ MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

2. Boost mode

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{F_{SW} \times I_{DIS,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{DIS,MAX}$ is the maximum discharge current.
SY20753 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{DIS,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{2 \times F_{SW} \times L}$$

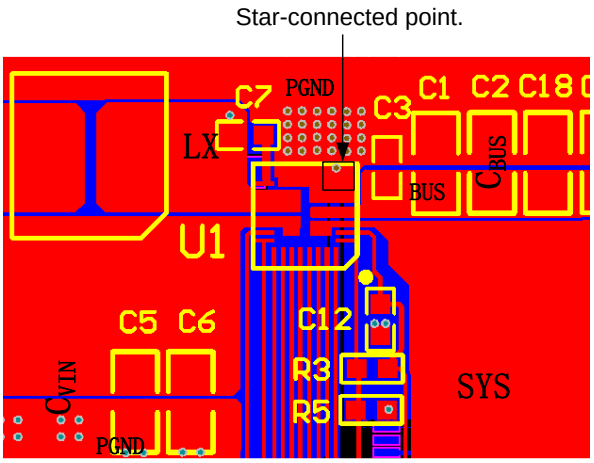
3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

Layout Design:

The layout design of SY20753 regulator is relatively simple. For the best efficiency and to minimize noise problems, we should place the following components close to the IC: C_{IN}, C_{BUS}, C_{SYS}, L.

1) It is desirable to maximize the PCB copper area connected to GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND, C_{BUS} must get close to pins BUS and GND. The loop area formed by C_{IN} and GND, C_{BUS} and GND must be minimized. The following figure is the recommended layout design.



3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The GND of MCU should be star-connected to the GND of the IC described in the above figure.

5) In high current applications, a RC snubber circuit should be placed between LX and GND for better EMI.

Typical Applications

Power Bank

In the application of power bank, when input source is present, SY20753 will work as a step down charger to charge battery and deliver power to SYS from input source. When input source is absent, SY20753 works as a step up converter to deliver power to SYS from battery.

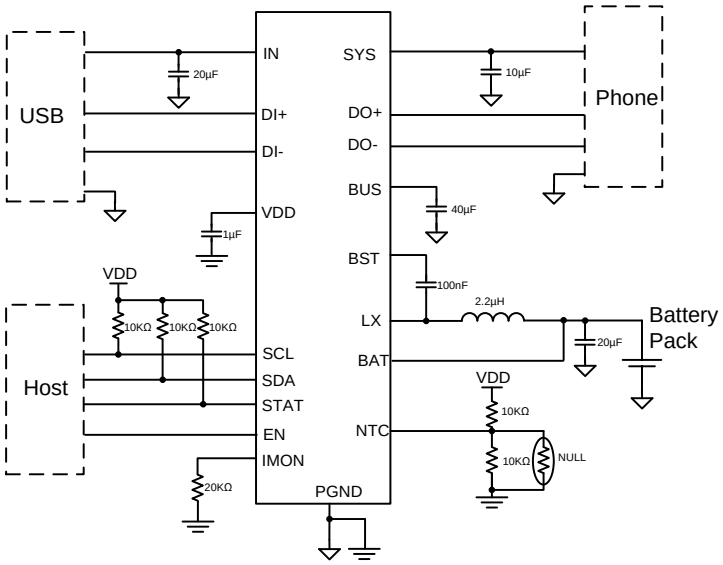


Figure3. Power Bank Application Schematic

1-cell Charger

In the application of 1-cell charger, SY20753 works as a step down charger with max 5A charge current. It features all the charger functions with VDPM, IDPM, CV, CC loop control and the protections with IN OVP, BAT SCP, NTC, thermal shutdown, timeout.

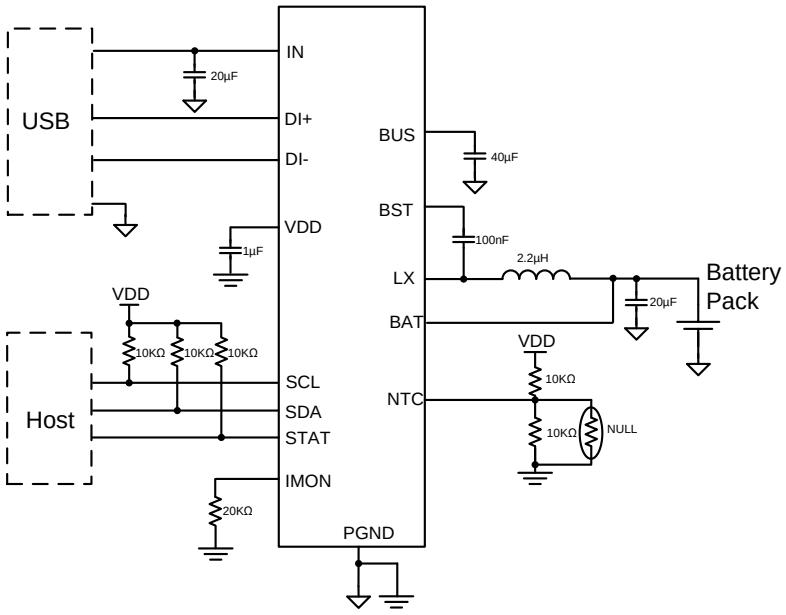


Figure4. 1-cell Charger Application Schematic

Boost Converter

In the application of Boost converter, SY20753 works as a step up converter with max 4.5A output current. The SYS voltage can be set according to the handshake of DO+/DO- or Downstream_Voltage_Set bit(REG05[4:2]). The Boost converter works in CV mode until the SYS current exceeds the SYS Current Limit. The SYS current will be limited to I_{SYS_Limit} when it exceeds I_{SYS_Limit}. SY20753 features all the protections with SYS SCP, BUS OVP, BAT depletion, NTC, thermal shutdown.

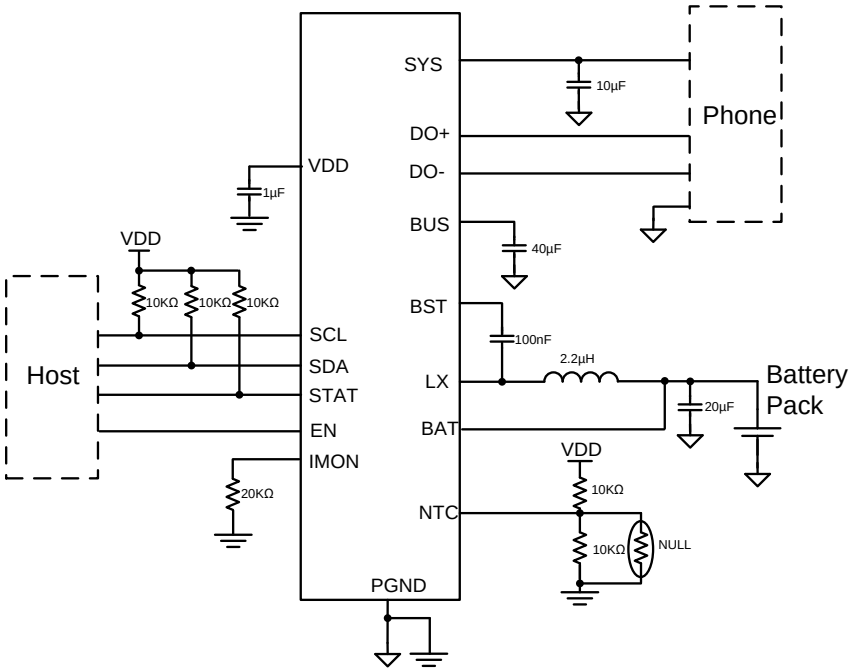


Figure5. Boost Converter Application Schematic

Register Description

Battery Charger Registers

The SY20753 supports 7 battery-charger registers that use either Write-Word or Read-Word protocols, as summarized in table 1. 04H are “read only” registers and can be used to identify SY20753.

Table1. Battery Charger Register Summary

Register Address	Register Name	Read/Write	Default
00H	Status/Control Register	Read or Write	XXH
01H	Control Register	Read or Write	84H
02H	Current Register	Read or Write	XXH
03H	Charge Register	Read or Write	89H
04H	Vendor/PN/Rev Register	Read	XXH
05H	Quick Charge Register1	Read or Write	XXH
06H	Quick Charge Register2	Read or Write	XXH
07H	Quick Charge Register3	Read or Write	XXH

REG00

Table2. Status/Control Register (00H)

Bit	Bit Name	R/W	Description
7	Reset	R/W	Write 1 to reset all the parameters, auto clear.
6	Boost	R	1: In Boost mode 0: Not in Boost mode
5:4	Status	R	00: Ready 01: Charge in progress 10: Charge done 11: Fault
3	BST_LLOAD	R	0:I_{SYS}> I_{SYS_L} 1:I_{SYS}< I_{SYS_L} ,Boost mode light load
2	BAT_DPL	R	0: V_{BAT}> V_{BATDEP} 1: V_{BAT}< V_{BATDEP}
1	V_{DPM}_STATE	R	1: In VDPM state 0: Not in VDPM state
0	V_{IN}_PRES	R	1: V_{IN} present; 0: V_{IN} absent.

REG01

Table3. Control Register (01H)

Bit	Bit Name	R/W	Description
7	Charge_Enable	R/W	0: Disable charger 1: Enable charger (default)
6	FB_EN	R/W	0:Disable FB(Default) 1:Enable FB
5	OTG_Enable	R/W	0: Disable OTG mode 1: Enable OTG mode (default)
4	OTG_Lightload	R/W	SYS light load threshold set. 0: 100mA (default) 1: 50mA
3	$V_{SYS\ COMP}$	R/W	System output voltage compensation in 5V mode. 1: 5.25V; 0: 5V(default).
2:1	Timer	R/W	Charge timeout protection. 00: 5h 01: 10h 10: 20h (default) 11: Disable timer
0	Freq	R/W	Buck and Boost converter frequency set. 0: 500kHz (default) 1: 300kHz

REG02

Table4. Current Register (02H)

Bit	Bit Name	R/W	Description
7:5	IDPM	R/W	Input current limit. 001: 0.5A 010: 1A 011: 1.5A 100: 2A 101: 2.5A 110: 3A 111: Disable input current limit
4:2	I_{SYS_Limit}	R/W	SYS current limit. 000: 1A 001: 1.5A 010: 2A 011: 2.5A 100: 3A 101: 3.5A (default) 110: 4A 111: 4.5A
1:0	I_{PKBST}	R/W	Boost peak current set. 00: 5A 01: 7A 10: 9A 11: 12A (default)

REG03

Table5. Voltage Register (03H)

Bit	Bit Name	R/W	Description
7:5	VDPM	R/W	Input voltage dynamic control. For 5V/7V/9V/12V input voltage set, $V_{DPM}=V_{IN\_SET}$ x(1-bit[7:5]). The VDPM need be clamped upon UVLO threshold. 000: 0 001: 2% 010: 4% 011: 6% 100: 8% (default) 101: 10% 110: 12% 111: Disable VDPM
4:3	Charge_Voltage	R/W	Max charge voltage. 00: 4.10V 01: 4.20V (default) 10: 4.35V 11: 4.4V
2:0	Charge_Current	R/W	Max charge current 000: 0.5A 001: 1A (default) 010: 1.5A 011: 2A 100: 2.5A 101: 3A 110: 4A 111: 5A

REG04

Table6. Vendor/PN/Rev Register (04H)

Bit	Bit Name	R/W	Description
7:5	Vendor_Code	R	101: Identify the supplied
4:3	PN	R	11: SY20753
2:0	Revision	R	001: Revision 1.0 010: Revision 1.1 011: Revision 1.2 ……

REG05

Table7. Quick Charge Register1 (05H)

Bit	Bit Name	R/W	Description
7:5	Downstream_Voltage_ Request	R	Record the voltage of downstream request. 111:12V(PE) 110:9V(PE) 101:7V(PE) 100:5V(PE) 011:12V(QC) 010:9V(QC) 001:continuous mode (QC) 000:5V(QC)
4:2	Downstream_Voltage_Set	R/W	Set the output voltage of SYS. 111:12V(PE) 110:9V(PE) 101:7V(PE) 100:5V(PE) 011:12V(QC) 010:9V(QC) 001:continuous mode (QC) 000:5V(default)
1:0	Continuous_Mode_UP_DOWN	R/W	QC3.0 continuous mode control. In continuous mode, in order to increase the SYS voltage by 200mV, these 2 bits must be set to 01 and then to 00; in order to decrease the SYS voltage by 200mV these bits must be set to 10 and then to 00. 10:DOWN 01:UP 00:HOLD (defalut) 11: Enable Divider mode(When bit 1:0 is 11b, the divider mode is enabled)

REG06

Table8. Quick Charge Register2 (06H)

Bit	Bit Name	R/W	Description
7:6	DI-_Input_Voltage	R	11:> 2.7V 10:2.0-2.7V 01:0.35V-2.0V 00:0-0.35V
5:4	DI+_Input_Voltage	R	11:> 2.7V 10:2.0-2.7V 01:0.35V-2.0V 00:0-0.35V
3:2	DI+_Output_Voltage	R/W	11:Floating(default) 10:3.3V 01:0.6V 00:0V

1:0	DI-_Output_Voltage	R/W	11:Floating(default) 10:3.3V 01:0.6V 00:0V

REG07

Table9. Quick Charge Register3 (07H)

Bit	Bit Name	R/W	Description
7:6	Input_Voltage_Set	R/W	Set the input voltage to change VDPM and VIN OVP. 11:12V 10:9V 01:7V 00: 5V(Default)
5:4	Upstream_USB_type	R	After BC1.2 detection, the USB type is recorded. 11: nonstandard adapter 10: DCP 01: CDP 00: SDP
3	BC1.2_DET_DONE	R	Indicate the BC1.2 detection status. 1: done 0: not done
2	Downstream_device_QC_support	R	Indicate whether downstream device supports QC. 1: support 0: not support
1	Downstream_QC_EN	R/W	1:Enable QC2.0 and QC3.0 Detect(default) 0:Disable QC2.0 and QC3.0 Detect
0	Downstream_OUT_SEL	R/W	SYS output voltage control. 1:Set by REG05[4:2] 0:SY20753 set according DO+/DO- (default)

I²C Interface

SY20753 uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two BUS lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the BUS and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6AH, receiving control inputs from the master device like a micro controller or a digital signal processor. （The device address should be left shift 1 bit for write and read operation, the new device address after left shift 1 bit is D4H). The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connected to the positive supply voltage via a current source or a pull- up resistor. When the BUS is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

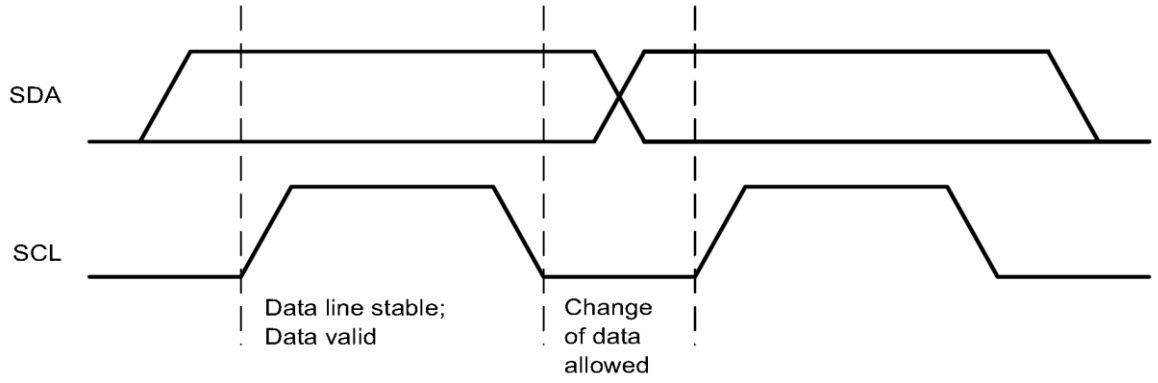


Figure6. Bit Transfer on the I²C BUS

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The BUS is considered busy after the START condition, and free after the STOP condition.

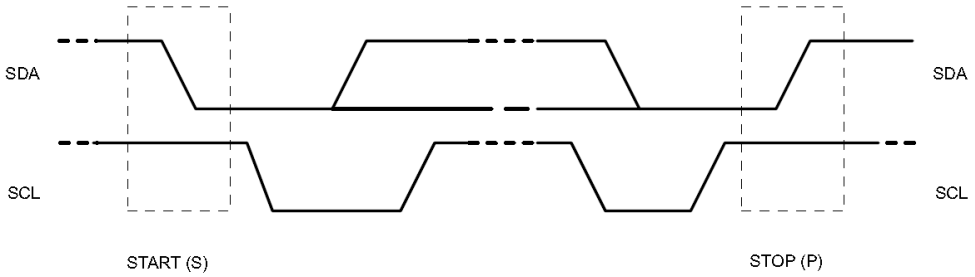


Figure7. START and STOP Conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data will transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

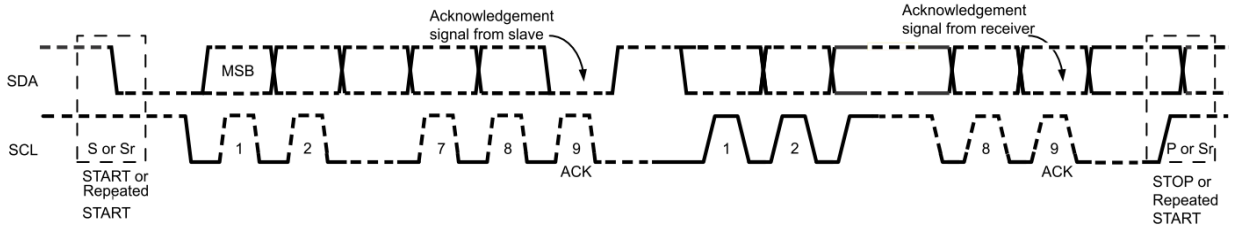


Figure8. Data Transfer on the I²C BUS

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A “0” indicates a transmission (WRITE) and a “1” indicates a request for data (READ).

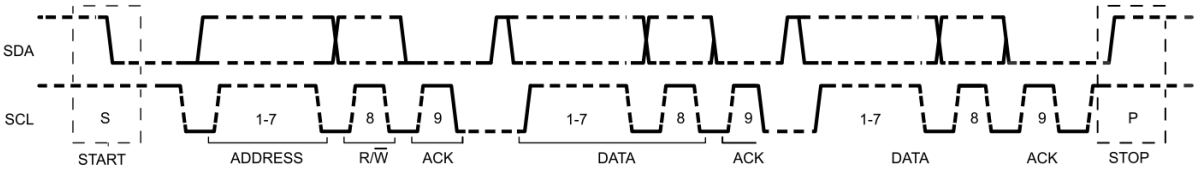


Figure9. Complete Data Transfer

Single Read and Write

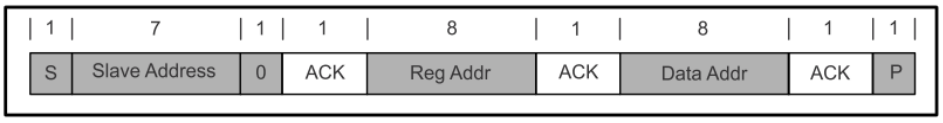


Figure10. Single Write

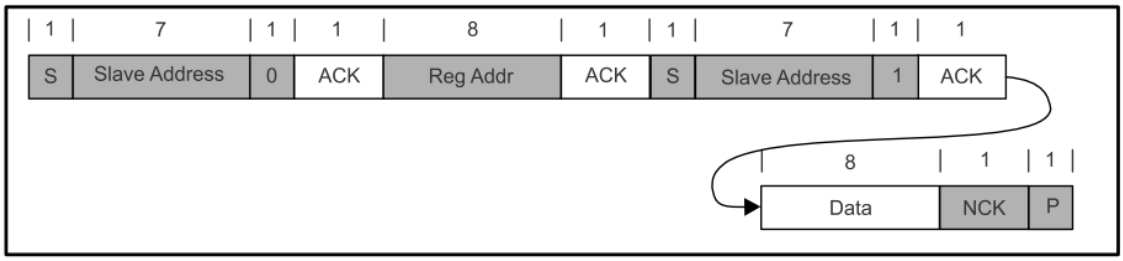
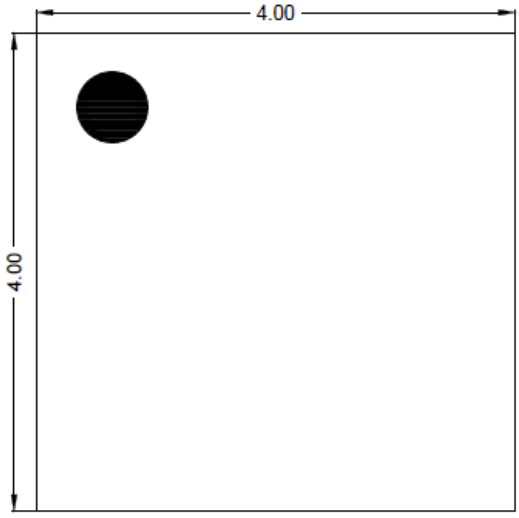


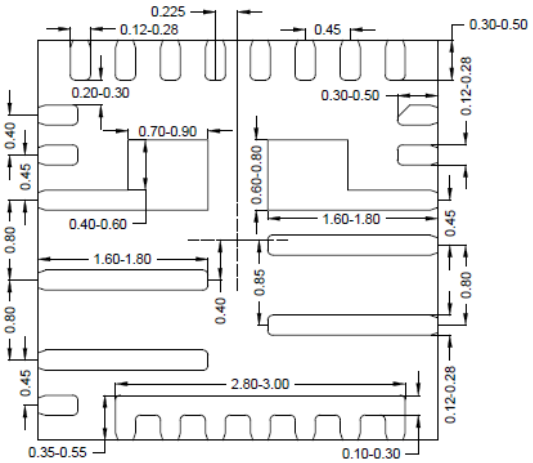
Figure11. Single Read

If the register address is not defined, the charger will be sent back to NACK and return to the idle state.

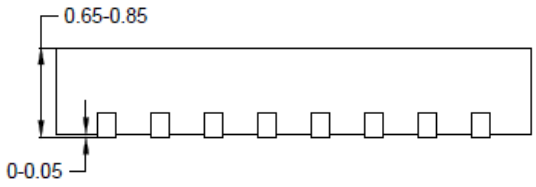
QFN4×4-20 Package Outline Drawing



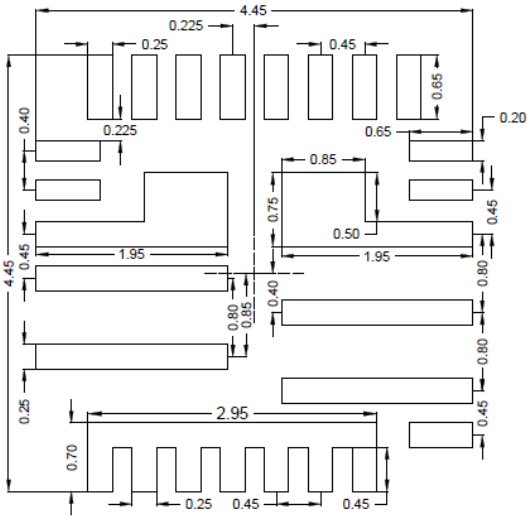
Top View



Bottom View



Side View

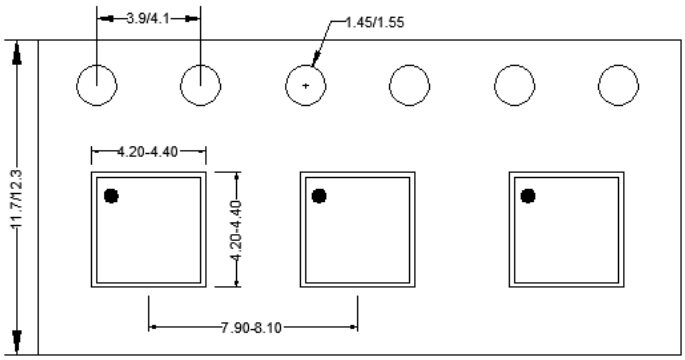


Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

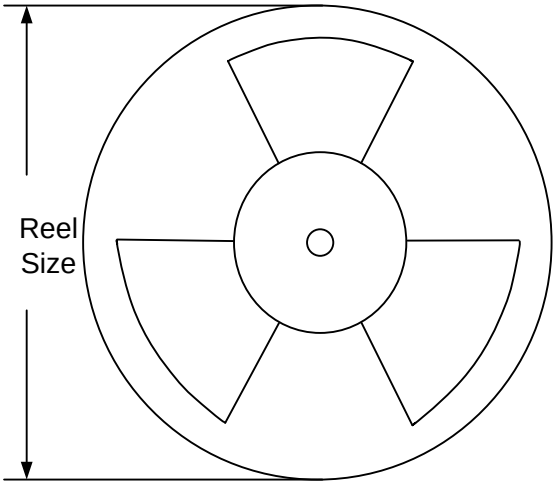
Taping & Reel Specification

1. QFN4×4 Taping Orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
QFN4x4	12	8	13"	400	400	5000

3. Others: NA

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