SY20759

Dual Ports, Wide Input, High Current, Bidirectional Regulator For Single Cell Li-Ion Battery Power Bank Application

General Description

The SY20759 is a dual ports wide input bidirectional regulator designed for Single Cell Li-Ion battery power bank application. Advanced bidirectional energy flow control with automatic input power source detection is adopted to achieve battery charging and battery discharging alternately. If the external power supply is present, the SY20759 will run in charging mode with fully protection function; if the external power supply is absent, the SY20759 will run in discharging mode with total output power capability up to 28W.

The SY20759 has integrated blocking switches to prevent current leaking from the output side or battery side to the input side and achieve over voltage/current protection at the output side. A half bridge with quasi-fixed high switching frequency is integrated to achieve power conversion for charging mode and discharging mode. All of them adopt N-channel MOSFET with 16V rating and extremely low $R_{DS(ON)}$ to optimize operation efficiency and extend battery life-time.

The SY20759 is available in QFN5×5 package to minimize the PCB layout size for wide portable applications.

Ordering Information

SY20759 □(□□□)

- □□ — Package Code
- □ — Optional Spec Code

Ordering Number	Package type	Note
SY20759QEQ	QFN 5×5-32	

Features

- Integrated N-Channel MOSFETs with 16V Voltage Rating and Extremely Low $R_{DS(ON)}$
- High Switching Frequency to Minimize Peripheral Circuit Design
- Trickle Current / Constant Current / Constant Voltage Charging Mode
- Maximum 8A Battery Charging Current
- Maximum 28W OTG Output Power
- Automatic Input Power Source Detection
- USB Port Identifier for Various Input Current Limit
- I^2C Controls
  - Programmable Battery Charge Voltage
  - Programmable Constant Charge Current
  - Programmable Input Voltage DPM
  - Programmable Input Current Limit and Output Current Limit
  - Programmable Bus Voltage for Discharging Mode
  - Programmable Battery Charging Timeout
- Charging Enable Control
- Charging Mode CV Tolerance +/-0.5%
- Host Enable Control for Standby Mode in Discharging Mode
- Battery UTP/OTP in Charging Mode and Discharging Mode
- Over Temperature Protection
- Light Load Status Indication
- Charge Status Indication
- Low Profile Package QFN5×5 for Portable Applications

Applications

- Single Cell Li-Ion Power Bank
- Portable Device with 1-Cell Battery Pack

Typical Application

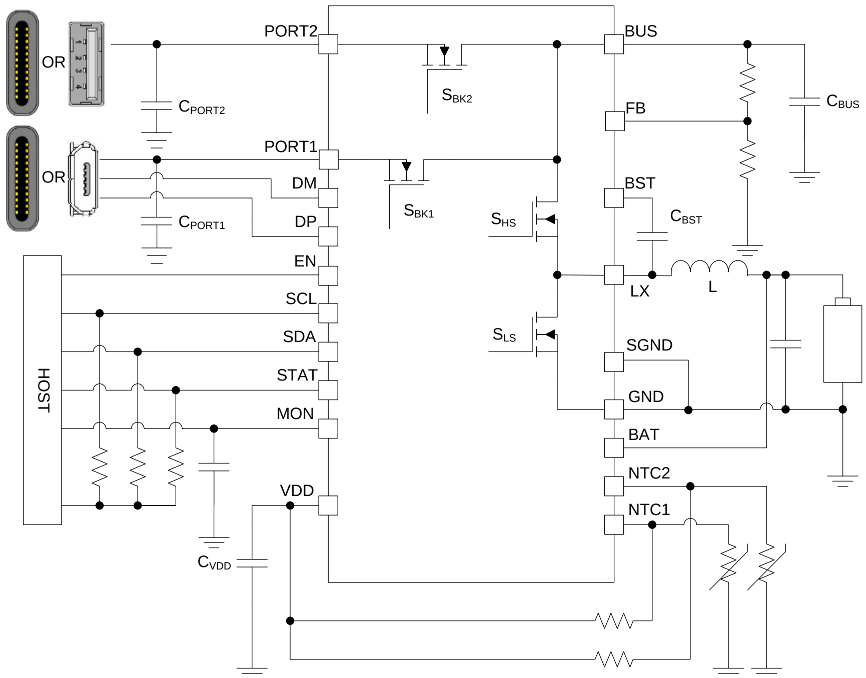
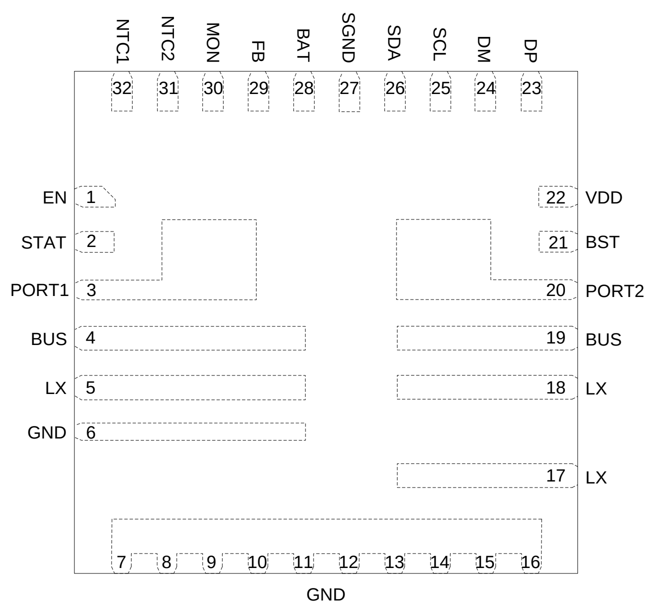


Figure1. Schematic Diagram

Pinout (Top view)



(QFN5×5-32)

Top Mark: EEE*xyz* (device code: **EEE**, ***x=year code, y=week code, z= lot number code)***

Pin Description

Name	PIN Number	Description
EN	1	Discharging mode enable pin. Active high to enable the IC and low to disable the IC when input power is absent. IC will always be enabled when input power is present.
STAT	2	Charging state indication pin. Open drain and can be used for turning on a LED to indicate the charge in process. When the charge is done, LED will be off. STAT pin will be pulled low for 256μs to generate an INT when input source type detection is finished.
PORT1	3	Bidirectional port. PORT1 accepts wide input voltage for normal operation. PORT1 can also provide a wide output voltage for the system. Connect a MLCC from this pin to ground to decouple high frequency noise.
BUS	4,19	Common connection point of the blocking FETs and half bridge. Connect at least 60μF MLCC from this pin to ground to decouple the high frequency noise.
LX	5,17,18	Switch node pin. Connect an external inductor from this pin to BAT pin.
GND	6,7,8,9,10,11,12,13,14,15,16	Power ground pin.
PORT2	20	Bidirectional port. PORT2 accepts wide input voltage for normal operation. PORT2 also can provide a wide output voltage for the system. Connect a MLCC from this pin to ground to decouple high frequency noise.
BST	21	Bootstrap pin. Connect a 100nF MLCC from this pin to LX.
VDD	22	Internal Linear regulator output. VDD is 3.3V when IC is enabled. Connect a 1μF ceramic capacitor from VDD to GND.
DP	23	DP/DM pins for PORT1. Support input USB type detection.
DM	24	
SCL	25	I²C Interface Clock.
SDA	26	I²C Interface Data.
SGND	27	Signal ground pin.
BAT	28	Battery positive sense pin.
FB	29	BUS voltage feedback pin. Connect to the center tape of a resistor divider to program the output voltage.
MON	30	Regulator monitor output pin. The sensed high-side current of half bridge, port current, port voltage and battery temperature can be reported on this pin.
NTC2	31	High temperature protection sense pin. In charging and discharging mode OTP threshold is 32.9% VDD. A 10kΩ resistor should be connected from NTC2 to the thermal resistor in the application of which the thermal resistor has the hot plug action.
NTC1	32	Battery thermal protection sense pin. In charging mode UTP threshold is 73.2% VDD and OTP threshold is 32.9% VDD. In discharging mode UTP threshold is 87.1% VDD and OTP threshold is 23.2% VDD.

Absolute Maximum Ratings (Note 1)

BUS, LX, PORT1, PORT2, BAT, EN, FB, STAT, DP, DM, SCL, SDA ---------------------------------- -0.5V to 18V
VDD, BST-LX, MON, NTC1, NTC2 -- -0.5V to 3.6V
Power Dissipation, P_D @ T_A = 25°C -- 2.5W
Package Thermal Resistance (Note 2)

θ_{JA} -- 25 °C/W

θ_{JC}-- 15°C/W

Junction Temperature Range --- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range --- -65°C to 125°C

Recommended Operating Conditions (Note 3)

BUS, LX, PORT1, PORT2, BAT, EN, STAT, DP, DM, SCL, SDA -- 0V to 16V
VDD, BST-LX, FB, MON, NTC1, NTC2 --- 0V to 3.3V
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range --- -40°C to 85°C

Electrical Characteristics

T_A=25°C, T_A=T_J, L=2.2μH, C_{BUS}=60μF, C_{PORT1}=1μF, C_{PORT2}=1μF, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Quiescent Current						
I_{BAT}	Battery Leakage Current	Input is absent, EN pull down, V_{BUS}≤V_{BAT}			40	μA
$I_{PORT1,2\_Q}$	PORT1,2 Input Quiescent Current	Charge terminated		2.8		mA
Input Power Supply UVLO						
V_{PORT_UVLO}	Input Voltage UVLO Threshold	Rising edge	3.6	3.8	4.0	V
V_{PORT_UVHYS}	Input Voltage UVLO Hysteresis	Falling edge		240		mV
LDO Output						
V_{VDD}	VDD Voltage	V_{BUS}=5V, chip enabled	3.2	3.3	3.4	V
I_{VDD}	VDD Source Current	V_{VDD}=3V	50			mA
Port FETs						
R_{BK1}, R_{BK2}	$R_{DS(ON)}$ of Blocking NMOS			15		mΩ
V_{PORT_OVP}	PORTs Voltage OVP Threshold Tolerance	V_{PORT_OVP}=6V	-3%		3%	
V_{PORT_OVPHYS}	PORTs Voltage OVP Hysteresis	Falling edge		2%		
V_{BUS_BATSC}	Output Short Circuit Protection Threshold	V_{BUS}-V_{BAT}, Falling edge	0.3	0.4		V
$T_{PORT\_SC\_REC}$	Port SCP Recovery Period			300		ms
$I_{PORT\_START\_MAX}$	PORT Maximum Current Limit at Start Up			3.5		A
Power MOSFET						
R_{HSFT}	$R_{DS(ON)}$ of High-side NFET			8		mΩ
R_{LSFT}	$R_{DS(ON)}$ of Low-side NFET			4.5		mΩ
Half-bridge in Buck Mode						
Voltage and Current Bias						
V_{DPM}	Input Voltage Regulation Tolerance	V_{DPM}=4.5V	-3.5%		0%	
I_{DPM}	Input Current Limit Tolerance	I_{DPM}=2A	-10%		10%	
		I_{DPM}=3A	-8%		8%	
Timer						
T_{TC}	Trickle Current Charge Timeout Tolerance	T_{TC}=0.1*T_{FC}	-15%		15%	
T_{FC}	Fast Charge (CC and CV) Timeout Tolerance	T_{FC}=20h	-15%		15%	
T_{MC}	Charging Mode Change Delay Time			30		ms
T_{TERM}	Termination Delay Time			300		ms
T_{RCHG}	Recharge Delay Time			300		ms
Switching Frequency						
f_{SWBK}	Buck Switching Frequency Tolerance	f_{SWBK}=500kHz	-20%		20%	
Battery Charging						
V_{CV}	Battery CV Voltage	V_{CV}=4.2V, Voltage on	-0.5%		0.5%	

	Tolerance	BAT pin				
ΔV_{RCH}	Battery Voltage Threshold Hysteresis for Recharge	Falling edge		100		mV
V_{BAT_OVP}	Battery Voltage OVP Threshold	Rising edge	103%	105%	107%	V_{CV}
V_{BAT_OVPHYS}	Battery Voltage OVP Hysteresis	Falling edge		2%		V_{CV}
V_{TRK}	Battery Trickle Charging Mode Voltage Threshold	Rising edge	2.7	2.8	2.9	V
I_{CC}	Charging Current Tolerance for Constant Current Mode	V_{BUS}=5V, V_{BAT}=3.5V, I_{CC}=6A	-10%		10%	
		V_{BUS}=5V, V_{BAT}=3.5V, I_{CC}=2A	-10%		10%	
I_{TC}	Charging Current Tolerance for Trickle Current Mode	V_{BUS}=5V, V_{BAT}=2.5V, I_{CC}=6A, I_{TC}=0.6A	-35%		25%	
		V_{BUS}=5V, V_{BAT}=2.5V, I_{CC}<=1A, I_{TC}=0.1A	-50%		50%	
I_{TERM}	Termination Current Tolerance	V_{BUS}=5V, I_{TERM}=0.2A	-40%		40%	
		V_{BUS}=5V, I_{TERM}=0.4A	-30%		30%	
Battery Short Circuit Protection						
V_{BAT_SHORT}	Battery Short Circuit Protection Threshold				2	V
Half-bridge in Boost Mode						
Voltage and Current Bias						
V_{BAT_DEP}	Battery Depletion Voltage Tolerance	Falling edge, BAT_DEP=1	2.65	2.8	2.95	V
		Falling edge, BAT_DEP=0	2.45	2.6	2.75	V
V_{BAT_DEPHYS}	Battery Depletion Voltage Hysteresis	Rising edge		400		mV
V_{FB}	FB Reference for Boost Regulation		0.99	1	1.01	V
V_{FB_OVP}	FB OVP Threshold in Boost Mode	Rising edge	108%	110%	112%	V_{FB}
V_{FB_OVPHYS}	FB OVP Hysteresis in Boost Mode	Falling edge		2%		V_{FB}
V_{BUS_SET}	BUS Voltage Tolerance in Boost Mode	V_{BUS_SET}=5V	-3%		1%	
V_{BUS_OVP}	BUS Voltage OVP Threshold in Boost Mode	Rising edge	106.5%	110%	113.5%	V_{BUS_SET}
V_{BUS_OVPHYS}	BUS Voltage OVP Hysteresis in Boost Mode	Falling edge		4.25%		V_{BUS_SET}
I_{O_LIMIT}	Output Current Limit Tolerance	I_{O_LIMIT}=1A	-10%		10%	
		I_{O_LIMIT}=3A	-8.5%		8.5%	
Switching Frequency						
f_{SWBST}	Boost Switching Frequency Tolerance	f_{SWBST}=500kHz	-20%		20%	
I_{PK_BOOST}	LSFET Peak Current Limit Tolerance in Boost Mode	I_{PK_BOOST}=11A	9.5	11	12.5	A

Other General Parameters						
Battery Thermal Protection NTC1						
K_{UT_CHG}	Under Temperature Protection in Charging Mode		71.2%	73.2%	75.2%	V_{DD}
	Under Temperature Protection Hysteresis in Charging Mode	Falling edge		5%		
K_{OT_CHG}	Over Temperature Protection in Charging Mode		31.4%	32.9%	34.4%	
	Over Temperature Protection Hysteresis in Charging Mode	Rising edge		2%		
K_{UT_DCHG}	Under Temperature Protection in Discharging Mode		85.1%	87.1%	89.1%	
	Under Temperature Protection Hysteresis in Discharging Mode	Falling edge		5%		
K_{OT_DCHG}	Over Temperature Protection in Discharging Mode		21.7%	23.2%	24.7%	
	Over Temperature Protection Hysteresis in Discharging Mode	Rising edge		2%		
Thermal Protection NTC2						
K_{OT}	Over Temperature Protection		31.4%	32.9%	34.4%	V_{DD}
	Over Temperature Protection Hysteresis	Rising edge		2%		
Logic Level and Timing						
V_{LOW}	EN, OTG,SCL,SDA Low Level Threshold				0.4	V
V_{HIGH}	EN, OTG,SCL,SDA High Level Threshold		1.2			V

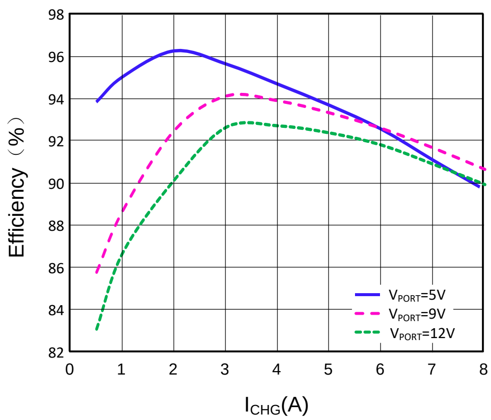
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC51-7 thermal measurement standard.

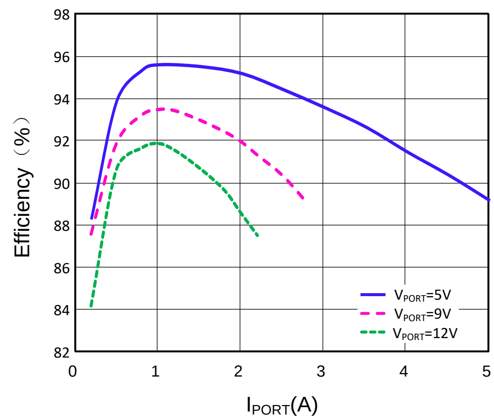
Note 3: The device is not guaranteed to function outside its operating conditions

Typical Performance Characteristics

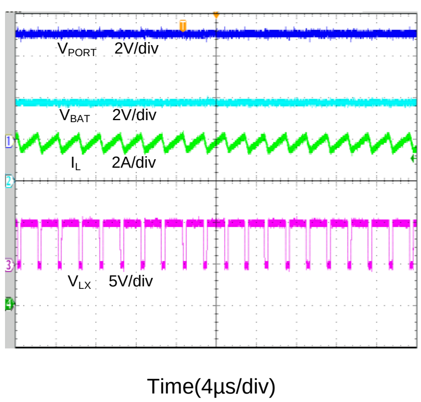
Efficiency vs. Charging Current (CV Mode)



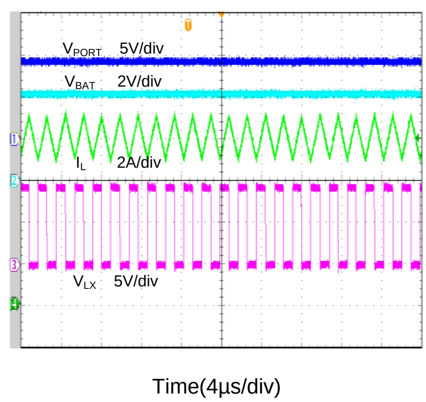
Efficiency vs. I_{PORT} (Boost Mode, BAT=3.7V)



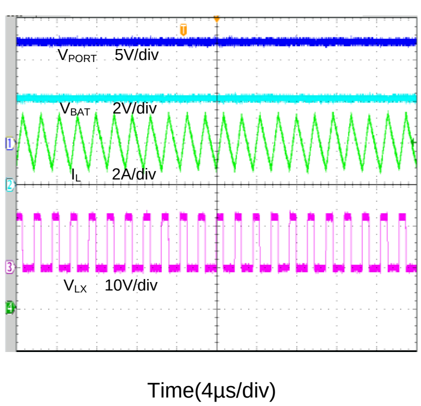
5V Buck Steady State



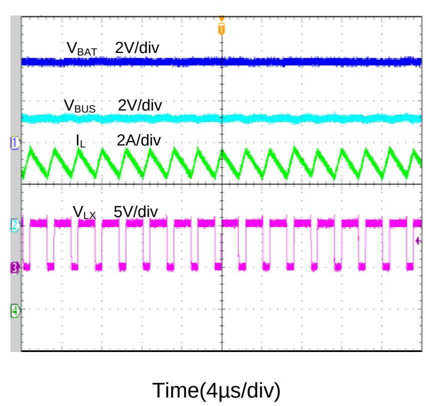
9V Buck Steady State



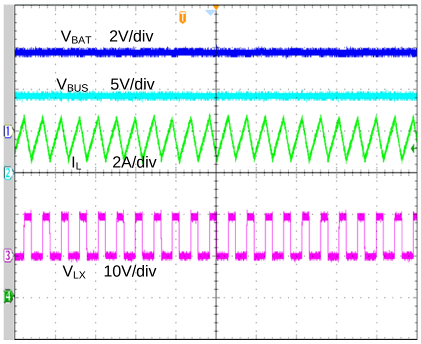
12V Buck Steady State



5V Boost Steady State

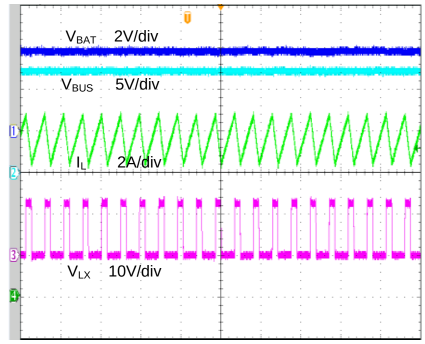


9V Boost Steady State



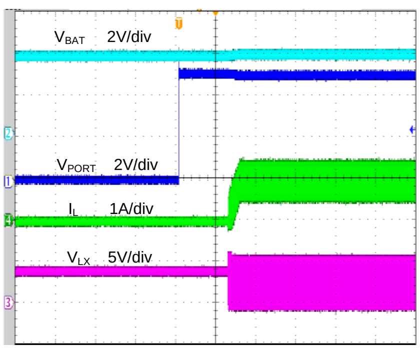
Time(4μs/div)

12V Boost Steady State



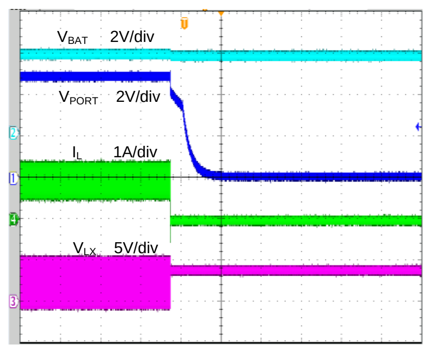
Time(4μs/div)

5V Buck Power on



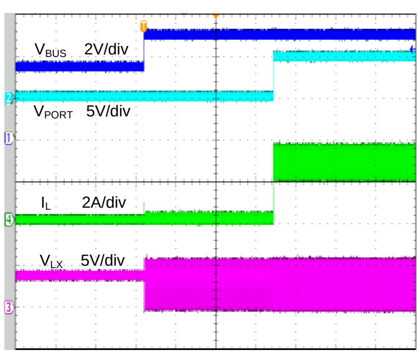
Time(40ms/div)

5V Buck Power off



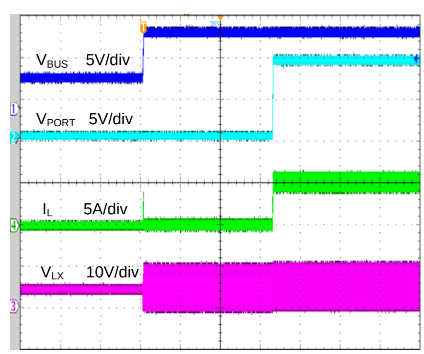
Time(40ms/div)

5V Boost OTG ON by I^2C



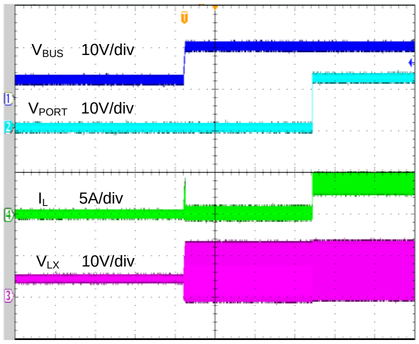
Time(100ms/div)

9V Boost OTG ON by I^2C



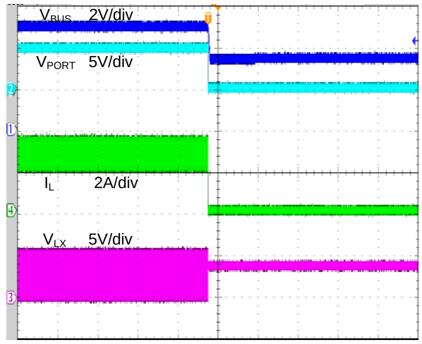
Time(100ms/div)

12V Boost OTG ON by I^{2}C



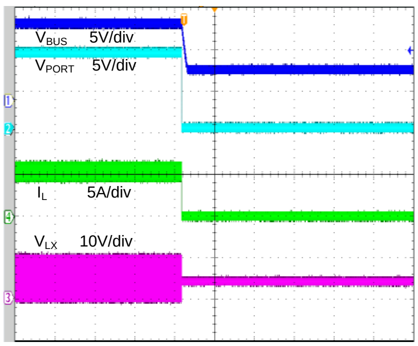
Time(100ms/div)

5V Boost OTG OFF by I^{2}C



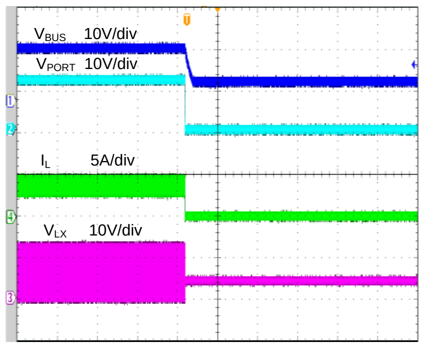
Time(100ms/div)

9V Boost OTG OFF by I^{2}C



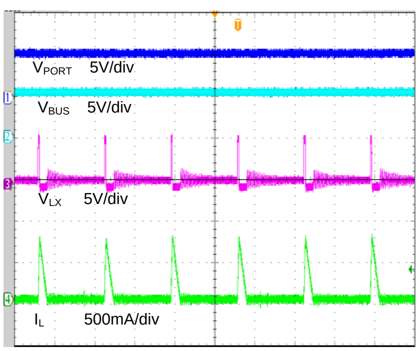
Time(100ms/div)

12V Boost OTG OFF by I^{2}C



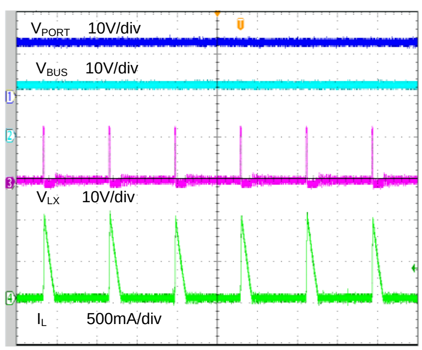
Time(100ms/div)

Battery Short in 5V Charging Mode



Time(10µs/div)

Battery Short in 12V Charging Mode



Time(10µs/div)

Operation

Device Power-on-Reset (POR)

The internal bias circuits are powered from the higher voltage of V_{BUS} and V_{BAT}. When V_{PORT} rises above V_{PORT_UVLO} or V_{BAT} rises above V_{BAT_DEP} and EN is high, the IC will be active, and VDD LDO will be powered on. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

Device Power up from Input Source

When an input source is plugged in, the SY20759 checks the input source voltage to turn on VDD LDO and all the bias circuits.

Automatic Input Power Supply Detection

When a good input source is present, PORT2_IN bit (REG0A[7]) or PORT1_IN bit (REG0A[6]) will be set to 1 and the STAT pin will generate an INT to host.

Input Source Type Detection

After the PORT1_IN bit is set to 1, the charger device runs Input Source Type Detection.

The SY20759 follows the USB Battery Charging Specification 1.2 (BC1.2) to detect USB type of adapter through USB DP/DM lines.

After input source type detection, DPDM_TYPE bits (REG0A[5:2]) is updated to indicate the input source USB type.

Charging (Buck) Mode Operation

As a battery charger, the SY20759 deploys constant off peak current mode step down converter to deliver power to battery. The constant off peak current converter keeps tight control of input voltage, input current, battery voltage, charge current, and simplifies output filter design.

An internal compensation network allows using ceramic capacitors at the output of the converter. The peak current of the inductor sensed by HSFET is compared to the internal error control signal to vary the duty cycle of the converter. The cycle-by-cycle current limit is implemented due to the peak current control mode.

Programmable Input Current Dynamic Power Management

When input current reaches I_{DPM}, the input current will be limited to I_{DPM} by regulating the duty cycle of Buck converter. The I_{DPM} loop will take control of the Buck converter until the input current decreases under I_{DPM}. The input current limit is programmed by IPORT2 and IPORT1 bits (REG03[7:0] and REG04[7:0]).

The I_{DPM} state is monitored by the SY20759 and is recorded by DPM_STAT bits (REG0B [7:6]). The host can read the register to monitor whether I_{DPM} loop works.

Programmable Input Voltage Dynamic Power Management

When input voltage drops to V_{DPM}, the input voltage will be limited to V_{DPM} by regulating the duty of Buck converter. The V_{DPM} loop will take control of the Buck converter until the input voltage rises above V_{DPM}. The input voltage limit is programmed by VDPM_SET bits (REG06[7:0]).

The V_{DPM} state is monitored by the SY20759 and is recorded by DPM_STAT bits (REG0B[7:6]). The host can read the register to monitor whether V_{DPM} loop works.

Programmable Charging Current

The max charging current of the SY20759 is limited to I_{CC} (set by CHG_CURRENT bits) when the charging current exceeds I_{CC}, charging current will be limited to I_{CC} by regulating the duty cycle of Buck converter. The constant current loop will take control of Buck converter.

Charging current is programmed by CHG_CURRENT bits (REG05[5:2]).

Programmable Termination Current

A charging cycle is terminated while battery voltage is above the recharging threshold and charging current is lower than termination current. After termination, only when battery voltage drops below recharging threshold, the SY20759 can exit termination state.

Termination current is programmed by ITERM bits (REG05[1:0]).

Programmable Charging Voltage

The max charging voltage is limited by the SY20759 to prevent the over-charging of Li-Ion. When the battery voltage reaches max charging voltage, the battery voltage will be limited to V_{CV} (set by CHG_VOLTAGE bits) by regulating the duty cycle of Buck converter. The charging voltage loop will take control of Buck converter until battery voltage drops below V_{CV}.

Charging voltage is programmed by CHG_VOLTAGE bits (REG05[7:6]).

Charging State Indication Description

1. Charge-in-process – Pulls and keeps STAT pin to Low;
2. Charge Done – Pulls and keeps STAT pin to High;

3. Fault Mode – Outputs high and low voltage alternatively with fixed 10Hz frequency.

Connect a LED from VDD to STAT pin. LED ON means Charge-in-process; LED OFF means Charge-Done; LED Flashing with10Hz means Fault-Mode. It can also be read by CHG_STAT bits (REG0B[1:0]).

Device Power up from Battery without Input Source

When the input source is absent and the battery voltage is above depletion threshold (V_{BAT_DEP}), VDD LDO will turn on after EN is high.

Discharging (Boost) Mode Operation

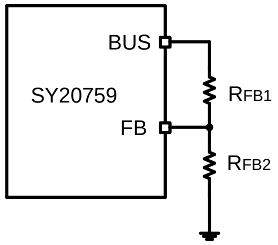
When the input is absent, the SY20759 deploys peak current mode step up converter to deliver power from the battery to other portable devices through PORT1 or PORT2 pin. The IC keeps tight control of BUS voltage and output current.

The Boost mode state can be monitored by reading the MODE bit (Reg0B[5]).

BUS Voltage Set

In discharging mode, the Boost converter modulates the BUS voltage according to FB or register setting.

If FB_SEL is set to 1, BUS voltage is set by external resister. $V_{BUS}=1\times(1+R_{FB1}/R_{FB2})$.



If FB_SEL is set to 0, BUS voltage is set by VBUS_SET_H bits (REG07[7:0]) and VBUS_SET_L bits (REG08[2:0]).

PORT Current Limit

In discharging mode, once PORT1 or PORT2 current exceeds its current limit I_{O_LIMIT}, the PORT current is limited to I_{O_LIMIT} by regulating the duty cycle of Boost converter. The PORT current limit loop takes control of Boost converter until the PORT current decreases under I_{O_LIMIT}.

PORT current limit is programmed by PORT Current Limit Register (REG03[7:0] and REG04[7:0]).

Interrupt to Host (INT)

The SY20759 will generate the INT (256us low) from STAT if one of below conditions is available.

1. Any DC input is present.
2. Input source type detection is done.

Protection Description

Charging Mode

During the half-bridge operating as synchronous Buck mode, the SY20759 has charging timeout protection, BAT over voltage protection, Input over voltage protection, BAT short circuit protection, PORT short circuit protection, and thermal protection for the Li-Ion battery and the device itself.

Input Over Voltage Protection

When the input voltage V_{PORT1} or V_{PORT2} is higher than the over voltage protection threshold, the half bridge will stop Buck operation immediately. The IC will recover to normal work when the monitored voltage backs to normal level.

BAT Over Voltage Protection

When V_{BAT} is higher than the over voltage protection threshold, the half bridge will stop Buck operation immediately. The IC will recover to normal work when the monitored voltage backs to normal level.

BAT Short Circuit Protection

When V_{BAT} is lower than V_{BAT_SHORT}, IC will wake up the battery with a safety small charge current.

Timeout Protection

Programmable timeout protection is designed for Trickle Current Charging Mode and Constant Current/Voltage Charging Mode. Once timeout is active, the IC will stop the charge operation and latch off. Only re-plug in power source can reset the latch logic and restart the normal charging work.

PORT Short Circuit Protection

When V_{PORT1} or V_{PORT2} is lower than V_{BUS}-0.45V over 1mS or lower than 2.25V, the IC will trigger PORT SCP. When PORT SCP occurs, the IC will turn off the linear FET immediately and try to recovery per 300ms.

NTC1 Thermal Protection

Thermal protection for battery is achieved through NTC1 pin. The IC will stop charging when UTP or OTP happens. It will recover to normal work when the temperature returns into normal range again.

NTC2 Thermal Protection

Thermal protection for connector (such as PORTC, PORTB) is achieved through NTC2 pin. The IC will stop charging when OTP happens. It will recover to normal work when the temperature decreases into normal range again.

Thermal Shutdown

To prevent the IC from over temperature, the IC will shut down when the junction temperature exceeds 150°C. It will recover to normal work when the junction temperature drops to 130°C.

Discharging Mode

During the half-bridge operating as synchronous Boost mode, the SY20759 has BUS over voltage protection, PORT short circuit protection, BAT depletion protection, and thermal protection for the Li-Ion battery and the device itself.

BUS Over Voltage Protection

When V_{BUS} is higher than the over voltage protection threshold, the half bridge will stop Boost operation. It will recover to normal work when BUS voltage backs to normal level.

BAT Depletion Protection

When the battery voltage is below the depletion threshold over 0.5S, IC stops Boost operation and reset the OTG_EN bit.

PORT Short Circuit Protection

When V_{PORT1} or V_{PORT2} is lower than V_{BUS}-V_{BUS_BATSC} over 1mS or lower than 2.25V, the IC will trigger PORT SCP. When PORT SCP occurs, the IC will turn off the PORT immediately and try to recovery per 300ms.

NTC1 Thermal Protection

Thermal protection for battery is achieved through NTC1 pin. The IC will stop discharging when UTP or OTP happens. It will recover to normal work when the temperature returns into normal range again.

NTC2 Thermal Protection

Thermal protection for connector (such as PORTC, PORTB) is achieved through NTC2 pin. The IC will stop discharging when OTP happens. It will recover to normal work when the temperature decreases into normal range again.

Thermal Shutdown

To prevent the IC from over temperature, the IC will shut down when the junction temperature exceeds 150°C. It will recover to normal work when the junction temperature drops to 130°C.

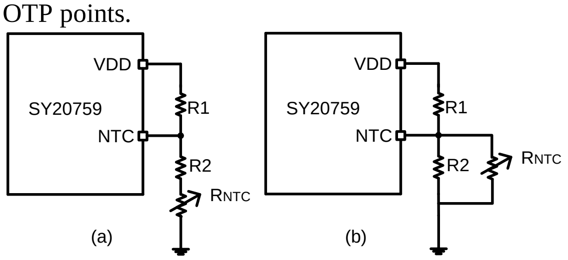
Applications Information

Because of the high integration of the SY20759, the application circuit based on this regulator IC is rather simple. Only port capacitor $C_{PORT1,2}$, BUS capacitor C_{BUS}, battery capacitor C_{BAT}, inductor L, NTC resistors R1, R2, need to be selected for the targeted application specifications.

NTC Resistor

The SY20759 monitors battery temperature by measuring the VDD voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K ($K = V_{NTC}/V_{VDD}$) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.

Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps of Figure (a) are:

1. Define K_{UT}, K_{UT}
2. Define K_{OT}, K_{OT}
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2

$$R2 = \frac{K_{OT}(1-K_{UT})R_{UT} - K_{UT}(1-K_{OT})R_{OT}}{K_{UT} - K_{OT}}$$

5. Calculate R1

$$R1 = (1/K_{OT} - 1)(R2 + R_{OT})$$

PORT Capacitor $C_{PORT1,2}$,

Input capacitor reduces the surge current drawn from the port and the switching noise from the device. The port capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency-switching current from passing to the input.

To minimize the potential noise problem, a typical X7R or better grade ceramic capacitor should be placed really close to the PORT1,2 and GND pins. Care should be taken to minimize the loop area formed by $C_{PORT1,2}$, and PORT1,2/GND pins. At least 1μF ceramic capacitor is suggested.

BUS Capacitor C_{BUS}

1. Buck mode

The capacitor acts as the input capacitor of the Buck converter. The input current ripple rms value is larger than:

$$I_{CIN\_MIN} = I_{CHG}\sqrt{D(1-D)}$$

Where I_{CHG} is the charge current.

2. Boost mode

C_{BUS} is the output capacitor of Boost converter. C_{BUS} reduces the bus voltage ripple and ensures the stability of Boost. The output current ripple rms value is :

$$I_{CBUS\_RMS} = I_{BUS}\sqrt{\frac{D}{1\text{-}D}}$$

Where I_{BUS} is the output current of Boost converter.

At least 60μF ceramic capacitor is suggested.

Battery Capacitor C_{BAT}

1. Buck mode

Battery capacitor acts as the output capacitor of Buck converter. C_{BAT} is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor. The output voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Buck} = \frac{(1-D)\times V_{BAT}}{8C_{BAT}F_{SW}^{2}L}$$

Where F_{SW} is the switching frequency.

2. Boost mode

C_{BAT} acts as the input capacitor of Boost converter. The input voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Boost} = \frac{D\times V_{BAT}}{8C_{BAT}F_{SW}^{2}L}$$

Where F_{SW} is the switching frequency.

At least 20μF ceramic capacitor is suggested.

Inductor L

Inductor selection trades off between cost, size, and efficiency. A lower inductance value corresponds with smaller size, but results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. However, a higher inductance value benefits from lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss. An inductor must not saturate under the worst-case condition.

1. Buck mode

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{BAT}(1 - V_{BAT}/V_{BUS,\,MAX})}{F_{SW} \times I_{CHG,\,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{CHG,MAX}$ is the maximum charge current.

The SY20759 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be larger than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{CHG,\,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{BUS,\,MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

2. Boost mode

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{F_{SW} \times I_{DIS,\,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{DIS,MAX}$ is the maximum discharge current.

The SY20759 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{DIS,\,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

Layout Design

The layout design of the SY20759 regulator is relatively simple. For the best efficiency and minimum noise problems, the following components should be placed close to the IC:

C_{PORT1}, C_{PORT2}, C_{BUS}, L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

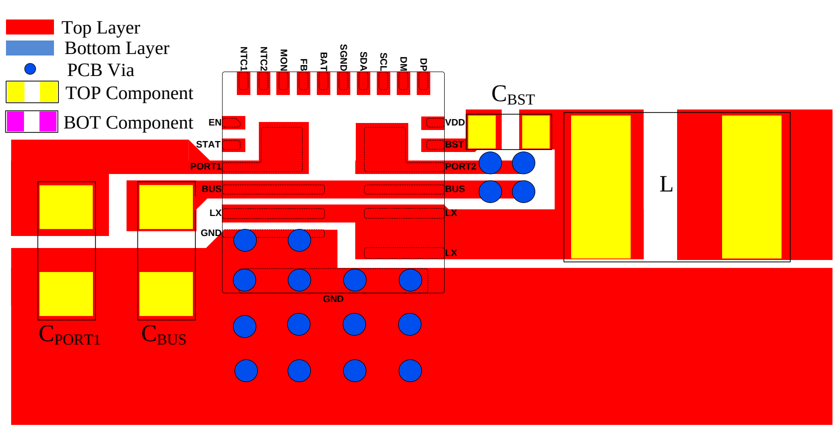
2) C_{BUS} must get close to Pins BUS and GND. The loop area formed by C_{BUS} and GND must be minimized.

3) C_{PORT1} should be close to Pins PORT1 and GND. C_{PORT2} should be close to Pins PORT2 and GND. The loop area formed by C_{PORT1} and GND, C_{PORT2} and GND should be minimized.

4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

5) In high current applications, a RC snubber circuit should be placed between LX and GND for better EMI.

Following figure is the recommended layout design.



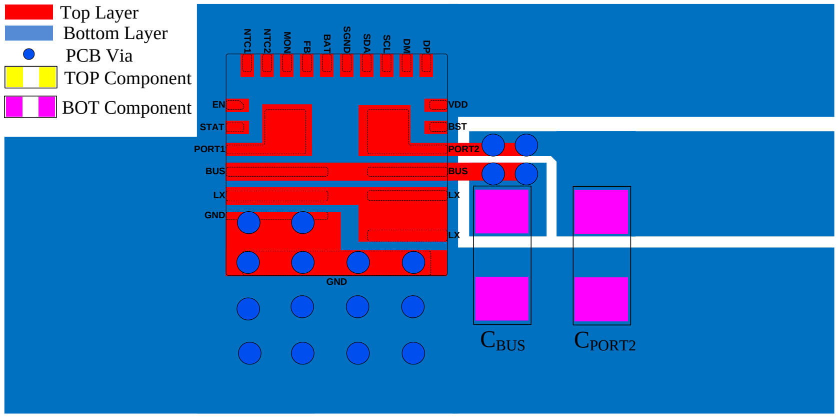


Figure2. Proposed PCB Layout

Register Description

Battery Charger Registers

The SY20759 supports 16 battery-charger registers that use either Write-Word or Read-Word protocols, as summarized in Table 1.

Table 1. Battery Charger Registers Summary

Register Address	Register Name	Read/Write
00H	Configuration Register 0	Read or Write
01H	Configuration Register 1	Read or Write
02H	Configuration Register 2	Read or Write
03H	PORT2 Current Limit Register	Read or Write
04H	PORT1 Current Limit Register	Read or Write
05H	Charger Control Register 0	Read or Write
06H	Charger Control Register 1	Read or Write
07H	Boost Control Register 0	Read or Write
08H	Boost Control Register 1	Read or Write
09H	Boost Control Register 2	Read or Write
0AH	Converter State Register 0	Read only
0BH	Converter State Register 1	Read only
0CH	Vendor/PN/Rev Register	Read only
0DH	DPDM Control Register	Read or Write
0EH	ADC Register	Read only
0FH	Faults Register	Read only

Table 2.Configuration Register 0 (00H)

Bit	Bit Name	R/W	Description
7	RESET	R/W	Write 1 to reset all the parameters. Auto clear.
6	PORT2_CFG	R/W	PORT2 direction control. 0: Input (default) 1: Output
5	PORT1_CFG	R/W	PORT1 direction control. 0: Input (default) 1: Output
4:3	PORT_OVP	R/W	PORT1 and PORT2 input voltage OVP. 00: 6V 01: 10.4V 10: 13.6V (default) 11: 16V

2:1	TIMEOUT	R/W	Charge timeout. 00: 5h 01: 10h 10: 20h (default) 11: Disable time out
0	NTC1_EN	R/W	NTC1 function enable. 0: Disable NTC1 UTP/OTP 1: Enable NTC1 UTP/OTP (default)

Table 3.Configuration Register 1 (01H)

Bit	Bit Name	R/W	Description
7	OTG_EN	R/W	Boost enable. 0: Disable OTG mode (default) 1: Enable OTG mode
6:5	OUT_LL	R/W	Output light load detection in both charging mode and discharging mode. 00: 0A, disable light load detection. 01: 50mA 10: 100mA 11: 200mA (default)
4	FB_SEL	R/W	Feedback selection in Boost mode. 0: VBUS_SET register 1: FB pin (default)
3:2	FSW	R/W	Switching frequency control. 00: 260kHz 01: 340kHz 10: 420kHz 11: 500kHz (default)
1	VBUS_COMP	R/W	Bus output voltage compensation. 0: 100% of VBUS_SET or VFB (default) 1: 105% of VBUS_SET or VFB
0	Reserved	NA	NA

Table 4.Configuration Register 2 (02H)

Bit	Bit Name	R/W	Description
7	BAT_DEP	R/W	Battery depletion voltage. 0: 2.6V (default) 1: 2.8V
6	FORCE_DPDM	R/W	Force DP/DM detection. 0: Not in DP/DM detection (default) 1: Force DP/DM detection
5	WIDE_INPUT_EN	R/W	PORT1 wide input enable bit. 0: Support 5V input voltage(default) 1: Support wide input voltage
4	FORCE_SBK2_OFF	R/W	PORT2 on/off control. 0: Not force S_{BK2} off (default) 1: Force S_{BK2} off
3	FORCE_SBK1_OFF	R/W	PORT1 on/off control. 0: Not force S_{BK1} off (default) 1: Force S_{BK1} off

2	EN_TEMPREG	R/W	Thermal loop enable. 0: Disable temp regulation loop(default) 1: Enable temp regulation loop
1:0	Reserved	NA	NA

Table 5.PORT2 Current Limit Register (03H)

Bit	Bit Name	R/W	Description
7:0	IPORT2	R/W	PORT2 current limit. When it is configured as an input pin, this register sets the I_{DPM} of PORT2. When it is configured as an output pin, this register sets the output current limit I_{O_LIMIT} of PORT2. PORT2 current limit, 00000000: 0mA, Shutdown S_{BK2} when it is an output port. 00000001: 25mA current limit 00000010: 50mA current limit 00000011: 75mA current limit 00000100:100mA current limit (default) … 11111111: 6375mA current limit

Table 6.PORT1 Current Limit Register (04H)

Bit	Bit Name	R/W	Description
7:0	IPORT1	R/W	PORT1 current limit. When it is configured as an input pin, this register sets the I_{DPM} of PORT1. When it is configured as an output pin, this register sets the output current limit I_{O_LIMIT} of PORT1. PORT1 current limit, 00000000: 0mA, Shutdown $S_{BK1}$when it is an output port. 00000001: 25mA current limit 00000010: 50mA current limit 00000011: 75mA current limit 00000100:100mA current limit (default) … 11111111: 6375mA current limit

Table 7.Charger Control Register 0 (05H)

Bit	Bit Name	R/W	Description
7:6	CHG_VOLTAGE	R/W	1-Cell max charge voltage. 00: 4.10V charge voltage 01: 4.20V charge voltage (default) 10: 4.35V charge voltage 11: 4.40V charge voltage
5:2	CHG_CURRENT	R/W	Max charge current. 0000: 0A charge current, disable charger 0001: 0.5A charge current (default) 0010: 1A charge current 0011: 1.5A charge current 0100: 2A charge current 0101: 2.5A charge current 0110: 3A charge current 0111: 3.5A charge current 1000: 4A charge current

			1001: 4.5A charge current 1010: 5A charge current 1011: 5.5A charge current 1100: 6A charge current 1101: 6.5A charge current 1110: 7A charge current 1111: 8A charge current
1:0	ITERM	R/W	Termination current of charger. 00: 100mA (default) 01: 200mA 10: 300mA 11: 400mA

Table 8.Charger Control Register 1 (06H)

Bit	Bit Name	R/W	Description
7:0	VDPM_SET	R/W	Input voltage dynamic control. 00000000: 2.5V(Disable VDPM) 00000001: 2.55V 00000010: 2.6V 00000011: 2.65V … 00101000: 4.5V (default) … 11111111: 15.25V

Table 9.Boost Control Register 0 (07H)

Bit	Bit Name	R/W	Description
7:0	VBUS_SET_H	R/W	BUS voltage set High 8 bits, V_{BUS_SET}= VBUS_SET_H*80mV+ VBUS_SET_L*10mV.The Boost is turned off, while V_{BUS_SET} is 2.5V. While V_{BUS_SET} is higher than 15.25V, REG07 and REG08 keep unchanged (VBUS_SET_H+ VBUS_SET_L=1001, 1111, 011 is the max value). V_{BUS_SET} is 5V in default (The default value is VBUS_SET_H+ VBUS_SET_L=0001, 1111, 010). 00000000: 2.5V(Disable Boost) 00000001: 2.580V 00000010: 2.660V 00000011: 2.720V … 00011111: 4.98V (default) … 10011111: 15.22V

Table 10.Boost Control Register1 (08H)

Bit	Bit Name	R/W	Description
7:3	Reserved	NA	NA
2:0	VBUS_SET_L	R/W	BUS voltage set Low 3 bits, V_{BUS_SET} = VBUS_SET_H*80mV+ VBUS_SET_L*10mV.The Boost is turned off, while V_{BUS_SET} is 2.5V. While V_{BUS_SET} is higher than 15.25V, REG07 and REG08 keep unchanged (VBUS_SET_H+ VBUS_SET_L=1001, 1111, 011 is the max

Bit	Bit Name	R/W	Description
			value). 000:0.00V 001:0.01V 010:0.02V(default) … 111:0.07V

Table 11.Boost Control Register 2 (09H)

Bit	Bit Name	R/W	Description
7:5	BOOST_IPK	R/W	Peak current limit in Boost mode. 000: 4A 001: 5A … 101: 9A (default) … 111:11A
4:2	MON_SET	R/W	Output one of the following parameters to the MON pin and ADC register. 000: VBAT (V_{MON}=0.25*V_{BAT}) 001: IHSFET (V_{MON}=0.25*I_{HSFET}) (default) (Buck) 010: VPORT2 (V_{MON}=0.1*V_{PORT2}) 011: IPORT2 (V_{MON}=0.25*I_{PORT2}) 100: VPORT1 (V_{MON}=0.1*V_{PORT1}) 101: IPORT1 (V_{MON}=0.25*I_{PORT1}) 110: VBUS (V_{MON}=0.1*V_{BUS}) 111: VNTC (V_{MON}=0.5*V_{NTC1})
1	Reserved	NA	NA
0	Reserved	NA	NA

Table 12.Converter State Register 0 (0AH)

Bit	Bit Name	R/W	Description
7	PORT2_IN	R	PORT2 input status. 0: No input on PORT2 1: DC source applied on PORT2 (INT)
6	PORT1_IN	R	PORT1 input status. 0: No input on PORT1 1: DC source applied on PORT1 (INT)
5:2	DPDM_TYPE	R	USB type of PORT1. 0000: Unknown adapter 0001: SDP 0010: CDP 0011: DCP 0100: 2V0/2V7 0101: 2V7/2V0 0110: 2V7/2V7 0111: 1V2/1V2 1000: Wide voltage adapter Sent INT when DPDM detection is done.
1	USBDET_DONE	R	Status of USB type detection. 0: Not done 1: Done
0	Reserved	NA	NA

Table 13.Converter State Register 1 (0BH)

Bit	Bit Name	R/W	Description
7:6	DPM_STAT	R	Input dynamic power management indication. 00: Not in DPM mode 01: In VDPM mode 10: In IDPM mode 11: NA
5	MODE	R	Status of half bridge. 0: Not in Boost mode 1: In Boost mode
4	SYS_LL_PORT1	R	PORT1 light load indication. 0: $I_{SYS}>I_{SYS\_LL}$ 1: $I_{SYS}<I_{SYS\_LL}$
3	SYS_LL_PORT2	R	PORT2 light load indication. 0: $I_{SYS}>I_{SYS\_LL}$ 1: $I_{SYS}<I_{SYS\_LL}$
2	BAT_DPL	R	Battery depletion indication. 0: Battery voltage is normal 1: Battery is depleted or removed
1:0	CHG_STAT	R	Charge status. 00: Ready, STAT=open 01: Charge in progress, STAT=low 10: Charge done, STAT=high 11: Charger fault, STAT high/low alternately

Table 14.Vendor/PN/Rev Register (0CH)

Bit	Bit Name	R/W	Description
7:5	VENDOR_CODE	R	101: Identify Silergy as the supplied
4:3	PN	R	11: SY20759
2:0	REVISION	R	001: Revision 1.0 010: Revision 1.1 011: Revision 1.2 ……

Table 15.DPDM Control Register (0DH)

Bit	Bit Name	R/W	Description
7:6	DM_INPUT_VOLT	R	DM input. 00:0-0.35V 01:0.35V-2.0V 10:2.0-2.7V 11:> 2.7V
5:4	DP_INPUT_VOLT	R	DP input. 00:0-0.35V 01:0.35V-2.0V 10:2.0-2.7V 11:> 2.7V
3:2	DP_OUTPUT_VOLT	R/W	DP output. 00:0V 01:0.6V 10:3.3V

Bit	Bit Name	R/W	Description
			11:Floating (default)
1:0	DM_ OUTPUT_VOLT	R/W	DM output. 00:0V 01:0.6V 10:3.3V 11:Floating (default) Set DP/DM output voltage before the input source type detection if the wide voltage adapter support is enabled.

Table 16.ADC Register (0EH)

Bit	Bit Name	R/W	Description
7:0	ADC_VBAT	R	BAT voltage.REG09[4:2]=000 Min resolution: 20mV Range: 0V~5.1V
	ADC_ICHG		Charging current in charging mode.REG09 [4:2] =001. Min resolution: I_{CC}/255 Range: 0~I_{CC}
	ADC_VPORT2 ADC_VPORT1 ADC_VBUS		PORT2 voltage.REG09[4:2]=010 PORT1 voltage.REG09[4:2]=100 BUS voltage.REG09[4:2]=110 Min resolution: 64mV Range: 0V~16.32V
	ADC_IPORT2 ADC_IPORT1		PORT2 current.REG09[4:2]=011 PORT1 current.REG09[4:2]=101 Min resolution: 25mA Range: 0A~6.375A
	ADC_VNTC/VDD		The result of V_{NTC1}/V_{DD}. REG09[4:2]=111 Min resolution: 0.35% Range: 0%~89.25%

Table 17. Faults Register (0FH)

Bit	Bit Name	R/W	Description
7	PORT_OVP	R	PORT OVP indication. 0: Not OVP 1: OVP
6	BUS_OVP	R	BUS OVP indication. 0: Not OVP 1: OVP
5	PORT_OCP/SCP	R	PORT OCP indication. 0: Not OCP 1: SYS OCP
4	BAT_OVP	R	Battery OVP indication. 0: Not OVP 1: OVP
3	CHG_ TIMEOUT	R	Charge timeout indication. 0: Not timeout 1: Timeout
2	NTC1_FAULT	R	NTC1 fault indication. 0: No fault 1: Fault
1	NTC2_FAULT	R	NTC2 fault indication. 0: No fault 1: Fault
0	THERMAL_SD	R	Thermal indication. 0: Not thermal 1: Thermal

I^{2}C Interface

The SY20759 uses I^{2}C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.
The device operates as a slave device with address d4H, receiving control inputs from the master device like micro controller or a digital signal processor. The I^{2}C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).
Both SDA and SCL are bidirectional lines, connecting to the positive supply voltage via a current source or pull- up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data transferred.

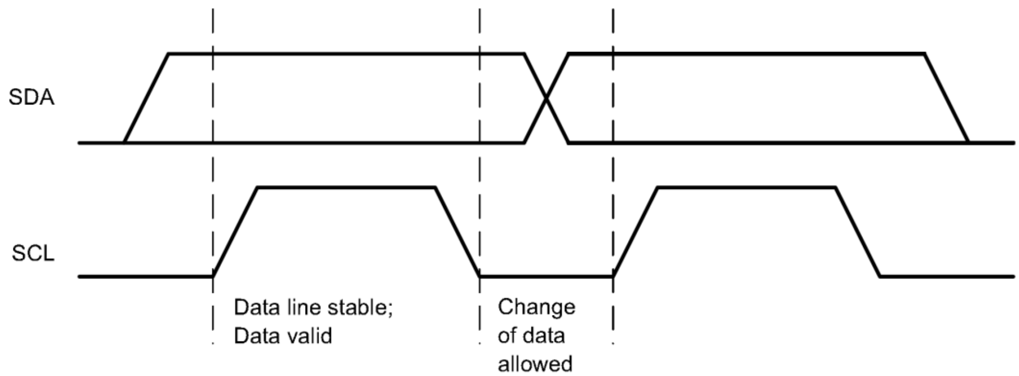


Figure3. Bit Transfer on the I^{2}C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.
START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

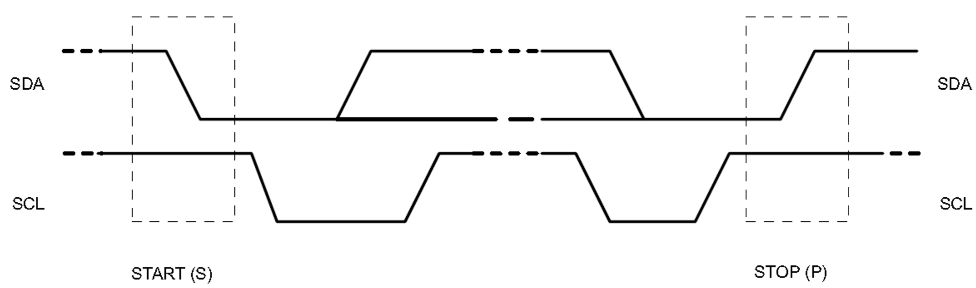


Figure4. START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first.

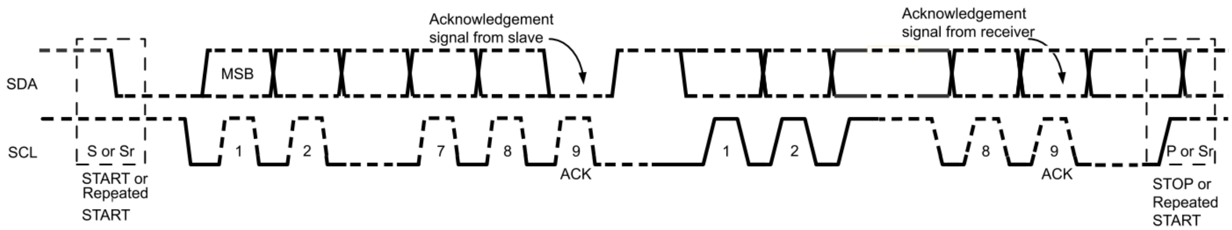


Figure5. Data Transfer on the I[2]C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.
The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.
When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

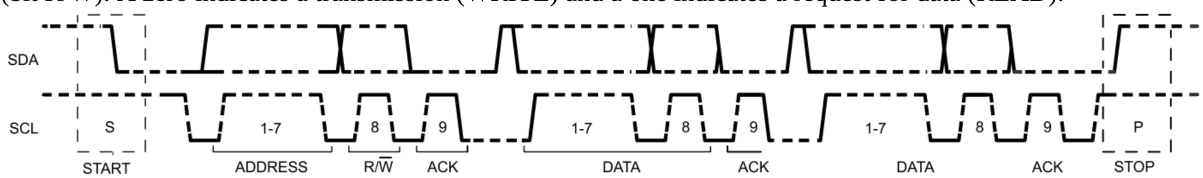


Figure6. Complete Data Transfer

Single Read and Write

Figure7. Single Write

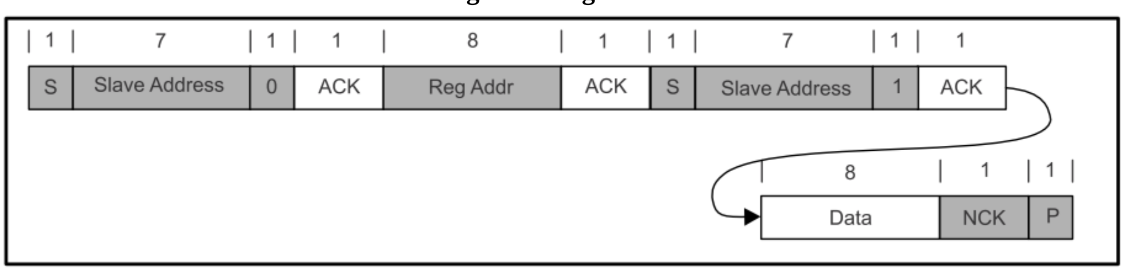
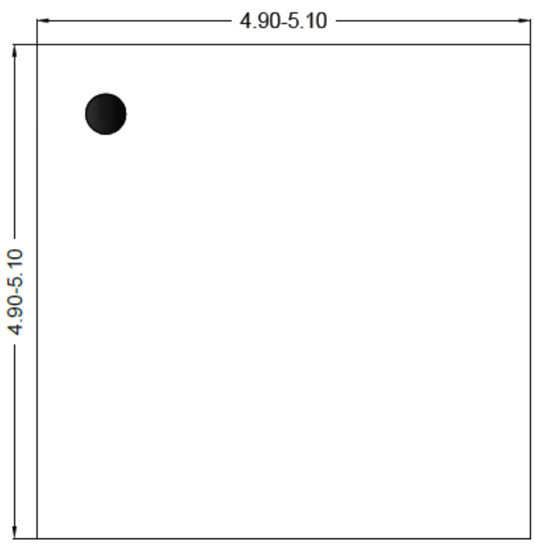


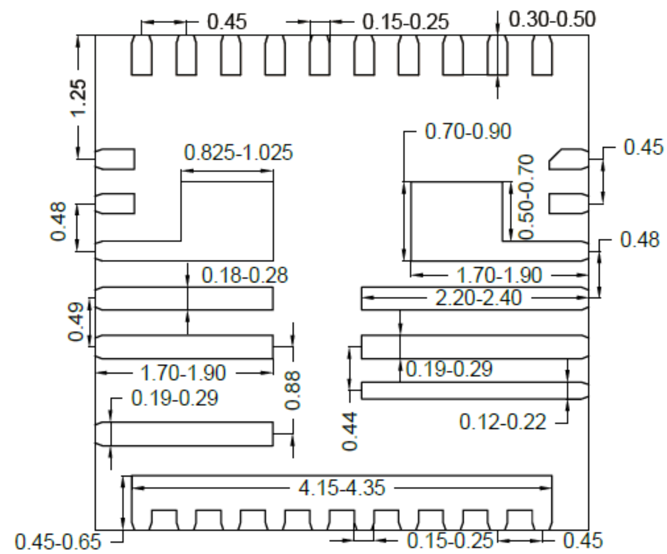
Figure8. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

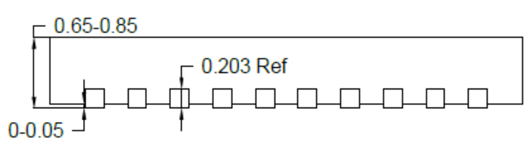
QFN5.0×5.0-32 Package Outline Drawing



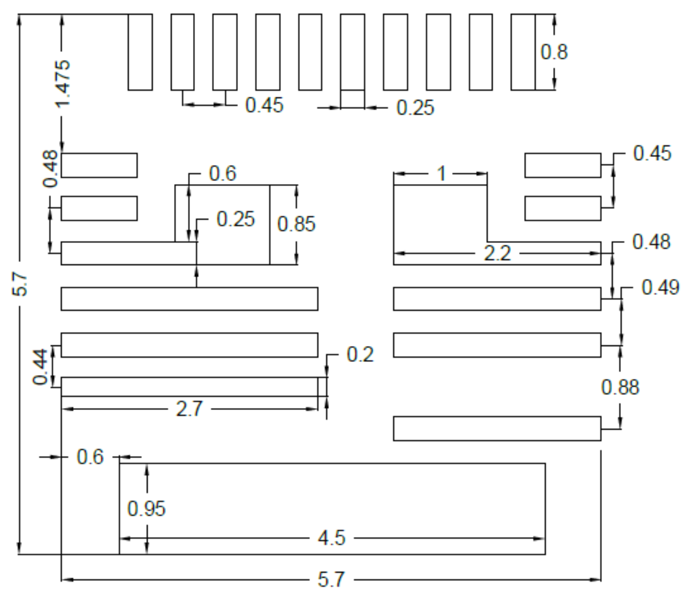
Top view



Bottom view



Side view



Recommended PCB layout (Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;

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