SY20762N

High Efficiency, 1.5A, Two-Cell Boost Li-Ion Battery Charger With System Power Path Management

General Description

The SY20762N is a synchronous Boost Li-Ion battery charger for two-cell with 3.6-5.5V input voltage range, which integrates 1MHz switching frequency and full protection functions. The charge current is up to 1.5A which can be programmed by using the external resistor for different portable applications. It has an input current limit with programmable threshold for safety battery charge operation. The IC consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design. The SY20762N also supports system power path management.

The SY20762N provides external separated control function for Boost and BATFET. It can provide power path selection to supply the system load from input source, battery, or both together.

The SY20762N is available in QFN3×3 package to minimize the PCB layout size for wide portable application.

Ordering Information

SY20762 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20762NQDC	QFN3×3-16	

Features

- Integrated Synchronous Boost with 18V Rating Low R_{DSON} FETs for High Charge Efficiency
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Maximum 1.5A Constant Charge Current
- Programmable Constant Charge Current
- Programmable Input Voltage Threshold for Adaptive Current Limit
- ±0.5% Battery Voltage Accuracy
- Input Voltage UVLO and OVP
- External Separated Control Function for Boost and BATFET
- System Power Path Management Function
- Input and Battery Inserted Indication
- Charge Status Indication
- Thermal Fold-back Protection
- Over Temperature Protection
- Low Profile QFN3×3 Package for Portable Applications

Applications

- Cellular Telephones, PDA, MP3 Players, MP4 Players
- Digital Cameras
- Bluetooth Applications
- PSP Game Players, NDS Game Players

Typical Application

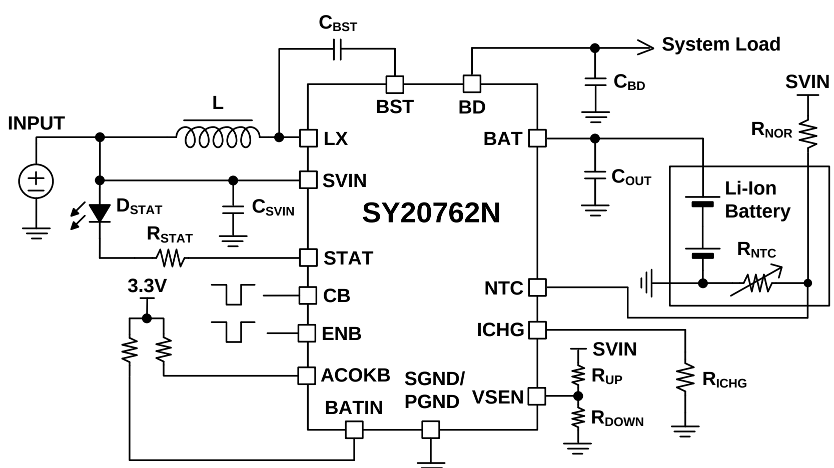

Figure1. Schematic Diagram

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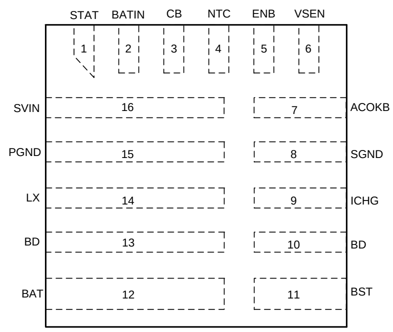
Pinout (top view)



(QFN3×3-16)

Top Mark: **F7*xyz***, **(**Device code: **F7**, ***x=year code, y=week code, z= lot number code)***

Pin Description

Pin Name	Pin No	Description
STAT	1	Charge status indication pin. It is open drain output pin and pulls high to SVIN through a LED to indicate the charge in process. When the charge is done, LED will be off.
BATIN	2	Battery inserted indication. Open drain output. Only can be pulled up to a lower than 3.3V power rail. Pull low if the battery is removed.
CB	3	BATFET control pin. Pull high logic to force the BATFET off.
NTC	4	Thermal protection pin. UTP threshold is typical 75% of V_{SVIN} and OTP threshold is typical 45% of V_{SVIN}. Pull down to ground will stop the charge.
ENB	5	Boost enable pin. Pull low to enable the Boost. ENB must be pulled high or low.
VSEN	6	Voltage sense of SVIN. If the voltage drops to internal 1.195V reference voltage, the SVIN will be clamped to setting value and input current will be limited.
ACOKB	7	Input power good indication. Open drain output. Pull low if the adapter or USB input is present.
SGND	8	Signal ground pin.
ICHG	9	Charge current program pin. Pull down to GND with a resistor R_{ICHG}. The mirror current about 1/10000 of the BATFET current will dump into the external resistor through ICHG pin and compared to the internal reference 1V. So I_{CC}=(1V/ R_{ICHG})×10000, I_{TC}=(1V/ R_{ICHG}) ×1000.
BD	10,13	Boost output pin. Bypass at least 20μF ceramic capacitor to GND. System load can be drawn from this pin.
BST	11	Boot-strap pin. Supply rectified FET's gate driver. Connect this pin to LX with 0.1μF ceramic capacitor.
BAT	12	Battery positive pin.
LX	14	Switch node pin. Connect to external inductor.
PGND	15	Power ground pin.
SVIN	16	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area.

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Absolute Maximum Ratings (Note 1)

SVIN, BAT, LX, NTC, STAT, ACOKB, BD, ENB, ICHG, VSEN-- -0.3V to 18V
BATIN, CB-- -0.3V to 4V
BST-LX -- -0.3V to 4V
Power Dissipation, PD @ T_A = 25°C, QFN3×3-- 2.6W
Package Thermal Resistance (Note 2)
θ_{JA} -- 38°C/W
θ_{JC} --- 4°C/W
Junction Temperature Range -- -40°C to +125°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range --- -65°C to 125°C

Recommended Operating Conditions (Note 3)

SVIN-- 3.6V to 5.5V
BAT, LX, NTC, STAT, ACOKB, BD, ENB, ICHG, VSEN-- -0.3V to 16V
BATIN, CB--- -0.3V to 3.3V
Ambient Temperature Range --- -40°C to 85°C

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Electrical Characteristics

T_A=25°C, V_{SVIN}=5V, GND=0V, C_{SVIN}=4.7μF, L=2.2μH, R_{ICHG}=10kΩ, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{SVIN})						
Supply Voltage Operation Range	V_{SVIN}		3.6		5.5	V
V_{SVIN} Under Voltage Lockout Threshold	V_{UVLO}	V_{SVIN} rising and measured from V_{SVIN} to GND			3.5	V
V_{SVIN} Under Voltage Lockout Hysteresis	ΔV_{UVLO}	Measured from V_{SVIN} to GND		100		mV
Input Over Voltage Protection	V_{OVP}	V_{SVIN} rising and measured from V_{SVIN} to GND	5.8			V
Input Over Voltage Protection Hysteresis	ΔV_{OVP}	Measured from V_{SVIN} to GND		0.5		V
Quiescent Current						
Battery Discharge Current	I_{BAT}	ACOKB=1, BAT=8.4V		50	70	μA
Input Quiescent Current	I_{IN}	V_{SVIN}=V_{NTC}=5V, ENB=1			1.5	mA
Oscillator and PWM						
Switching Frequency	F_{SW}			1000		kHz
Main N-FET Minimum off Time	t_{MIN_OFF}			100		ns
Main N-FET Maximum off Time	t_{MAX_OFF}			30		μs
Main N-FET Minimum on Time	t_{MIN_ON}			100		ns
Power MOSFET						
$R_{DS(ON)}$ of Main N-FET	R_{NFET_M}	MOSFET between LX and PGND		80		mΩ
$R_{DS(ON)}$ of Rectified N-FET	R_{NFET_R}	MOSFET between LX and BD		40		mΩ
$R_{DS(ON)}$ of BAT N-FET	R_{NFET_B}	BATFET, MOSFET between BD and BAT		40		mΩ
Voltage Regulation						
Battery Charge Voltage	V_{BAT_REG}		8.358	8.40	8.442	V
Recharge Threshold refer to V_{BAT_REG}	ΔV_{RCH}		100	200	300	mV
Trickle Current Charge Mode Battery Voltage Threshold	V_{TRK}	Rising edge threshold	5.4	5.6	5.8	V
Battery Connect Detection						
NTC Voltage Threshold for Battery Detection	V_{DET}		85%		95%	V_{SVIN}
Detect Delay Time	t_{DET}			30		ms
Charge Current						
Internal Charge Current Accuracy for Constant Current Mode		I_{CC}=1000mA	-10		10	%
Internal Charge Current Accuracy for Trickle Current Mode		I_{TC}=100mA	-50		50	%
Termination Current	I_{TERM}	I_{CC}=1000mA	50	100	150	mA
BAT Voltage OVP						
Battery Voltage OVP Threshold	V_{BAT_OVP}		105%	110%	115%	V_{BAT_REG}
Input Voltage Threshold for Adaptive Current Limit						
Voltage Reference of VSEN	V_{SEN}		1.17	1.195	1.22	V
Timer						
Charge Mode Change Delay Time	t_{MC}			30		ms
Termination Delay Time	t_{TERM}			30		ms
Recharge Deglitch Time	t_{RCHG}			20		s
Short Circuit Protection						
BAT Short Protection Threshold	V_{SHORT}		1.7	2	2.3	V

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Battery Charger Current when BAT Short Protection	I_{SC}	$V_{BAT}<V_{SHORT}$		5%		I_{CC}
BD Voltage Regulation						
BD Loop Voltage Regulation with Low Voltage Battery	V_{BD}	$V_{BAT}<V_{TRK}$		6.8		V
BD Loop Voltage Regulation with Normal Voltage Battery, $V_{BD}=V_{BAT}+\Delta V_{BD\_REG}$	ΔV_{BD_REG}	$V_{BAT}>V_{TRK}$		200		mV
BD Over Voltage Protection Threshold	V_{BD_OVP}			9.3		V
BD Over Voltage Protection Hysteresis	ΔV_{BD_OVP}			300		mV
Logic Input Voltage (ENB,CB)						
High Level Logic	V_{H_ENB}		1.5			V
	V_{H_CB}		1.5		3.3	
Low Level Logic	V_{L_ENB}, V_{L_CB}				0.4	V
Battery Thermal Protection NTC						
Under Temperature Protection	V_{NTC_UTP}		74%	75%	76%	V_{SVIN}
Under Temperature Protection Hysteresis	$V_{NTC\_UTP\_HYS}$	Falling edge		1.5%		
Over Temperature Protection	V_{NTC_OTP}		44%	45%	46%	
Over Temperature Protection Hysteresis	$V_{NTC\_OTP\_HYS}$	Rising edge		1.5%		
Thermal Fold-back and Thermal Shutdown						
Thermal Fold-back Threshold	T_{Fold}	Rising edge		120		ºC
Thermal Fold-back Threshold Hysteresis	T_{Fold_HYS}			20		ºC
Thermal Fold-back Ratio				0.25		I_{CC}
Thermal Shutdown Temperature	T_{SD}	Rising edge		160		ºC
Thermal Shutdown Temperature Hysteresis	T_{SD_HYS}			30		ºC

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

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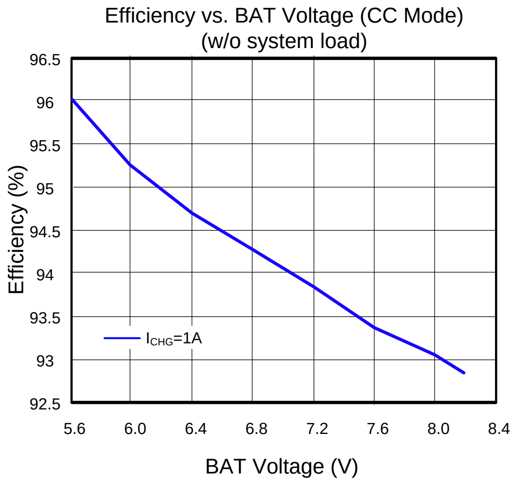
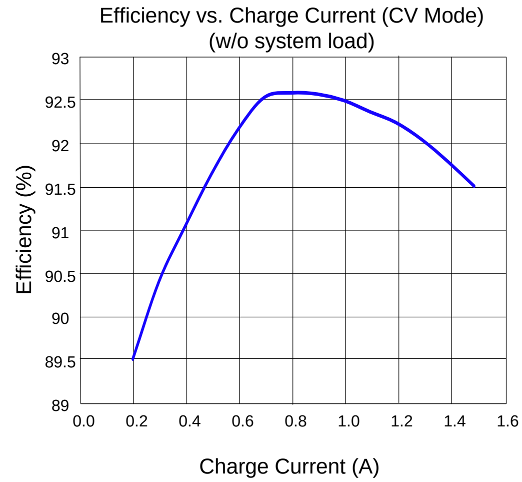
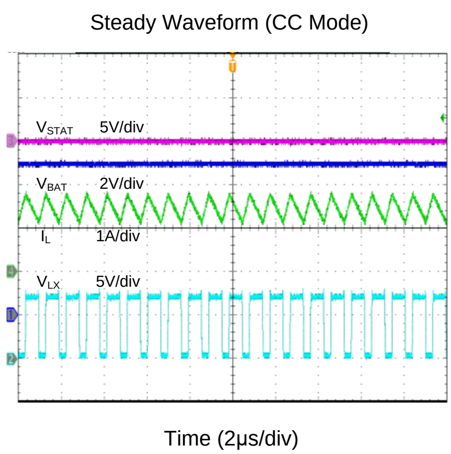
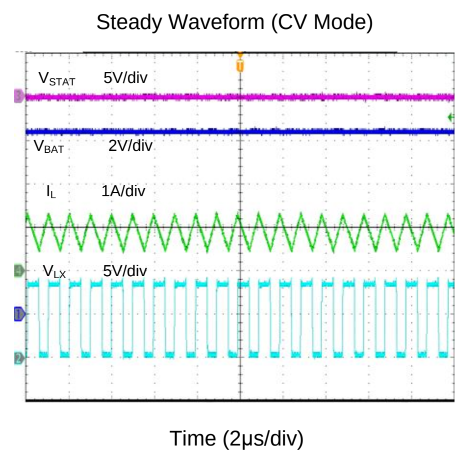
Typical Performance Characteristics

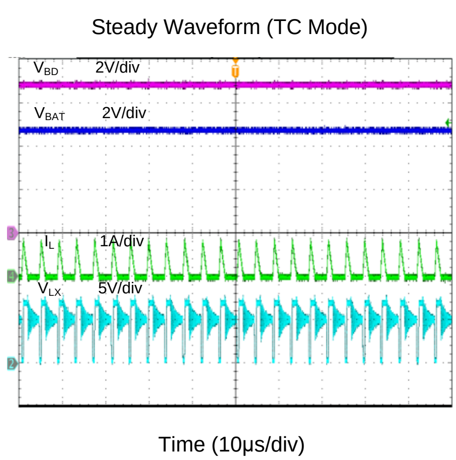
(T_A=25°C, V_{IN}=5V, GND=0V, C_{IN}=4.7μF, L=2.2μH, R_{ICHG}=10kΩ, unless otherwise specified.)

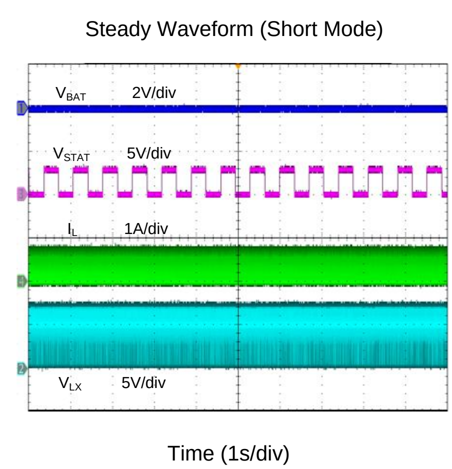












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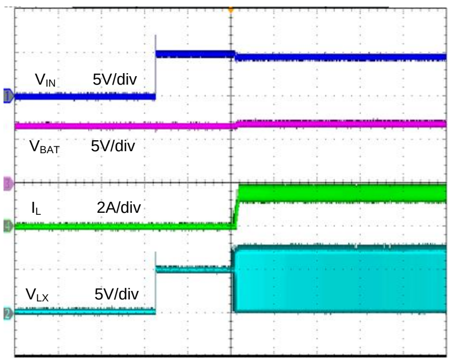
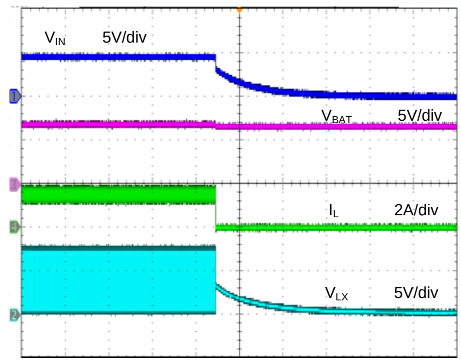
Power ON (CC Mode)



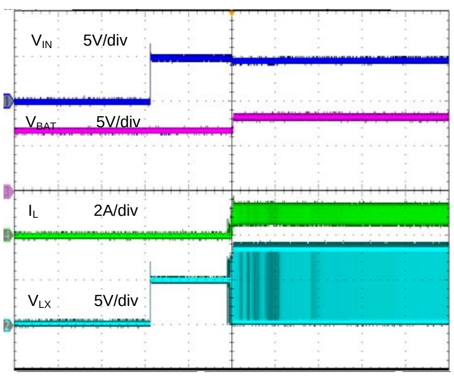
Time (400ms/div)

Power OFF (CC Mode)



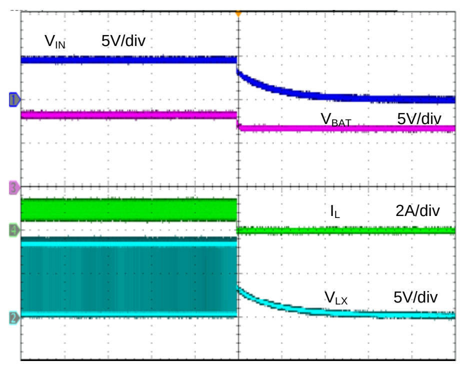
Time (400ms/div)

Power ON (CV Mode)



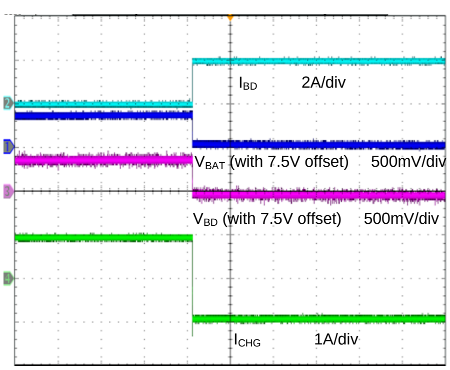
Time (400ms/div)

Power OFF (CV Mode)



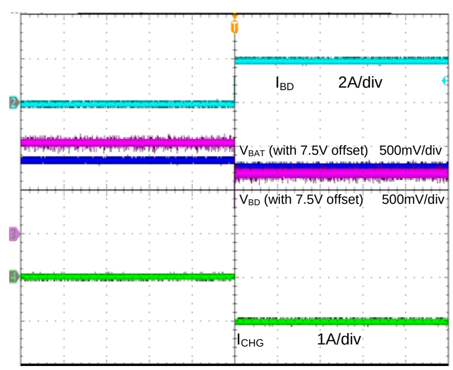
Time (400ms/div)

System 2A Load On during Charging



Time (1s/div)

System 2A Load On after Charge Termination



Time (1s/div)

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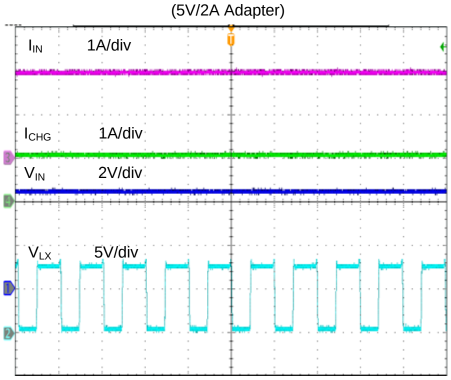
Adaptive Input Current Limit
(5V/2A Adapter)



Time (1μs/div)

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General Function Description

The SY20762N is a synchronous Boost Li-Ion battery charger for two-cell with 3.6-5.5V input voltage range, which integrates 1MHz switching frequency and full protection functions. The charge current is up to 1.5A which can be programmed by using the external resistor for different portable applications. It has an input current limit with programmable threshold for safety battery charge operation. The IC consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design. The SY20762N also supports system power path management.

Charging Status Indication Description

1. Charge-In-Process – Pull and keep STAT pin to low;
2. Charge Done – Pull and keep STAT pin to high;
3. Fault Mode – Outputs high and low voltage alternatively with 1.3Hz frequency. Connect a LED from SVIN to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flashing with 1.3Hz means Fault Mode. Fault Mode includes Input OVP, BAT OVP, BAT Short Circuit, NTC(UTP/OTP), No Battery Connection and Thermal Shutdown.

Input and Battery Indication Description

The SY20762N has input and battery detecting functions. If the input is present, the ACOKB will be pulled down. The device can judge if the battery pack is inserted based on the NTC pin voltage. If the battery is present, BATIN can be pulled high through the pull-up resistor.
ACOKB and BATIN detection will always work if the input adapter is present, regardless of the ENB level.
ACOKB and BATIN pins will be open internally if the input adapter is absent.

ENB, CB Control Logic Definition

The SY20762N provides external separated control function for Boost and BATFET.

a) ACOKB = High;
Boost FET always off and BATFET will keep on when a normal voltage battery is present, no matter what the CB signal is. The battery will discharge reversely for the system demand.

b) ACOKB = Low;
Boost FET is controlled by ENB signal, and BATFET is decided by ENB and CB signal when a normal voltage battery is present. The high CB signal can force BATFET off.

Charger Mode Basic Operation Description

In the charger mode, before the SY20762N starts up, C_{BD} is charged by the battery through the body diode of BATFET, and V_{BD} equals to V_{BAT}.
If the plug in input voltage V_{SVIN} is higher than V_{BD}, C_{BD} is charged by V_{IN} further through the body diode of Boost sync-FET. Under this condition, the Boost charger will operate in light load mode and regulate the V_{BD} at 6.8V and the BATFET work in linear charge mode. If the V_{BAT} is lower than the internal short circuit threshold V_{SHORT}, the linear charge current will be 1/20 I_{CC}. When V_{BAT} is higher than V_{SHORT} but lower than the threshold of trickle charge, the linear charge current will be 1/10 of I_{CC}. Note that, charging current will not be increased to I_{CC} when the BATFET operates in linear mode. With the increasing of V_{BAT}, when V_{BAT} is higher than V_{TRK}, the BATFET will be fully turned on and the switching mode Boost charger will take over the battery charging. The current in the BATFET is mirrored to be as the charging current I_{CHG}. If V_{IN} is lower than $V_{BD}=V_{BAT}$ at the plug in time, the switching mode Boost charger will start work directly.
During the charging mode, constant (trickle) charging current loop is active at first. When V_{BAT} equals to constant voltage threshold V_{BAT_REG}, constant voltage loop will take over and pull down the charging current. When I_{CHG} is lower than the termination current threshold I_{TERM}, the BATFET will be turned off first and Boost charger will regulate V_{BD} at V_{BAT}+200mV. Then, the SY20762N will be waiting for recharge mode.
The charge process is based on below rules.

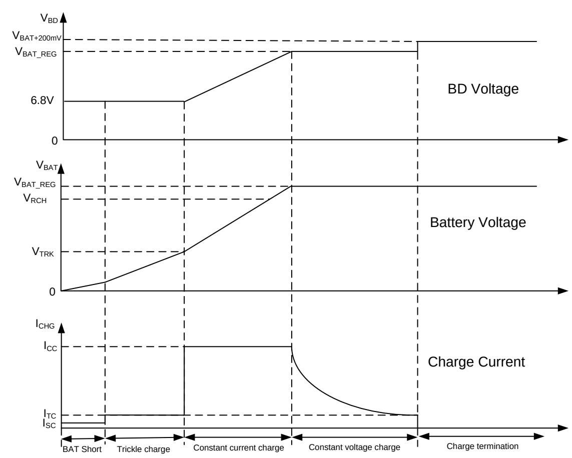

Figure2. Charge Process Sequence Diagram

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System Power Path Management

The SY20762N can provide power path selection to supply the system (BD pin) from input source, battery, or both together.

a) If the input source is absent (ACOKB=1) and the SY20762N can turn on the BATFET to supply system power from the battery.

b) If the input source is present (ACOKB=0), and the charge is ongoing, the SY20762N will provide system power and charging current from the input source. And when the charge is done, the SY20762N will turn off BATFET and regulate the BD voltage at V_{BAT}+200mV.

The SY20762N provides supplement mode to prevent overloading the input source. The heavy system load can be powered by input source and battery together.

Full Charger Protections Description

In charge mode, the SY20762N has full protections to protect the IC and the battery.

Input Over Voltage Protection – The SY20762N has input over voltage protection. It will turn off Boost and BATFET when input OVP occurs. IC will auto recover normal operation when fault removes.

BAT Over Voltage Protection –The SY20762N will turn off internal BATFET and stop charge when BAT OVP occurs. IC will auto recover normal operation when fault removes.

BAT Short – When the V_{BAT} is lower than V_{SHORT}, the SY20762N will regulate V_{BD} at 6.8V. The BATFET will enter linear mode with 1/20I_{CC} charge current.

BD Over Voltage Protection –When the V_{BD} is higher than V_{BD_OVP}, the SY20762N will turn off Boost. IC will auto recover normal operation when fault removes.

Battery Thermal Protection – When NTC voltage is lower than OTP threshold or higher than UTP threshold, the SY20762N will stop charging. IC will auto recovery when fault removes.

Thermal Shutdown Protection – The IC will turn off Boost and BATFET when the junction temperature is higher than 160°C. It will auto recover normal when fault removes.

Adaptive Input Current Limit Principle

The SY20762N can protect the input DC source from over load by the special loop control. The high load current will caused a voltage drop at SVIN when the input DC source is over load. When VSEN drops below the internal 1.195V reference, the SY20762N will decrease the duty cycle to reduce the load current.

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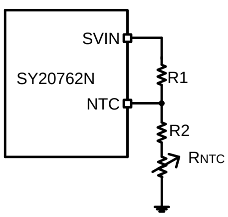
Applications Information

Because of the high integration of the SY20762N, the application circuit based on this charger IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, NTC resistors R_1, R_2, input voltage threshold resistors R_{UP}, R_{DOWN} need to be selected for the targeted applications specifications.

NTC Resistor

The SY20762N monitors battery temperature by measuring the input voltage and NTC voltage. The controller will trigger the UTP or OTP when the rate K ($K=V_{NTC}/V_{SVIN}$) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.

Choose R_1 and R_2 to program the proper UTP and OTP points.



The calculation steps are:

1. Define K_{UT}, K_{UT} =74~76%
2. Define K_{OT}, K_{OT} =44~46%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R_2,

$$R_2=\frac{K_{OT}(1-K_{UT})R_{UT}-K_{UT}(1-K_{OT})R_{OT}}{K_{UT}-K_{OT}}$$

5. Calculate R_1

$$R_1=(\frac{1}{K_{OT}}-1)\times(R_2+R_{OT})$$

If choose the typical values K_{UT} =75% and K_{OT}=45%, then

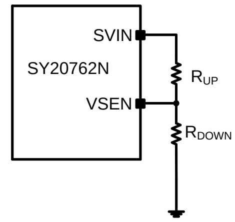
$$R_2=0.375R_{UT}-1.375R_{OT}$$

$$R_1=1.222(R_2+R_{OT})$$

Input Voltage Threshold for Adaptive Current Limit

The SY20762N will monitor input voltage by measuring the VSEN pin voltage, when the voltage of VSEN pin drops below the internal 1.195V reference, SY20762N will decrease the duty cycle to reduce the load current.

The input voltage sense network shows below, choose R_{UP}, R_{DOWN} to set the input voltage threshold V_{INT}:



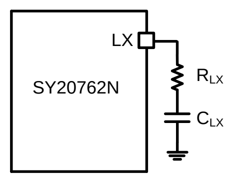
$$V_{INT}=\frac{V_{SEN}\times(R_{DOWN}+R_{UP})}{R_{DOWN}} \quad \text{unit: V}$$

V_{SEN} is 1.195V.

Spike Voltage Snubber Circuit

To prevent switching noise problem and get better EMC performance, a RC snubber circuit is strongly recommended especially when the average input current exceeds 2.4A.

The components should be placed close to LX pin on the PCB layout.



Input Capacitor C_{IN}

The ripple current through input capacitor is larger than

$$I_{CIN\_RMS}=\frac{V_{IN}\times(V_{OUT}-V_{IN})}{2\sqrt{3}\times L\times F_{SW}\times V_{OUT}}$$

X5R or X7R ceramic capacitors with larger than 4.7µF capacitance are recommended to handle this ripple current.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. This ripple voltage is related to the capacitance and its equivalent series resistance (ESR). For the best performance, it is recommended to use X5R or better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required capacitance can be calculated as:

$$C_{OUT}=\frac{I_{CC}\times(V_{OUT}-V_{IN})}{F_{SW}\times V_{OUT}\times V_{RIPPLE}}$$

$V_{RIPPLE}$is the peak to peak output ripple, I_{CC} is the setting constant charge current.

For SY20762N, output capacitor is paralleled with C_{BD} and C_{BAT}, for smaller output ripple noise, each capacitor with larger than 10µF capacitance is recommended.

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Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{I_{CC} \times F_{SW} \times 40\%}$$

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L \times F_{SW} \times V_{OUT}}$$

Where F_{SW} is the switching frequency and I_{CC} is the setting constant charge current.

The SY20762N is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be higher than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{CC} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Layout Design

The layout design of SY20762N regulator is relatively simple. For the best efficiency and minimum noise problems, the following components should be placed close to the IC: C_{SVIN}, L, and C_{BD}.

1) The loop of main MOSFET, rectifier diode, and C_{BD} must be as short as possible.

2) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance.

3) C_{SVIN} must be close to pin SVIN and GND.

4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

5) The small signal components R_{ICHG}, R_{UP} and R_{DOWN} must be placed close to IC and must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

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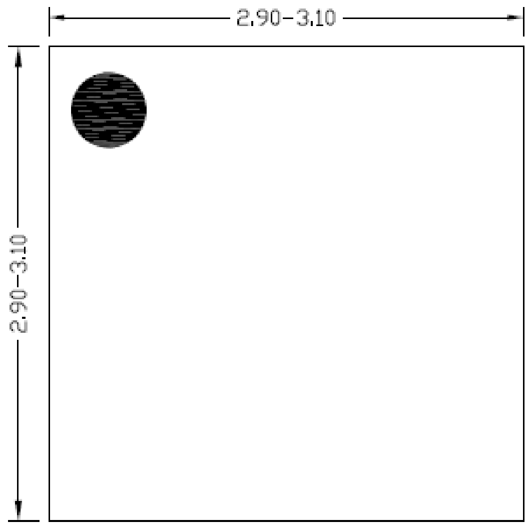
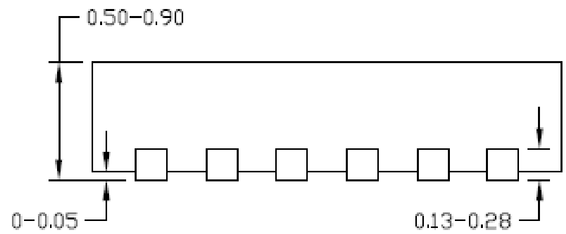
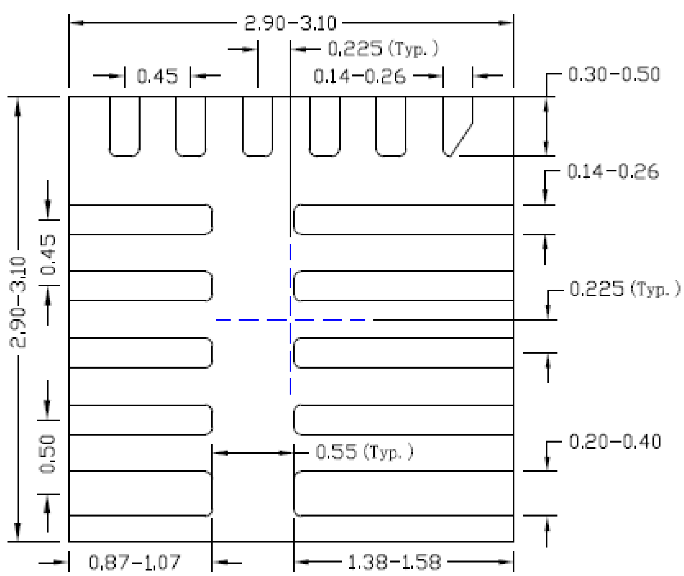
QFN3x3-16 Package Outline Drawing



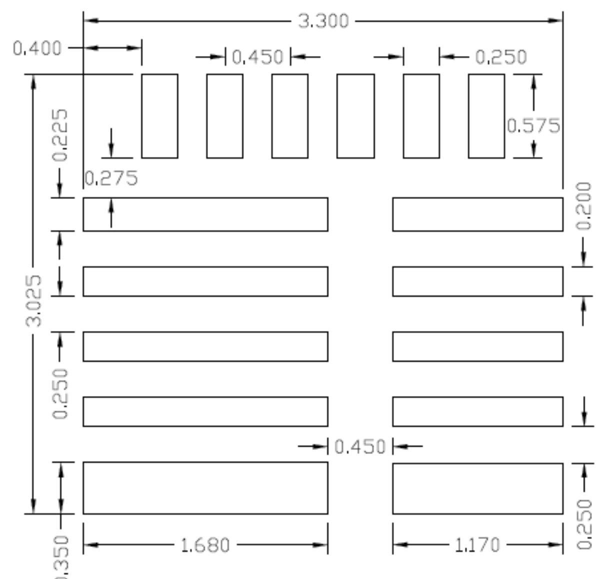
Top View



Side View



Bottom View



Recommended PCB layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

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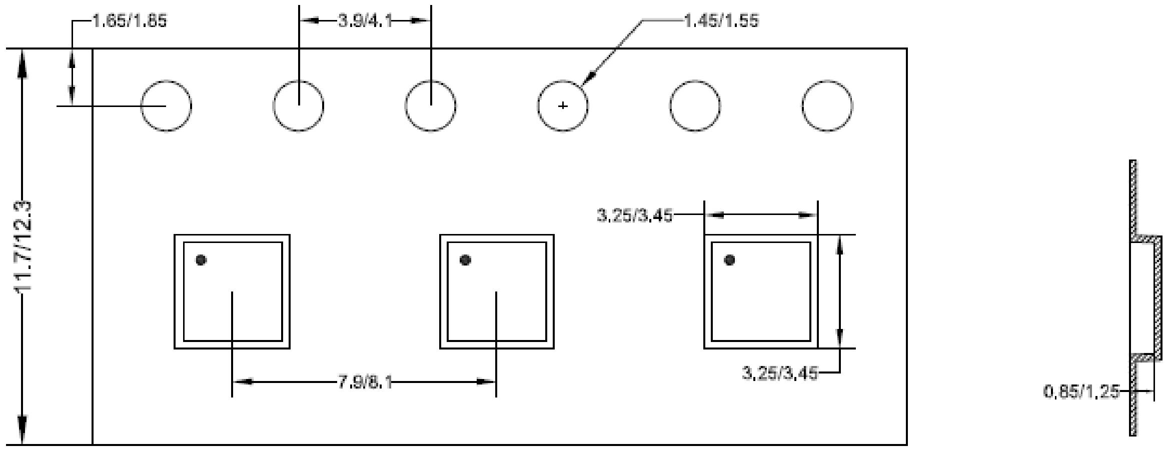
Taping & Reel Specification

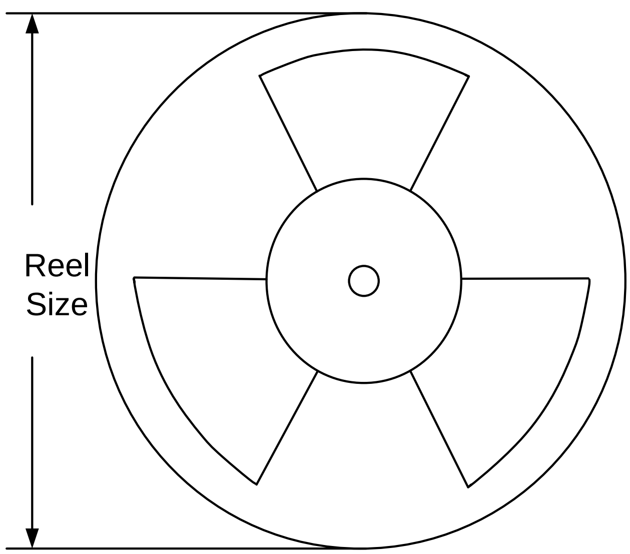
1. Taping orientation

QFN3x3



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x3	12	8	13"	400	400	5000

3. Others: NA

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