SY20778

Fully Integrated Synchronous Boost Converter with QC3.0 for Li-Ion Battery Power Bank Application

General Description

SY20778 is a wide input, high power density, fully integrated synchronous Boost converter with QC3.0 and PE+ for Li-Ion battery power bank application. With the extremely low $R_{DS(ON)}$ switch, SY20778 provides high efficiency with small size. It can provide up to 20W output power.

A half bridge with 0.3MHz or 0.5MHz switching frequency is integrated to achieve power conversion. The Boost convertor adopts peak current control to regulate the SYS voltage and SYS current. The light load status is monitored in the register and the MCU can read this status to shut down the chip to achieve extremely low power loss. In light load condition, the switching frequency will decrease according to the load automatically to increase the efficiency.

SY20778 is available in QFN4x4 package to minimize the PCB layout size for portable applications.

Ordering Information

SY20778 □(□,□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20778QYC	QFN4x4-20	

Features

- Integrated N-Channel MOSFETs with 16V Voltage Rating and Extremely Low $R_{DS(ON)}$ for
  - Linear Switch
  - Half Bridge
- 0.3MHz or 0.5MHz Selectable Switching Frequency to Minimize Peripheral Circuit Design
- Up to 20W Output Power
- I^2C Controls
  - Programmable Peak Current Limit
  - Programmable Over Current Limit for SYS Load
- Integrated SYS Current Sense
- Do+/Do- Divider Mode Compliant
- QC3.0 Class a Output Compliant
  - 5V4A
  - 9V/2.22A
  - 12V/1.67A
- MTK PE+ Compliant
- Host Enable Control for Standby Mode
- Over Temperature Protection
- Battery UTP/OTP
- Light Load Status Indication

Applications

- Single Cell Li-Ion Power Bank
- Multiple Output Ports Charger

Typical Applications

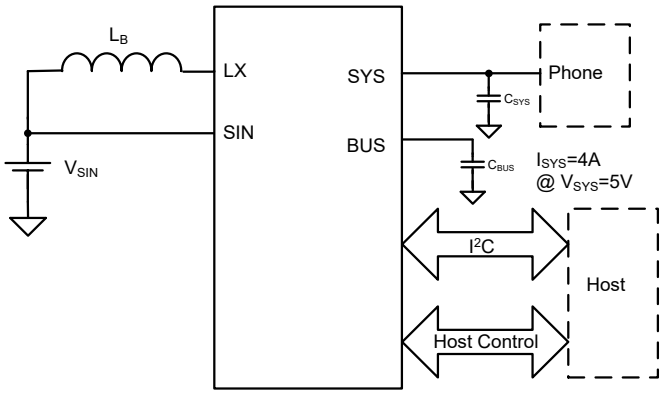
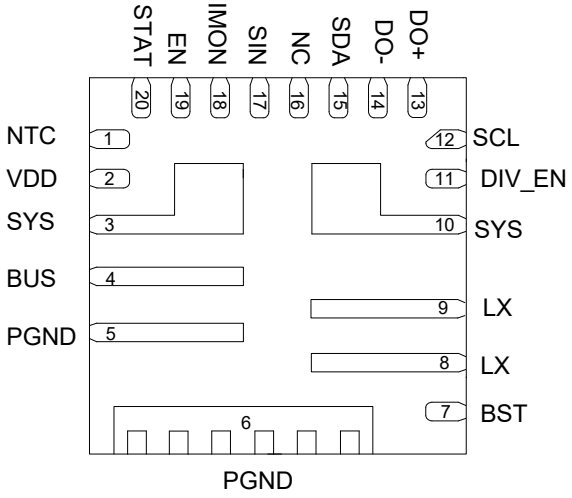


Figure 1. Simplified Schematic

Pinout (Top view)



(QFN4x4-20)

Top Mark: BLN*xyz* (device code: **BLN**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
NTC	1	Thermal protection and battery detection pin. UTP threshold is about 80% of VDD and OTP threshold is about 30% of VDD.
VDD	2	Internal linear regulator output. VDD is the output of 3.3V linear regulator. Connect a 1μF ceramic capacitor from VDD to GND.
SYS	3,10	System load pin. Connect a MLCC from this pin to ground to decouple the high frequency noise.
BUS	4	Connection point for reverse blocking FET and bypass linear switch. Connect a MLCC from this pin to ground to decouple the high frequency noise.
PGND	5,6	Power ground pin.
BST	7	Boot strap pin. Connect a MLCC from this pin to LX pin.
LX	8,9	Switch node pin. Connect an external inductor from this pin to SIN pin.
DIV_EN	11	Divider mode enable pin. Pull it high to disable divider mode or low to enable it.
DO+	13	USB D+ for system connection. Support Divider mode and BC1.2 and QC3.0 handshake.
DO-	14	USB D- for system connection. Support Divider mode and BC1.2 and QC3.0 handshake.
SDA	15	I^2C Interface data.
SCL	12	I^2C Interface clock.
NC	16	Let it float.
SIN	17	Input voltage sense pin. Connect it to the inductor terminal.
IMON	18	Buffered current pin. In Boost mode, IMON outputs the current of LNFET. $V_{IMON}=I\times R_{IMON}/80k$
EN	19	Whole chip enable pin. When SIN is present, pull it high to enable the IC and low to shut down the IC.
STAT	20	Boost status indication pin. It is an open drain output pin which can be used for turning on a LED to indicate Boost status. When Boost is working, the LED will be on. STAT pin will be pulled low for 200μs to generate an INT when QC detection is done or the voltage of QC request is changed.

Functional Block Diagram

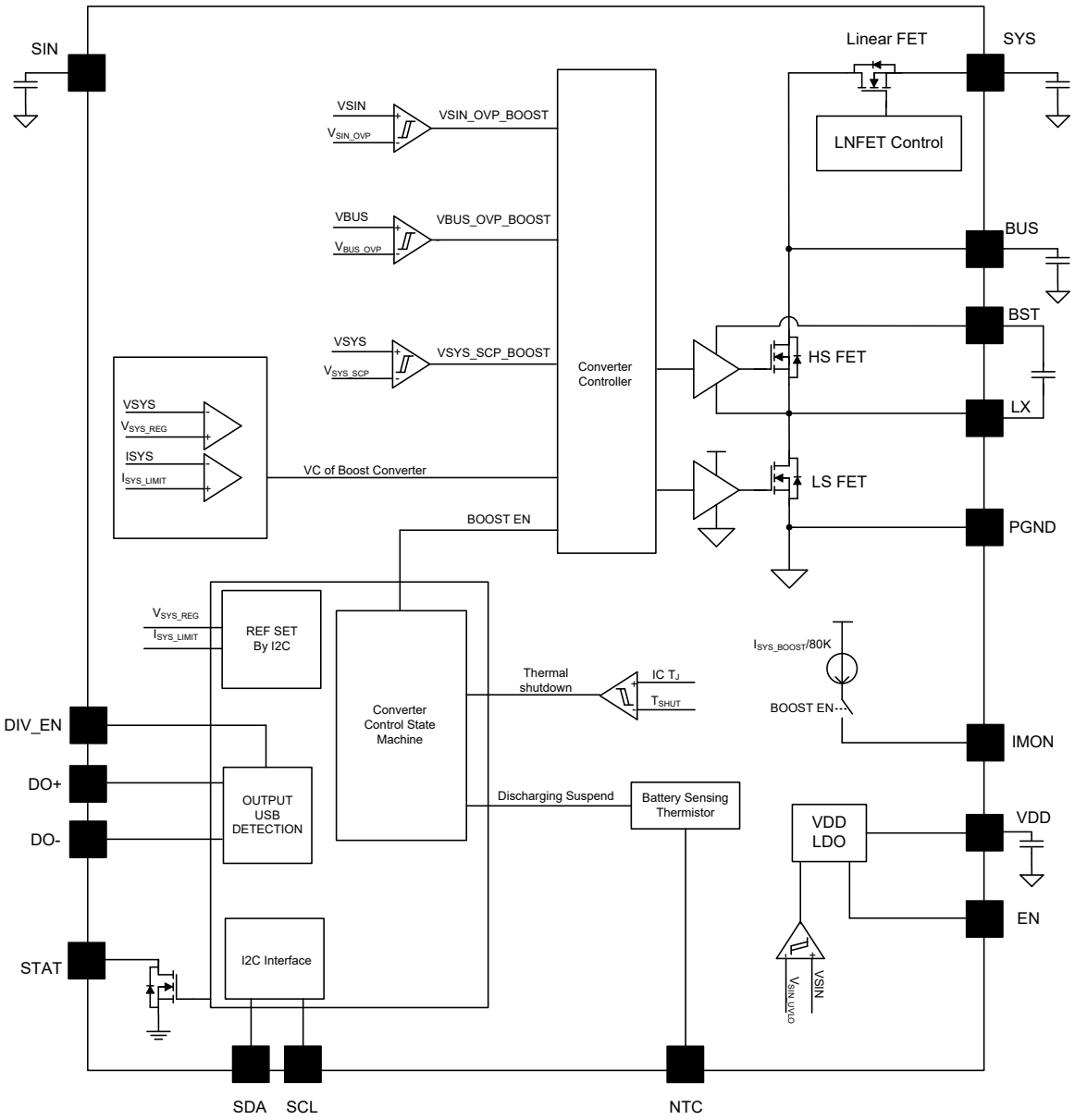


Figure 2. Functional Block Diagram

Absolute Maximum Ratings (Note 1)

STAT, LX, BUS, SIN, SYS, EN, DIV_EN ---------- -0.5~18V
SCL, SDA, DO+, DO- ---------- -0.5~6V
VDD, NTC, IMON ---------- -0.5- 4V
BST-LX ---------- -0.5-4V
Power Dissipation, P_D @ T_A = 25°C, ---------- 2.5 W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 30 °C/W
θ_{JC} ---------- 15 °C/W
Junction Temperature Range ---------- -40°C to +150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
Storage Temperature Range ---------- -65°C to 125°C

Recommended Operating Conditions (Note 3)

STAT, LX, BUS, SIN, SYS, EN, DIV_EN ---------- less than 16V
SCL, SDA, DO+, DO- ---------- -0.3 -5.5V
VDD, NTC, IMON ----------0-3.6V
BST-LX ----------0-3.6V
Junction Temperature Range ---------- -20°C to 100°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

T_A=25°C, T_A=T_J, V_{SIN}=3.5V, GND=0V, L_B=1μH, R_{IMON}=20kΩ, C_{SIN}=20μF, C_{BUS}=60μF, C_{SYS}=20μF, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Quiescent Current						
I_{SIN}	SIN Leakage Current	EN pull down			10	μA
I_{BOOST}	Boost Null-Load Input Current	V_{SIN}=4.35V,V_{SYS}=5V, I_{SYS}=0V, Converter switching		2		mA
Input Power Supply						
V_{SIN}	Input Supply Voltage	SIN_OVP is enabled.	3		4.5	V
$V_{SINUVLO}$	Input Voltage UVLO Threshold	Falling edge	2.5	2.6	2.7	V
V_{UVHYS}	Input Voltage UVLO Hysteresis	Rising edge		280		mV
V_{SINOVP}	Input Voltage OVP Threshold	Rising edge	4.55			V
$V_{SINOVPHYS}$	Input Voltage OVP Hysteresis	Falling edge		0.1		V
LDO Output						
V_{VDD}	VDD Voltage	V_{BUS}=5V		3.3		V
I_{VDD}	VDD Source Current	V_{VDD}=2.8V	80		210	mA
Linear FET						
R_{LNFT}	$R_{DS(ON)}$ of the Linear NFET			12		mΩ
I_{SYSMAX}	System Current Limit Tolerance	Reg02[4:2]=000, V_{SYS}<8.4V, I_{SYS_LIMIT}=1A	-10		10	%
Boost Converter Output Voltage and Current Bias						
V_{BOVP}	BUS Voltage OVP Threshold	Rising edge	13			V
$V_{BOVPHYS}$	BUS Voltage OVP Hysteresis	Falling edge		1		V
V_{SYS}	SYS Voltage Tolerance		-1		1	%
I_{SYS_LOW}	OTG Light Load Threshold	REG02[1:0]=10,I_{SYS_LOW}=50mA, falling edge	2	30	75	mA
		REG02[1:0]=11,I_{SYS_LOW}=100mA, falling edge	70	95	120	mA
$I_{PEAK\_MAX\_BT}$	Boost Mode Max Peak Current Tolerance	REG03[7:5]=111, $I_{PEAK\_MAX\_BT}$=11.2A	-15		15	%

Other General Parameters						
Battery Thermal Protection NTC						
UTP	Under Temperature Protection	Rising edge	78%	80%	82%	
	Under Temperature Protection Hysteresis	Falling edge		5%		
OTP	Over Temperature Protection	Falling edge	28%	30%	32%	
	Over Temperature Protection Hysteresis	Rising edge		2%		
Power MOSFET						
R_{HSFT}	$R_{DS(ON)}$ of High-Side NFET			12		mΩ
R_{LSFT}	$R_{DS(ON)}$ of Low-Side NFET			5		mΩ
Logic Level and Timing						
V_{LOW}	EN,SCL,SDA, DIV_EN Low Level Threshold				0.4	V
V_{HIGH}	EN,SCL,SDA, DIV_EN Low Level Threshold		1.3			V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

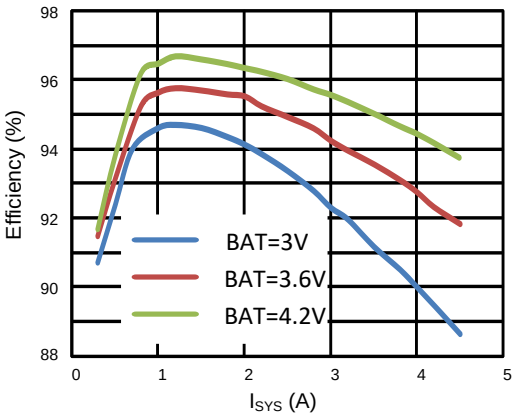
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

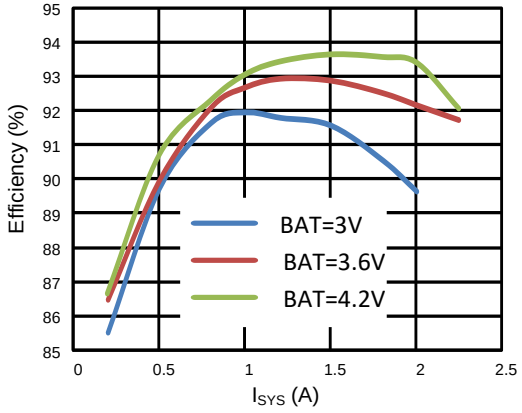
Typical Performance Characteristics

(T_A=25°C, V_{SIN}=4V, unless otherwise specified.)

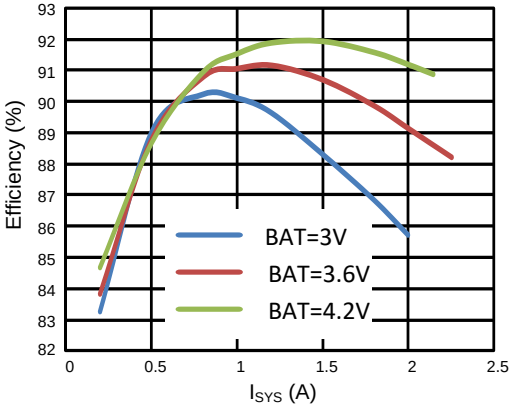
Efficiency vs. I_{SYS} (Boost Mode,CV=5V)



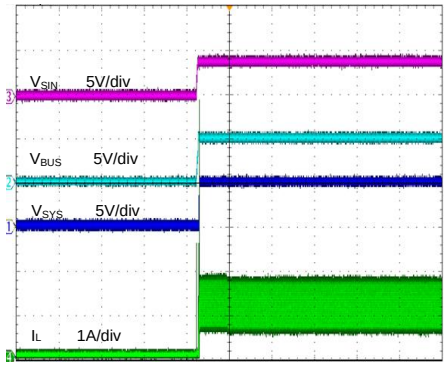
Efficiency vs. I_{SYS} (Boost Mode,CV=9V)



Efficiency vs. I_{SYS} (Boost Mode,CV=12V)

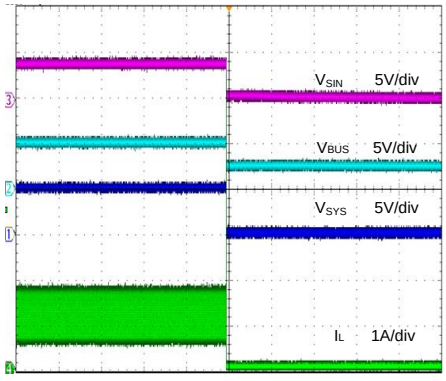


4V V_{SIN} Power ON



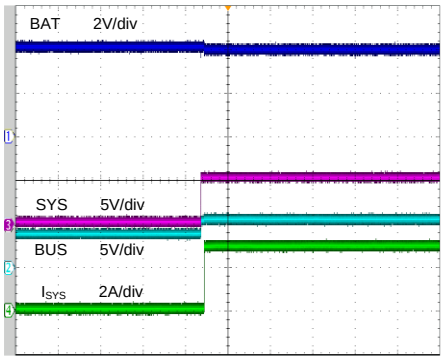
Time (200ms/div)

4V V_{SIN} Power OFF



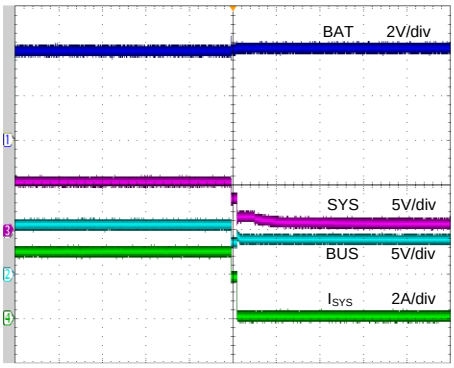
Time (200ms/div)

5V Boost Mode ON by I²C



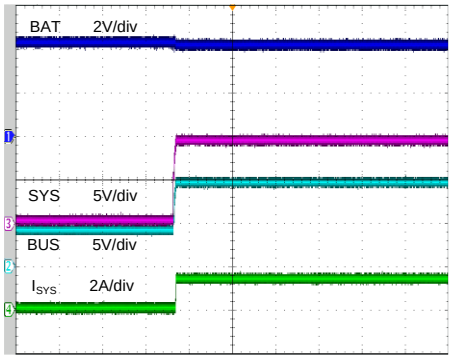
Time (200ms/div)

5V Boost Mode OFF by I²C



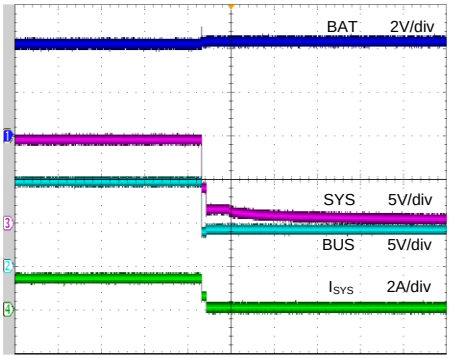
Time (200ms/div)

9V Boost Mode ON by I²C



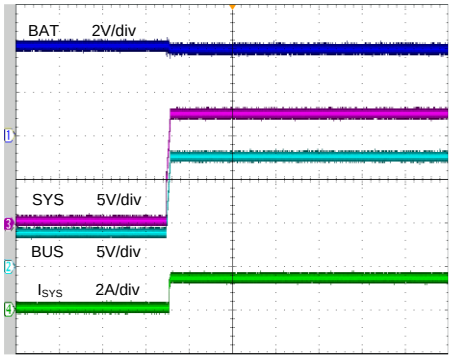
Time (200ms/div)

9V Boost Mode OFF by I²C



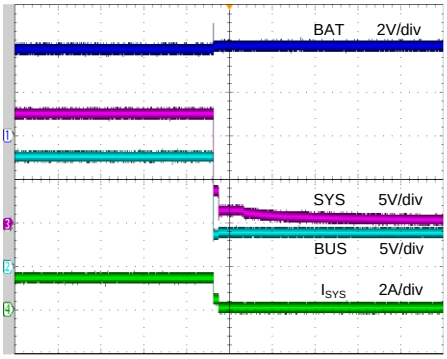
Time (200ms/div)

12V Boost Mode ON by I²C



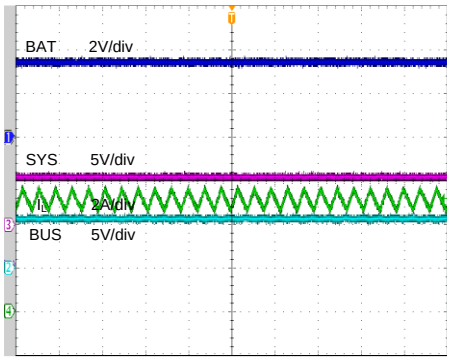
Time (200ms/div)

12V Boost Mode OFF by I²C



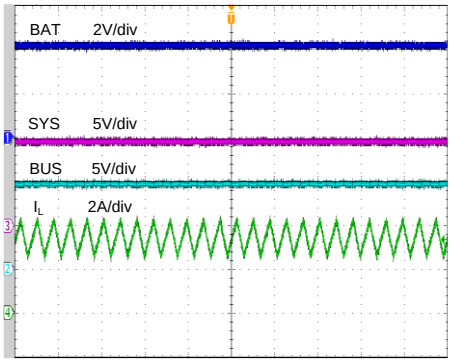
Time (200ms/div)

5V Boost Steady State



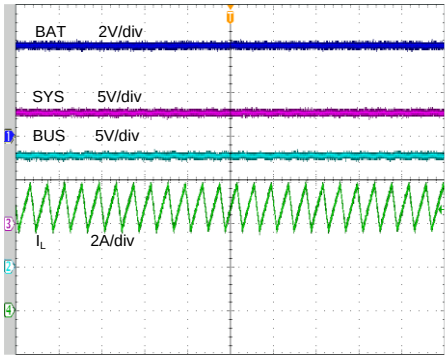
Time (4μs/div)

9V Boost Steady State



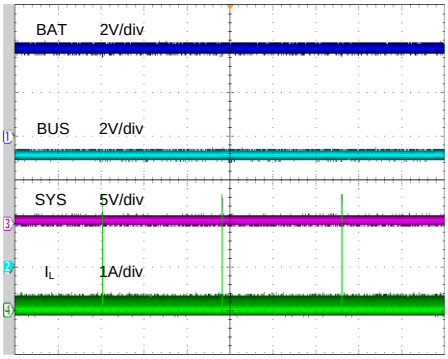
Time (4μs/div)

12V Boost Steady State



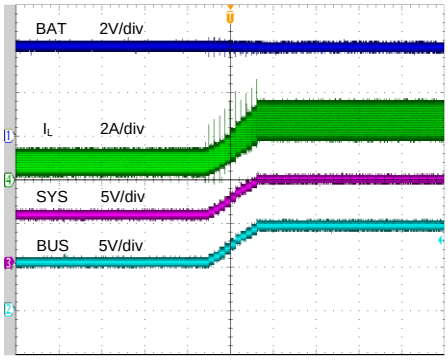
Time (4μs/div)

Boost SYS Short



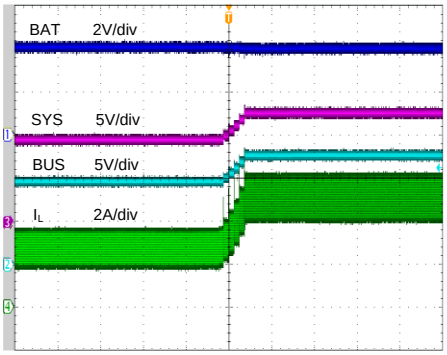
Time (200ms/div)

Boost 5V to 9V



Time (10ms/div)

Boost 9V to 12V



Time (10ms/div)

Detailed Description

SY20778 is a wide input, high power density, fully integrated synchronous Boost converter with QC3.0 and PE+ for Li-Ion battery power bank application. It is highly integrated with linear FET(LNFET), high-side switching FET(HSFET), low-side switching FET(LSFET). With the extremely low $R_{DS(ON)}$ switch, SY20778 provides high efficiency with small size. It can provide up to 20W output power.

General Function Description

1Device Power ON Reset (POR)

The internal bias circuits are powered from the higher voltage of V_{BUS} and V_{SIN}. When V_{SIN} rises above V_{SIN_UVLO} and EN is high, the IC will be active, the VDD LDO will be powered on. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

2 Device Power UP Operation

2.1 Power UP VDD Regulation (LDO)

The VDD LDO supplies internal bias circuits as well as the HSFET and LSFET gate drivers. The LDO also provides bias rail to NTC external resistors. The pull-up rail of STAT can be connected to VDD as well. The VDD will be enabled when V_{SIN} is above V_{SIN_UVLO} and EN is high.

2.2 Converter Power UP

If V_{SIN} is above V_{SIN_UVLO}, VDD LDO will stay off until EN is high. When EN is low, the IC will be shut down to save the power. The Boost converter will turn on if both EN is high and Boost_Enable(REG01[5]) is set to 1. SY20778 always monitors the SYS voltage and the current of LNFET. When V_{SYS} is lower than $V_{SHORTSYS}$, the linear FET will modulate the current to be saw tooth shape from 0A to 1.7A for short circuit protection recovery. SY20778 will try to recover for 5ms per 0.7s when SYS is shorted. When the current of LNFET exceeds the SYS current limit (set by REG02[4:2]), the Boost converter will decrease the duty cycle to limit the output current of Boost converter.

As a synchronous Boost converter, the device deploys a high efficient 0.3MHz or 0.5MHz step-up switching regulator. The constant-off peak current converter keeps tight control of the output voltage and output current, which simplifies the output filter design.

An internal compensation network allows using ceramic capacitors at the output of the converter. The peak current of I_L sensed by LSFET is compared to the internal error control signal to vary the duty cycle of the converter. The cycle-by-cycle current limit is implemented due to the peak current control mode.

3 Boost Mode Operation

SY20778 supports Boost converter operation to deliver power from the battery to other portable devices through the SYS pin. The Boost mode output current rating supports maximum output current up to 4A at LV output mode and 2.22A at HV output mode to charge smart-phones and tablets.

In Boost mode, SY20778 deploys a 300kHz or 500kHz peak current mode step up converter to deliver power from input to SYS. The Boost mode state can be monitored by reading the Boost bit (Reg00[6]).

4 SYS Output Management

4.1 SYS Voltage Set

The Boost converter modulates the SYS voltage according to the handshake of DO+/DO- or Downstream_Voltage_Set bit (REG05[4:2]).The Boost converter will work in CV mode until the SYS current exceeds the SYS current limit.
When Downstream_OUT_SEL is 1, SYS voltage will be set by Downstream_Voltage_Set bit(REG05[4:2]). When Downstream_OUT_SEL is 0 and Downstream_QC_ EN is 1, SYS voltage will be set by DO+/DO-.

4.2 SYS Current Limit

In supply mode, once SYS current exceeds I_{SYS_Limit}, SYS current will be limited to I_{SYS_Limit} by regulating the duty cycle of Boost converter. The SYS current limit loop will take control of Boost converter until the SYS current decreases under I_{SYS_Limit}.
SYS current limit is programmed by I_{SYS_Limit} bit (REG02[4:2]).

4.3 Boost Status Indication Description

1. **In Boost mode** – Pull and keep STAT pin low;
2. **Not in Boost Mode** – When fault happens, pull output high. Fault mode includes SIN OVP, SYS SCP, SYS OVP BAT UTP/OTP.

Connect a LED from VDD to STAT pin. If the LED is on, it will be indicated in Boost mode, otherwise, not.

Boost status is recorded in REG00[6]

5 The Monitor of Current

The host can monitor the current of SY20778 by measuring the voltage of IMON.

In Boost mode, IMON monitors the output current of LNFET. The max voltage of IMON must be lower than 2V, the proper R_{IMON} can be derived from following formula:

$V_{IMON}=I\times R_{IMON}/80k$

6 Interrupt to Host (INT)

In some applications, the host does not always monitor the Boost operation. The INT notifies the system on the device operation. The following events will generate 200μs INT pulse.

- DO+ DO- detection is done
- The request voltage of DO+ DO- is changed

After INT is generated, the MCU must read I^2C to clear the INT, otherwise the INT will be sent every 800ms.

7 Protection Descriptions

7.1 Thermal Protection-Thermal protection for battery is achieved through NTC pin in Boost mode. The basic scheme is shown in application information. Thermal shutdown is active for the device itself. The IC returns to normal work when the temperature returns to normal range again.

7.2 Short Circuit Protection- There is a SYS short circuit protection in SY20778. When V_{SYS} is lower than $V_{SHORTSYS}$, the linear FET will modulate the current to be saw tooth shape from 0A to 1.7A for short circuit protection recovery. SY20778 tries recovery for 5ms every 0.7s.

7.3 Over Voltage Protection- When V_{BUS} or V_{SIN} is higher than the over voltage protection threshold, the half bridge will stop Boost operation immediately. It will return to normal work when the monitored voltage returns to normal level. Input voltage has UVLO and OVP, which would make the device shutdown, SY20778 will return to normal work when the V_{SIN} returns to normal range.

Applications Information

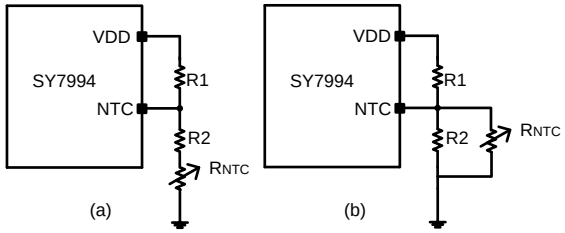
1 Applications Information

Because of the high integration of SY20778, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{SIN}, BUS capacitor C_{BUS}, inductor L, NTC resistors R1, R2, need to be selected for the target applications specifications.

1.1 NTC Resistor:

SY20778 monitors battery temperature by measuring the VDD voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K ($K= V_{NTC}/V_{VDD}$) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.

Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps of Figure (a) are:

1. Define K_{UT}, K_{UT} =80%
2. Define K_{OT}, K_{OT} =30%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2

$$R2 = \frac{K_{OT}(1-K_{UT})R_{UT} - K_{UT}(1-K_{OT})R_{OT}}{K_{UT} - K_{OT}}$$

5. Calculate R1

$$R1 = (1/K_{OT} - 1)(R2 + R_{OT})$$

If choose the typical values K_{UT} =80% and K_{OT}=30%, then

$$R2 = 0.12R_{UT} - 1.12R_{OT}$$
$$R1 = 2.333(R2 + R_{OT})$$

1.2 Input Capacitor C_{SIN}:

C_{SIN} acts as the input capacitor of Boost converter. The input voltage ripple is calculated as below:

$$V_{Ripple\_IN\_Boost} = \frac{D \times V_{SIN}}{8 C_{SIN} F_{SW}^{2} L}$$

Where F_{SW} is the switching frequency.

At least a 20μF ceramic capacitor is suggested.

1.3 BUS Capacitor C_{BUS}:

C_{BUS} is the output capacitor of Boost converter. C_{BUS} reduces the bus voltage ripple and ensures the stability of Boost. The output current ripple rms value is :

$$I_{CBUS\_RMS} = \frac{\Delta I}{2\sqrt{3}}$$

Where ΔI is the current ripple of the inductor.

At least a 60μF ceramic capacitor is suggested.

1.4 Inductor L:

Inductor selection trades off among cost, size, and efficiency. A lower inductance value corresponds with smaller size, but results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. However, a higher inductance value benefits from lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss. An inductor must not saturate under the worst-case condition.

As in Boost mode,

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{SIN}(1 - V_{SIN}/V_{BUS\_MAX})}{F_{SW} \times I_{DIS,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{DIS,MAX}$ is the maximum discharge current.

SY20778 is quite tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{DIS,MAX} + \frac{V_{SIN}(1 - V_{SIN}/V_{BUS\_MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

The range of 0.68μH to 1.5μH inductance is suggested to get the good stability with the internal compensation circuits.

1.5 Layout Design:

The layout design of SY20778 regulator is relatively simple. For the best efficiency and to minimum noise problems, we should place the following components close to the IC: C_{BUS}, C_{SYS}, L.

1) It is desirable to maximize the PCB copper area adjacent to GND pin to achieve the best thermal performance and noise performance. If the board space allows, a ground plane is highly desirable.

2) C_{SYS} must be close to pins SYS and GND, C_{BUS} must get close to pins BUS and GND. The loop area formed by C_{SYS} and GND, C_{BUS} and GND must be minimized.

The following figure is the recommended layout design.

3) The PCB copper area adjacent to LX pin must be minimized to avoid the potential noise problem.

4) In high current applications, a RC snubber circuit should be placed between LX and GND for better EMI.

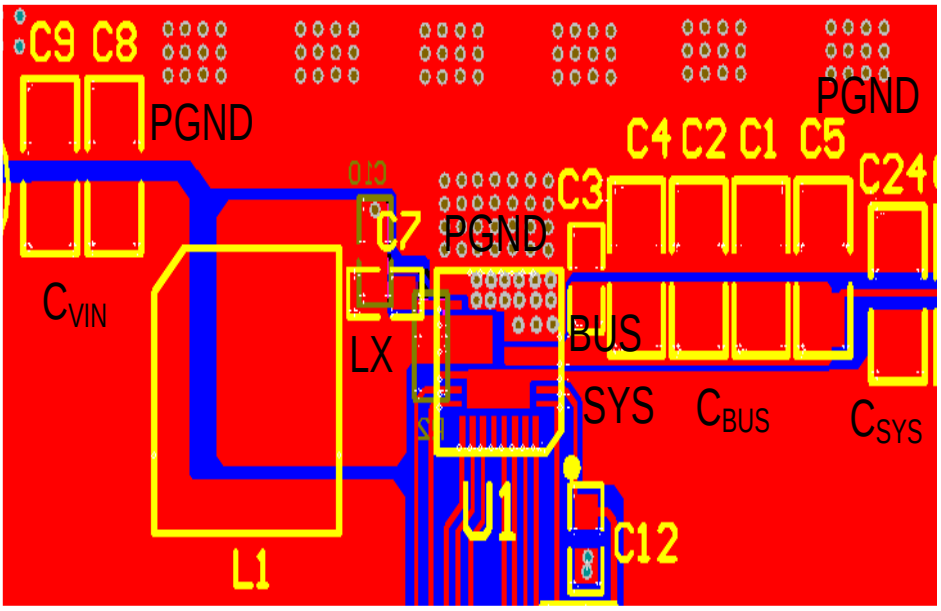


Figure3. PCB Layout Suggestion

Typical Applications

Boost Converter

In the application of Boost converter, SY20778 works as a step up converter with max 4A output current. The SYS voltage can be set according to the handshake of DO+/DO- or Downstream_Voltage_Set bit(REG05[4:2]). The Boost converter will work in CV mode until the SYS current exceeds the SYS current limit. The SYS current will be limited to I_{SYS_Limit} when it exceeds I_{SYS_Limit}. SY20778 features all the protections with SYS SCP, BUS OVP, SIN OVP, NTC, thermal shutdown.

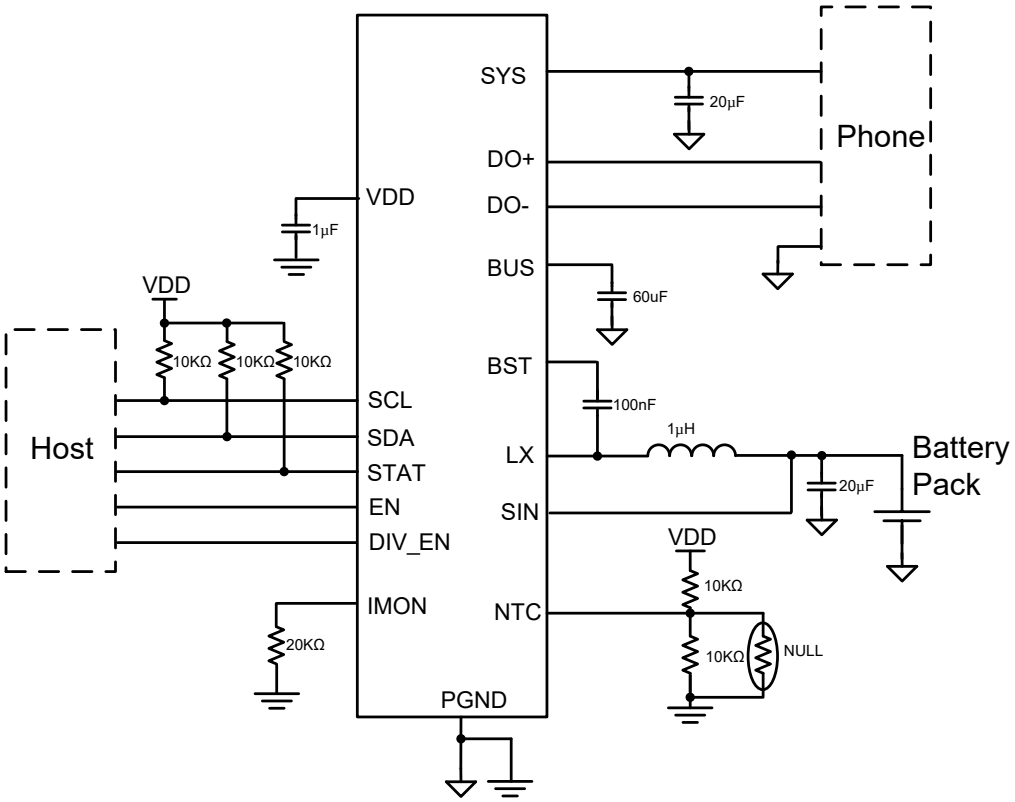


Figure 4. Boost Converter Application Schematic

Register Description

Boost Converter Registers

The SY20778 supports 6 Boost converter registers that use either Write-Word or Read-Word protocols, as summarized in Table 1. 04H are “read only” registers and can be used for identifying the SY20778.

Table 1. Boost Converter Register Summary

Register Address	Register Name	Read/Write	Default
00H	Status/Control Register	Read or Write	XXH
01H	Control Register	Read or Write	84H
02H	Current Register	Read or Write	XXH
03H	Peak Current Register	Read or Write	89H
04H	Vendor/PN/Rev Register	Read	XXH
05H	Quick Discharge Register1	Read or Write	XXH
07H	Quick Discharge Register2	Read or Write	XXH

1 REG00

Table 2. Status/Control Register (00H)

Bit	Bit Name	R/W	Description
7	Reset	R/W	Write 1 to reset all the parameters, auto clear
6	Boost	R	1: In Boost mode 0: Not in Boost mode
5:4	Reserved	NA	NA
3	BST_LLOAD	R	0:I_{SYS}> I_{SYS_L} 1:I_{SYS}< I_{SYS_L} ,Boost mode light load
2	SIN_UVLO	R	0: V_{SIN}> $V_{SINUVLO}$ 1: V_{SIN}< $V_{SINUVLO}$
1:0	Reserved	NA	NA

2 REG01

Table 3. Control Register (01H)

Bit	Bit Name	R/W	Description
7:6	Reserved	NA	NA
5	Boost_Enable	R/W	0: Disable Boost converter. 1: Enable Boost converter. (default)
4	SIN_OVP	R/W	0: Enable. (default) 1: Disable.
3	VSYS_COMP	R/W	System output voltage compensation in 5V mode. 1: 5.25V; 0: 5V(default).
2:1	Reserved	NA	NA

0	F_{SW}	R/W	Boost converter switching frequency set. 0: 500kHz (default) 1: 300kHz

3 REG02

Table 4. Current Register (02H)

Bit	Bit Name	R/W	Description
7:5	Reserved	NA	NA
4:2	I_{SYS_Limit}	R/W	SYS current limit 000: 1A 001: 1.5A 010: 2A 011: 2.5A 100: 3A 101: 3.5A (default) 110: 4A 111: 4.5A
1	Boost_Lightload_EN	R/W	0: Disable Boost light load detection. 1: Enable Boost light load detection (default)
0	Boost _Lightload	R/W	0:50mA 1:100mA (default)

4 REG03

Table 5. Peak Current Register (03H)

Bit	Bit Name	R/W	Description
7:5	I_{PEAK}	R/W	000: 3.8A 001: 4.8A 010: 6A 011: 7A 100: 8A 101: 9A 110: 10A 111: 11.2A (default)
4:0	Reserved	NA	NA

5 REG04

Table 6. Vendor/PN/Rev Register (04H)

Bit	Bit Name	R/W	Description
7:5	Vendor_Code	R	101: Identify the supplied
4:3	PN	R	11: SY20778
2:0	Revision	R	001: Revision 1.0 010: Revision 1.1 011: Revision 1.2 ……

6 REG05

Table 7. Quick Discharge Register1 (05H)

Bit	Bit Name	R/W	Description
7:5	Downstream_Voltage_Request	R	Record the voltage of downstream request. 111:12V(PE) 110:9V(PE) 101:7V(PE) 100:5V(PE) 011:12V(QC) 010:9V(QC) 001:Continuous mode (QC) 000:5V(QC)
4:2	Downstream_Voltage_Set	R/W	Set the output voltage of SYS. 111:12V(PE) 110:9V(PE) 101:7V(PE) 100:5V(PE) 011:12V(QC) 010:9V(QC) 001:Continuous mode (QC) 000:5V(default)
1:0	Continuous_Mode_UP_DOWN	R/W	QC3.0 continuous mode control. In continuous mode, in order to increase the SYS voltage by 200mV, these 2 bits must be set to 01 and then to 00; in order to decrease the SYS voltage by 200mV, these bits must be set to 10 and then to 00. 10:DOWN 01:UP 00:HOLD (defalut) 11:HOLD

7 REG07

Table 8. Quick Discharge Register2 (07H)

Bit	Bit Name	R/W	Description
7:3	Reserved	NA	NA
2	Downstream_Device_QC_Support	R	Indicate whether the downstream device supports QC. 1: Support 0: Not support
1	Downstream_QC_EN	R/W	1:Enable QC2.0 and QC3.0 Detection(default) 0:Disable QC2.0 and QC3.0 Detection
0	Downstream_OUT_SEL	R/W	SYS output voltage control. 1:Set by REG05[4:2] 0:SY20778 set according DO+/DO- (default)

I²C Interface

SY20778 uses I²C compatible interface for flexible discharging parameter programming and instantaneous device status reporting. Only two BUS lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered as a slave.

The device operates as a slave device with address d4H, receiving control inputs from the master device like a micro controller or a digital signal processor. The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connected to the positive supply voltage via a current source or pull- up resistor. When the BUS is free, both lines are HIGH. The SDA and SCL pins are open drain.

1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

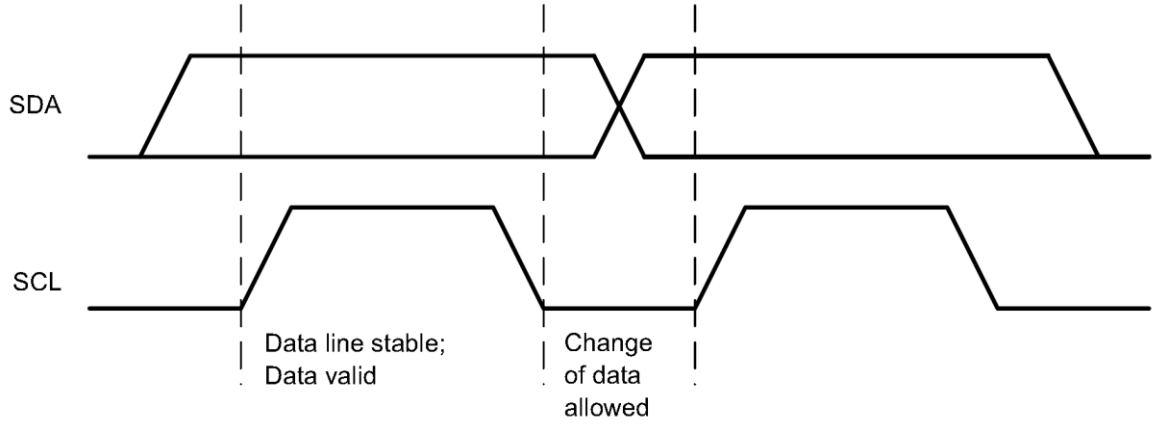


Figure 5. Bit Transfer on the I²C Bus

2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and will be free after the STOP condition.

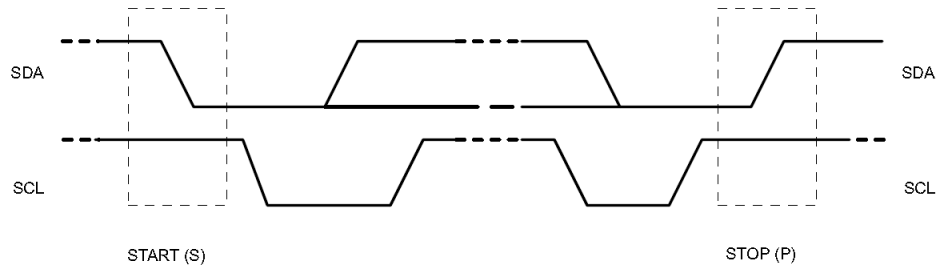


Figure 6. START and STOP conditions

3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data will transfer then continues when the slave is ready for another byte of data and releases the clock line SCL.

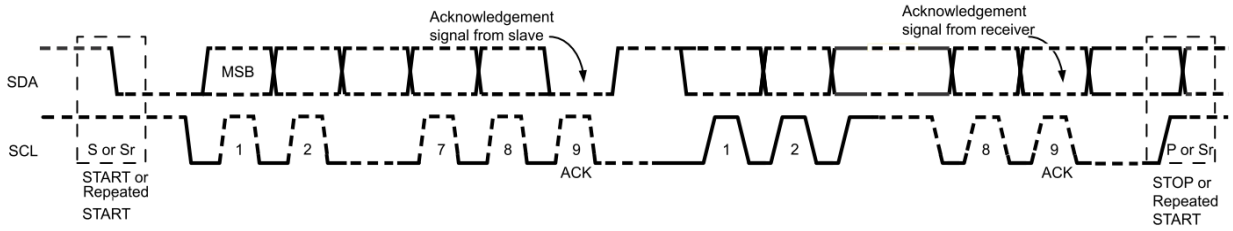


Figure 7. Data Transfer on the I^2C Bus

4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the not acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A “0” indicates a transmission (WRITE) and a “1” indicates a request for data (READ).

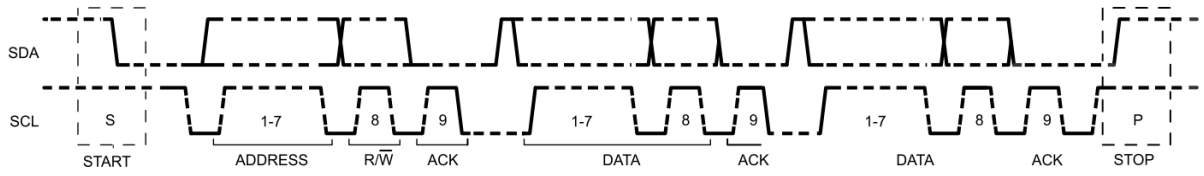


Figure 8. Complete Data Transfer

Single Read and Write

Figure 9. Single Write

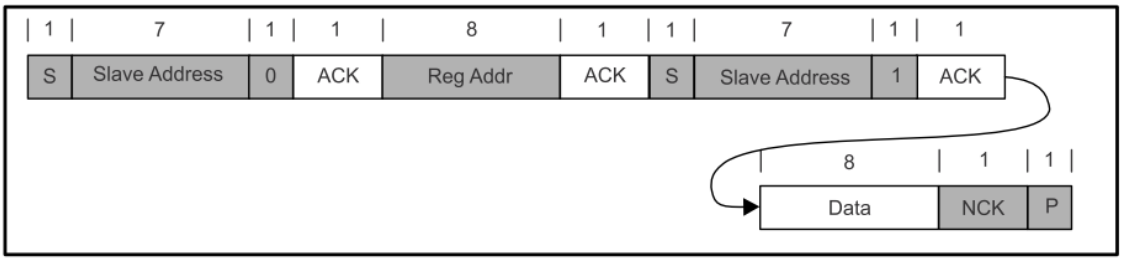
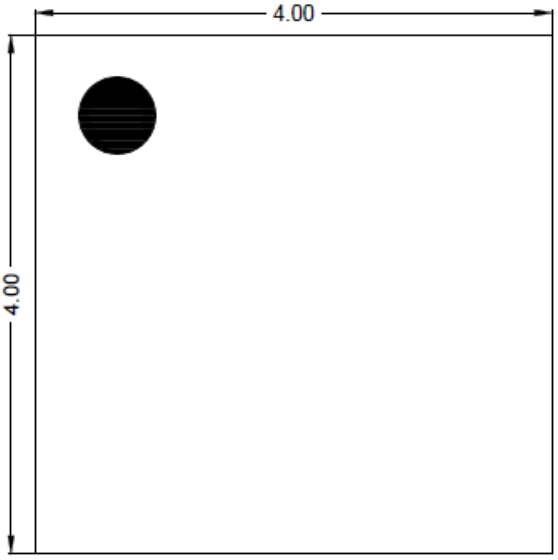


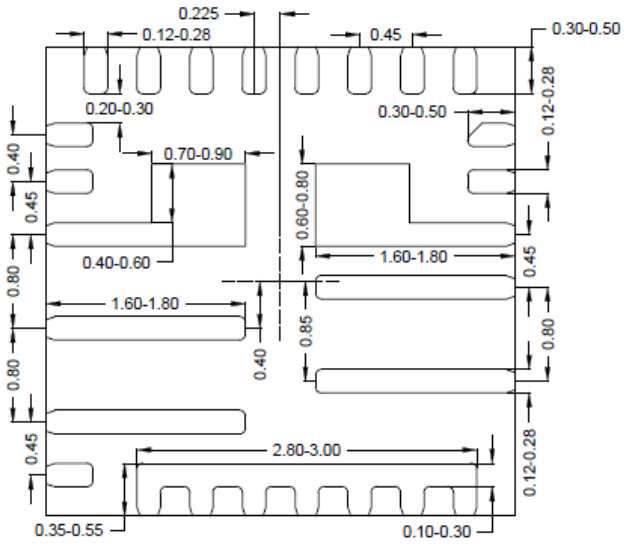
Figure 10. Single Read

If the register address is not defined, the IC will be sent back to NACK and return to the idle state.

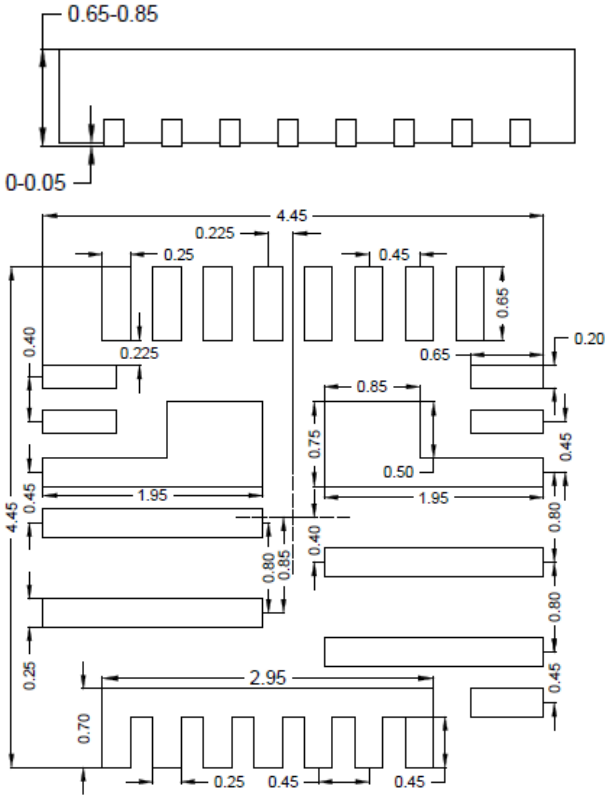
QFN4x4-20 Package Outline Drawing



Top View



Bottom View



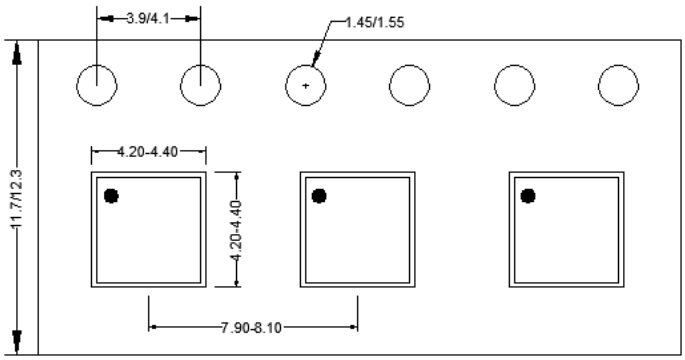
Side View

Recommended PCB layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

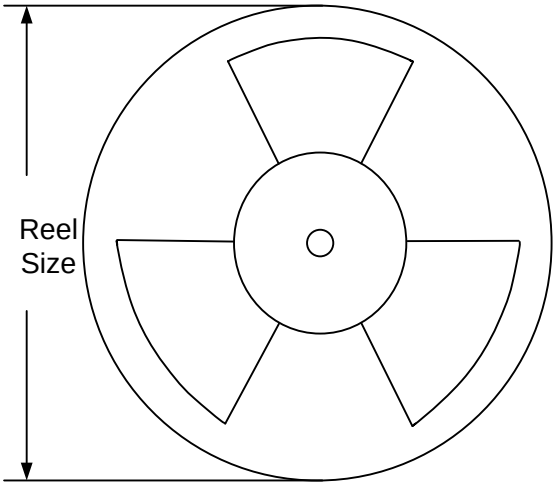
Taping & Reel Specification

1. QFN4x4 taping orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
QFN4x4	12	8	13"	400	400	5000

3. Others: NA

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